

# SN54LV574A, SN74LV574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS412G – APRIL 1998 – REVISED AUGUST 2003

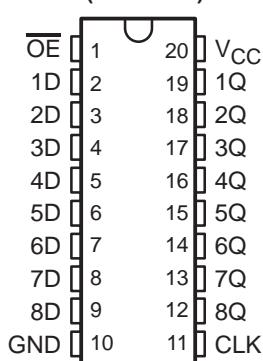
- 2-V to 5.5-V  $V_{CC}$  Operation
- Max  $t_{pd}$  of 10 ns at 5 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  
 $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  
 $>2.3$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

**SN54LV574A ... J OR W PACKAGE**

**SN74LV574A ... DB, DGV, DW, NS,**

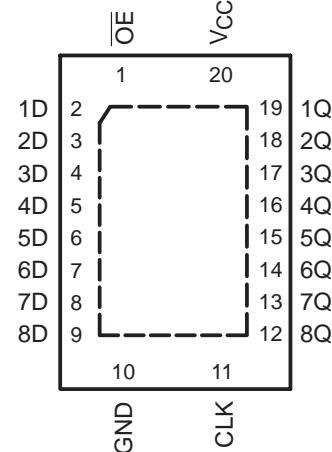
**OR PW PACKAGE**

**(TOP VIEW)**



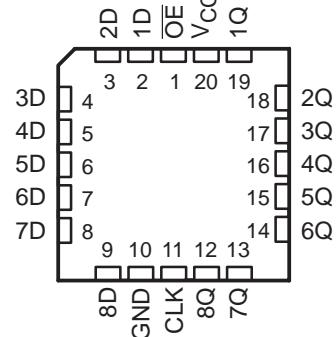
**SN74LV574A ... RGY PACKAGE**

**(TOP VIEW)**



**SN54LV574A ... FK PACKAGE**

**(TOP VIEW)**



## description/ordering information

### ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LV574ARGYR	LV574A
	SOIC – DW	Tube of 25	SN74LV574ADW	LV574A
		Reel of 2000	SN74LV574ADWR	
	SOP – NS	Reel of 2000	SN74LV574ANSR	74LV574A
	SSOP – DB	Reel of 2000	SN74LV574ADBR	LV574A
	TSSOP – PW	Tube of 70	SN74LV574APW	LV574A
		Reel of 2000	SN74LV574APWR	
		Reel of 250	SN74LV574APWT	
	TVSOP – DGV	Reel of 2000	SN74LV574ADGVR	LV574A
	VFBGA – GQN	Reel of 1000	SN74LV574AGQNR	LV574A
–55°C to 125°C	CDIP – J	Tube of 20	SNJ54LV574AJ	SNJ54LV574AJ
	CFP – W	Tube of 85	SNJ54LV574AW	SNJ54LV574AW
	LCCC – FK	Tube of 55	SNJ54LV574AFK	SNJ54LV574AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**description/ordering information (continued)**

The 'LV574A devices are octal edge-triggered D-type flip-flops designed for 2-V to 5.5-V  $V_{CC}$  operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

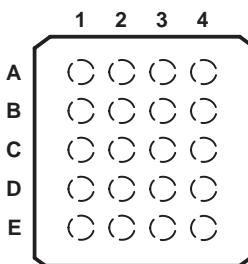
A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

**GQN PACKAGE  
(TOP VIEW)**



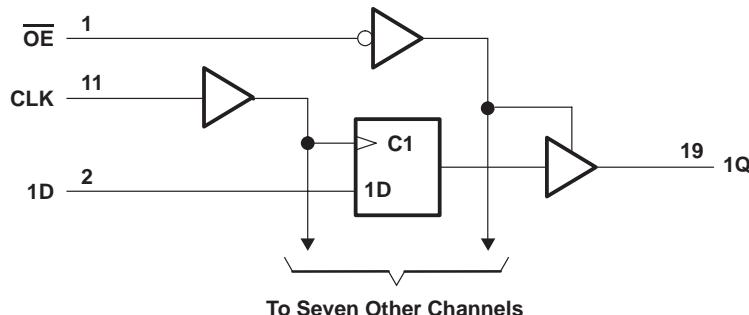
**terminal assignments**

	1	2	3	4
A	1D	$\overline{OE}$	$V_{CC}$	1Q
B	3D	3Q	2D	2Q
C	5D	4D	5Q	4Q
D	7D	7Q	6D	6Q
E	GND	8D	CLK	8Q

**FUNCTION TABLE  
(each flip-flop)**

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	H or L	X	$Q_0$
H	X	X	Z

**logic diagram (positive logic)**



Pin numbers shown are for the DB, DGV, DW, FK, J, NS, PW, RGY, and W packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, V <sub>CC</sub> .....	-0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V <sub>O</sub> (see Note 1) .....	-0.5 V to 7 V
Output voltage range applied in the high or low state, V <sub>O</sub> (see Notes 1 and 2) .....	-0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub> ) .....	±20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> ) .....	±50 mA
Continuous output current, I <sub>O</sub> (V <sub>O</sub> = 0 to V <sub>CC</sub> ) .....	±35 mA
Continuous current through V <sub>CC</sub> or GND .....	±70 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3): DB package .....	70°C/W
(see Note 3): DGV package .....	92°C/W
(see Note 3): DW package .....	58°C/W
(see Note 3): GQN package .....	78°C/W
(see Note 3): NS package .....	60°C/W
(see Note 3): PW package .....	83°C/W
(see Note 4): RGY package .....	37°C/W
Storage temperature range, T <sub>stg</sub> .....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 5.5 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51-7.
- 4. The package thermal impedance is calculated in accordance with JESD 51-5.

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**recommended operating conditions (see Note 5)**

		SN54LV574A			SN74LV574A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>CC</sub>	Supply voltage	2	5.5		2	5.5		V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		1.5			V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.7		V <sub>CC</sub> × 0.7			
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.7		V <sub>CC</sub> × 0.7			
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.7		V <sub>CC</sub> × 0.7			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5		0.5			V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.3		V <sub>CC</sub> × 0.3			
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.3		V <sub>CC</sub> × 0.3			
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.3		V <sub>CC</sub> × 0.3			
V <sub>I</sub>	Input voltage	0	5.5		0	5.5		V
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>	0	V <sub>CC</sub>		V
		3-state	0	5.5	0	5.5		
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V		-50		-50		µA
		V <sub>CC</sub> = 2.3 V to 2.7 V		-2		-2		mA
		V <sub>CC</sub> = 3 V to 3.6 V		-8		-8		
		V <sub>CC</sub> = 4.5 V to 5.5 V		-16		-16		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V		50		50		µA
		V <sub>CC</sub> = 2.3 V to 2.7 V		2		2		mA
		V <sub>CC</sub> = 3 V to 3.6 V		8		8		
		V <sub>CC</sub> = 4.5 V to 5.5 V		16		16		
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 2.3 V to 2.7 V		200		200		ns/V
		V <sub>CC</sub> = 3 V to 3.6 V		100		100		
		V <sub>CC</sub> = 4.5 V to 5.5 V		20		20		
T <sub>A</sub>	Operating free-air temperature	-55	125		-40	85		°C

NOTE 5: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LV574A			SN74LV574A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	2 V to 5.5 V	V <sub>CC</sub> - 0.1			V <sub>CC</sub> - 0.1			V
	I <sub>OH</sub> = -2 mA	2.3 V	2			2			
	I <sub>OH</sub> = -8 mA	3 V	2.48			2.48			
	I <sub>OH</sub> = -16 mA	4.5 V	3.8			3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	2 V to 5.5 V		0.1			0.1		V
	I <sub>OL</sub> = 2 mA	2.3 V		0.4			0.4		
	I <sub>OL</sub> = 8 mA	3 V		0.44			0.44		
	I <sub>OL</sub> = 16 mA	4.5 V		0.55			0.55		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V		±1			±1		µA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V		±5			±5		µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		20			20		µA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0		5			5		µA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		1.8			1.8		pF

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**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER		$T_A = 25^\circ\text{C}$		SN54LV574A		SN74LV574A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_W$	Pulse duration	CLK high or low	7	7	7	7	ns	
$t_{SU}$	Setup time	High or low before CLK↑	5.5	5.5	5.5	5.5	ns	
$t_H$	Hold time	Data after CLK↑	2	2	2	2	ns	

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER		$T_A = 25^\circ\text{C}$		SN54LV574A		SN74LV574A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_W$	Pulse duration	CLK high or low	5	5	5	5	ns	
$t_{SU}$	Setup time	High or low before CLK↑	3.5	3.5	3.5	3.5	ns	
$t_H$	Hold time	Data after CLK↑	1.5	1.5	1.5	1.5	ns	

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER		$T_A = 25^\circ\text{C}$		SN54LV574A		SN74LV574A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_W$	Pulse duration	CLK high or low	5	5	5	5	ns	
$t_{SU}$	Setup time	High or low before CLK↑	3.5	3.5	3.5	3.5	ns	
$t_H$	Hold time	Data after CLK↑	1.5	1.5	1.5	1.5	ns	

**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			UNIT	
				MIN	TYP	MAX		
$f_{max}$			$C_L = 15 \text{ pF}$	60*	100*		50*	MHz
			$C_L = 50 \text{ pF}$	50	85		40	
$t_{pd}$	CLK	Q	$C_L = 15 \text{ pF}$	9.6*	16.6*	1* 20*	1 20	ns
$t_{en}$	$\overline{OE}$	Q		9.2*	16.1*	1* 19*	1 19	
$t_{dis}$	$\overline{OE}$	Q		6.5*	12.8*	1* 15*	1 15	
$t_{pd}$	CLK	Q	$C_L = 50 \text{ pF}$	11.6	19.6	1 23	1 23	ns
$t_{en}$	$\overline{OE}$	Q		10.9	19	1 22	1 22	
$t_{dis}$	$\overline{OE}$	Q		8.4	17.5	1 20	1 20	
$t_{sk(o)}$					2		2	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV574A	SN74LV574A	UNIT
				MIN	TYP	MAX	MIN	MAX	
$f_{max}$			$C_L = 15 \text{ pF}$	80*	145*		65*	65	MHz
			$C_L = 50 \text{ pF}$	50	120		45	45	
$t_{pd}$	CLK	Q	$C_L = 15 \text{ pF}$		6.8*	13.2*	1*	15.5*	1 15.5
$t_{en}$	$\overline{OE}$	Q			6.4*	12.8*	1*	15*	1 15
$t_{dis}$	$\overline{OE}$	Q			4.8*	13*	1*	15*	1 15
$t_{pd}$	CLK	Q	$C_L = 50 \text{ pF}$		8.1	16.7	1	19	1 19
$t_{en}$	$\overline{OE}$	Q			7.7	16.3	1	18.5	1 18.5
$t_{dis}$	$\overline{OE}$	Q			6.1	15	1	17	1 17
$t_{sk(o)}$						1.5			1.5

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV574A	SN74LV574A	UNIT
				MIN	TYP	MAX	MIN	MAX	
$f_{max}$			$C_L = 15 \text{ pF}$	130*	205*		110*	110	MHz
			$C_L = 50 \text{ pF}$	85	175		75	75	
$t_{pd}$	CLK	Q	$C_L = 15 \text{ pF}$		4.8*	8.6*	1*	10*	1 10
$t_{en}$	$\overline{OE}$	Q			4.6*	9*	1*	10.5*	1 10.5
$t_{dis}$	$\overline{OE}$	Q			3.5*	9*	1*	10.5*	1 10.5
$t_{pd}$	CLK	Q	$C_L = 50 \text{ pF}$		5.7	10.6	1	12	1 12
$t_{en}$	$\overline{OE}$	Q			5.5	11	1	12.5	1 12.5
$t_{dis}$	$\overline{OE}$	Q			4.1	10.1	1	11.5	1 11.5
$t_{sk(o)}$						1			1

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**noise characteristics,  $V_{CC} = 3.3 \text{ V}$ ,  $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 6)**

PARAMETER	SN74LV574A			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic $V_{OL}$		0.7	0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic $V_{OL}$		-0.6	-0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$		2.8		V
$V_{IH(D)}$ High-level dynamic input voltage		2.31		V
$V_{IL(D)}$ Low-level dynamic input voltage		0.99		V

NOTE 6: Characteristics are for surface-mount packages only.

**operating characteristics,  $T_A = 25^\circ\text{C}$**

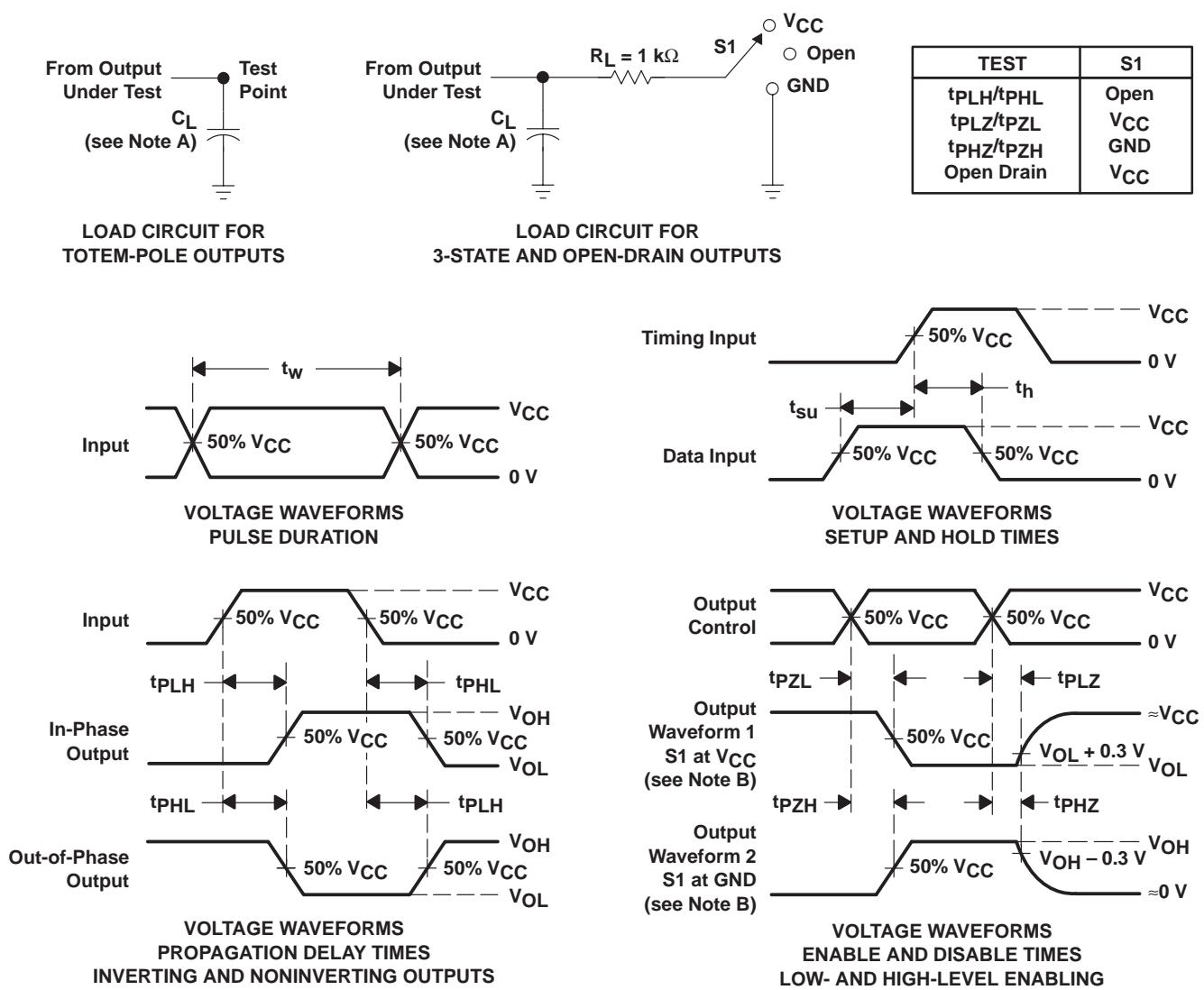
PARAMETER	TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	Outputs enabled	$C_L = 50 \text{ pF}$ , $f = 10 \text{ MHz}$	3.3 V	20.4
			5 V	23.8 pF

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## PARAMETER MEASUREMENT INFORMATION

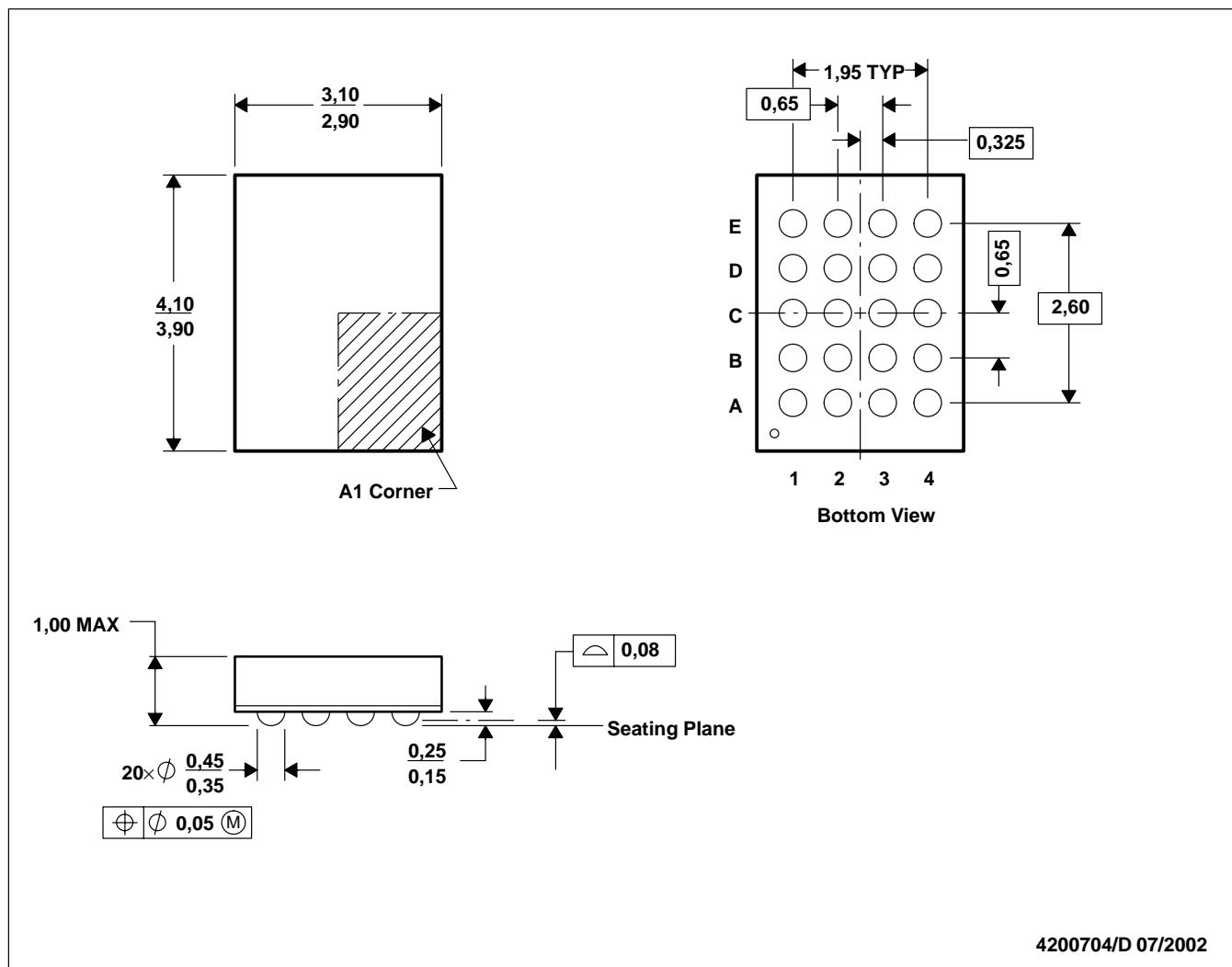


- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

## GQN (R-PBGA-N20)

## PLASTIC BALL GRID ARRAY



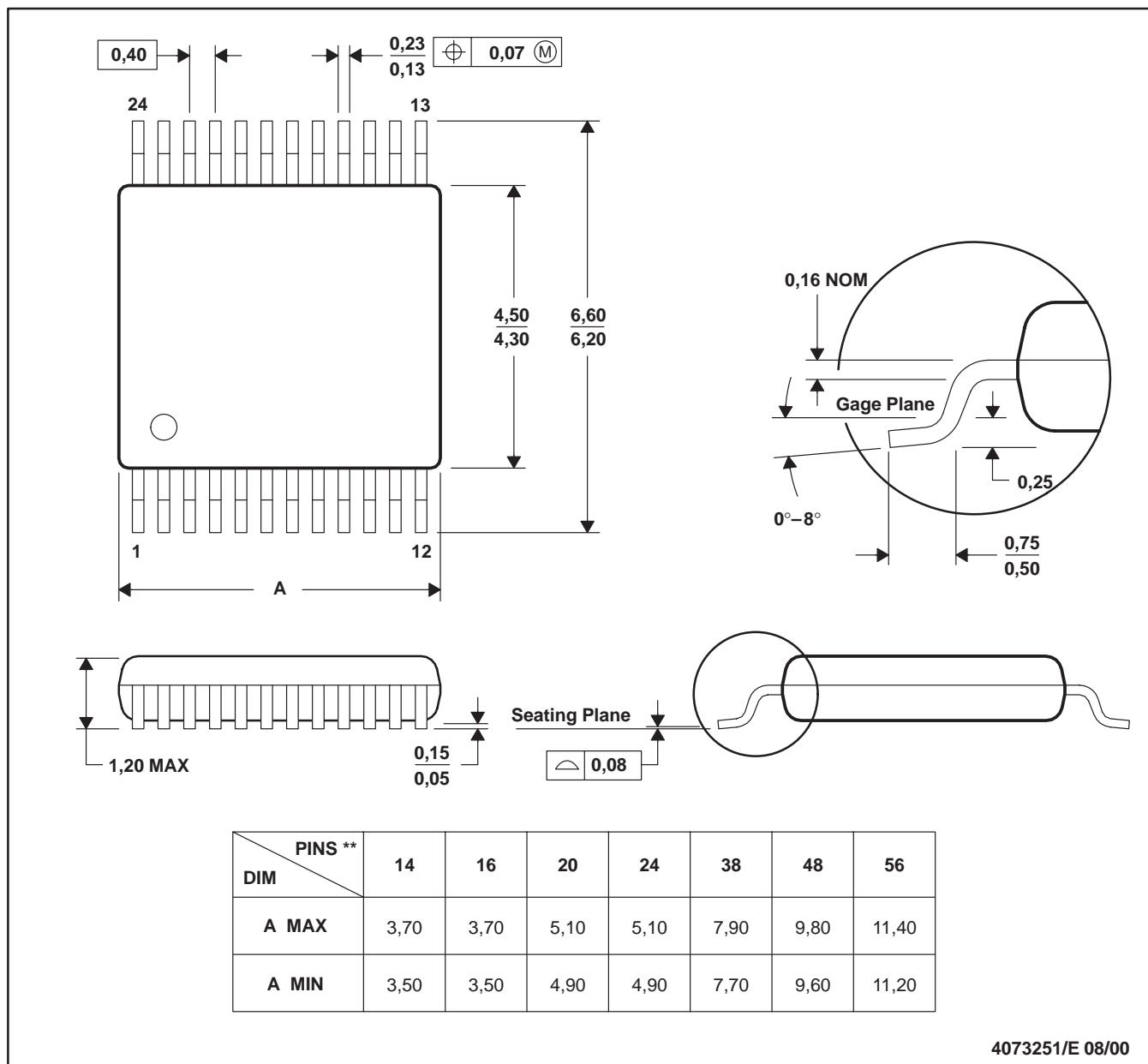
- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - MicroStar Junior™ configuration
  - Falls within JEDEC MO-225 variation BC.
  - This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

MicroStar Junior is a trademark of Texas Instruments.

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN

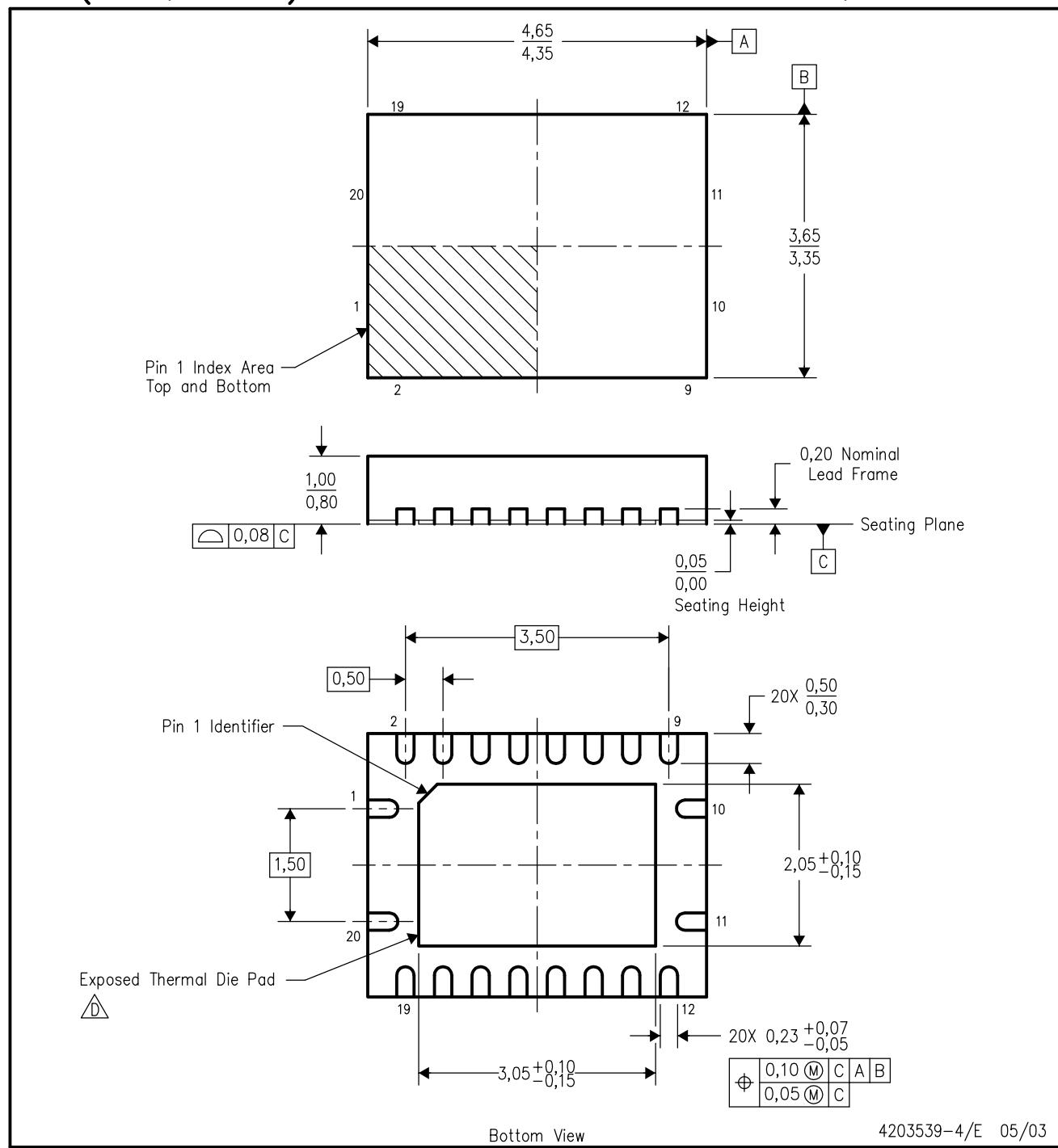


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
  - D. Falls within JEDEC: 24/48 Pins – MO-153  
14/16/20/56 Pins – MO-194

## MECHANICAL DATA

**RGY (R-PQFP-N20)**

**PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. QFN (Quad Flatpack No-Lead) package configuration.

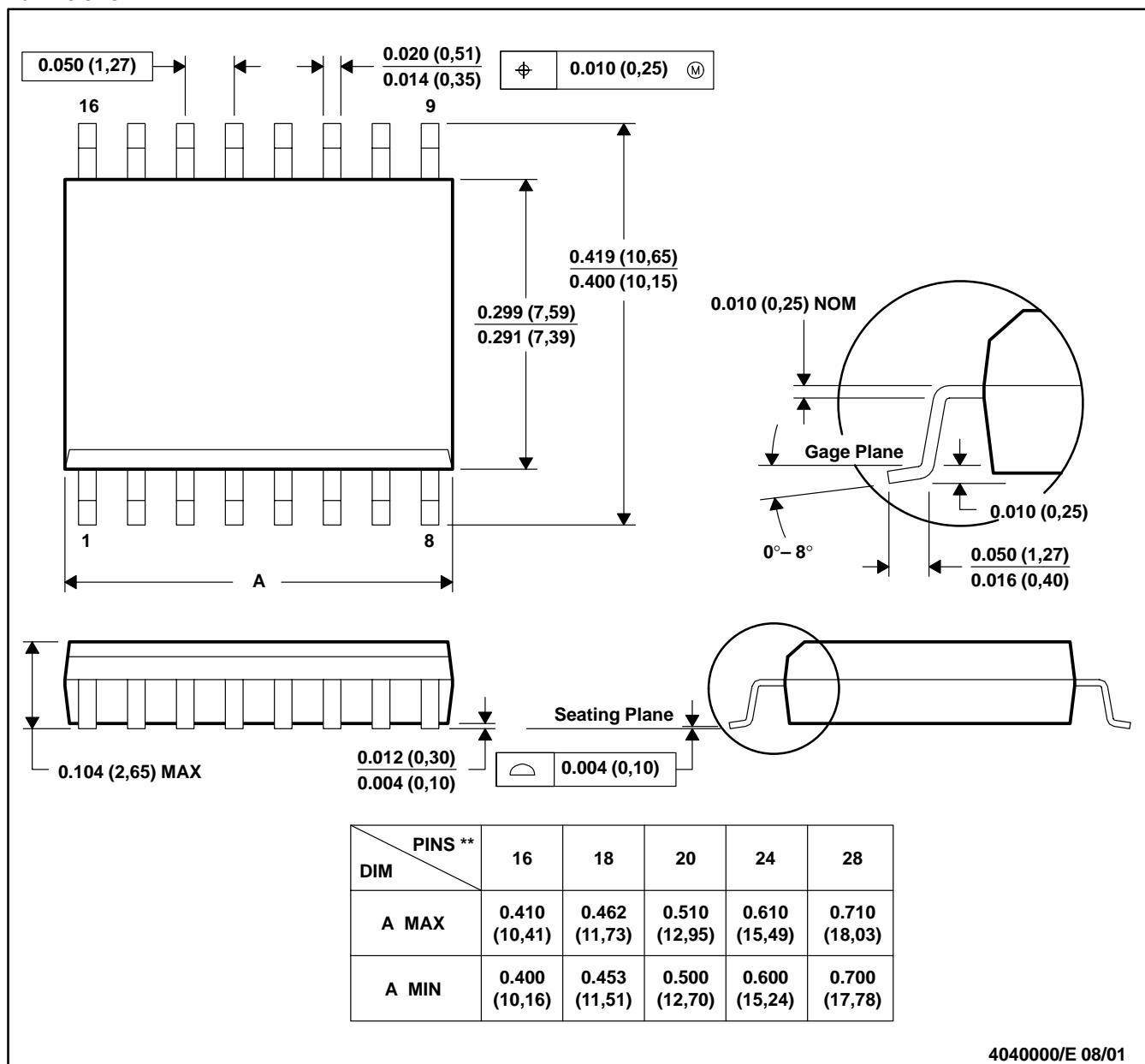
D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.

E. Package complies to JEDEC MO-241 variation BC.

## DW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



404000/E 08/01

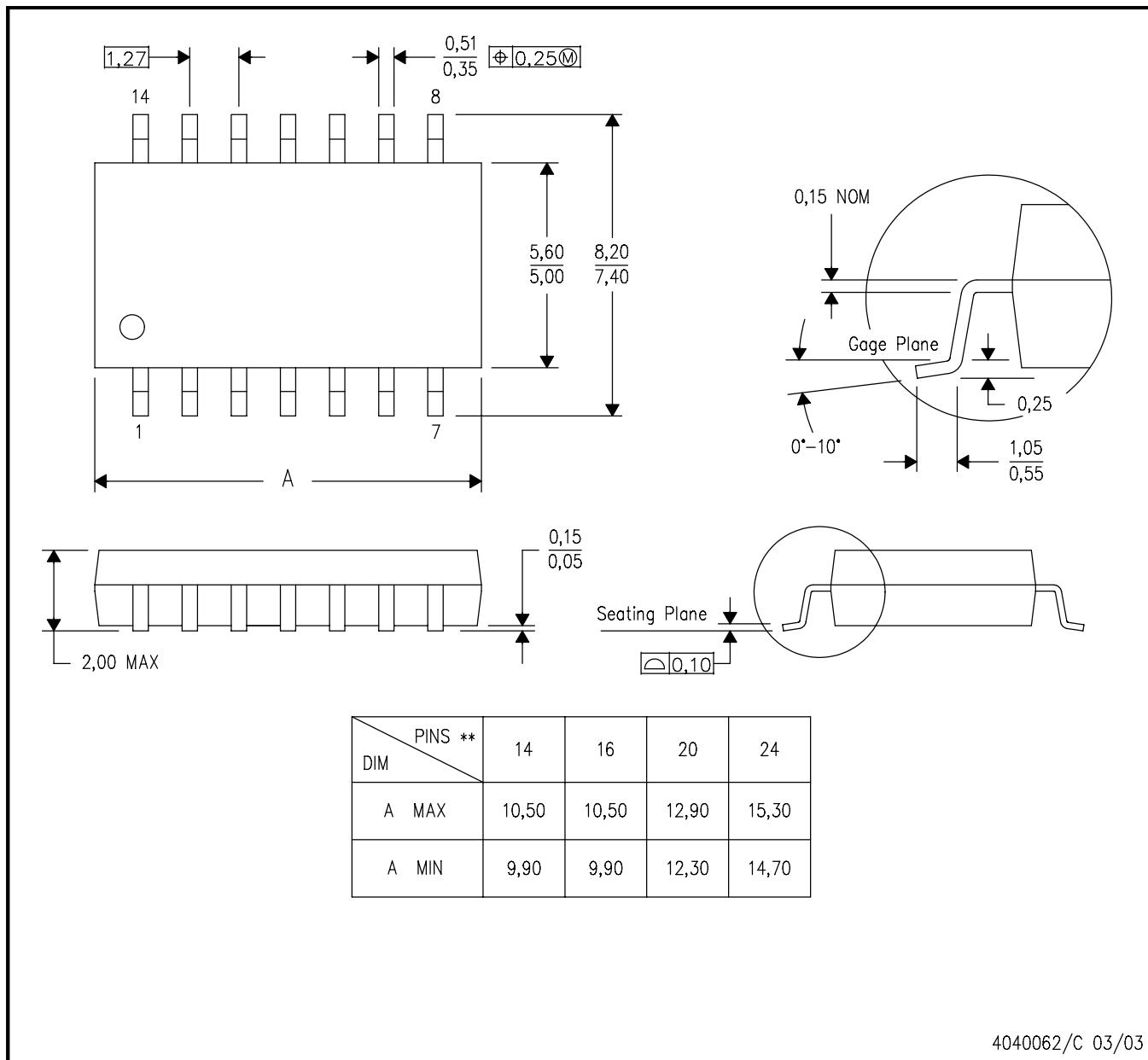
- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).  
 D. Falls within JEDEC MS-013

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**14-PINS SHOWN**

**PLASTIC SMALL-OUTLINE PACKAGE**



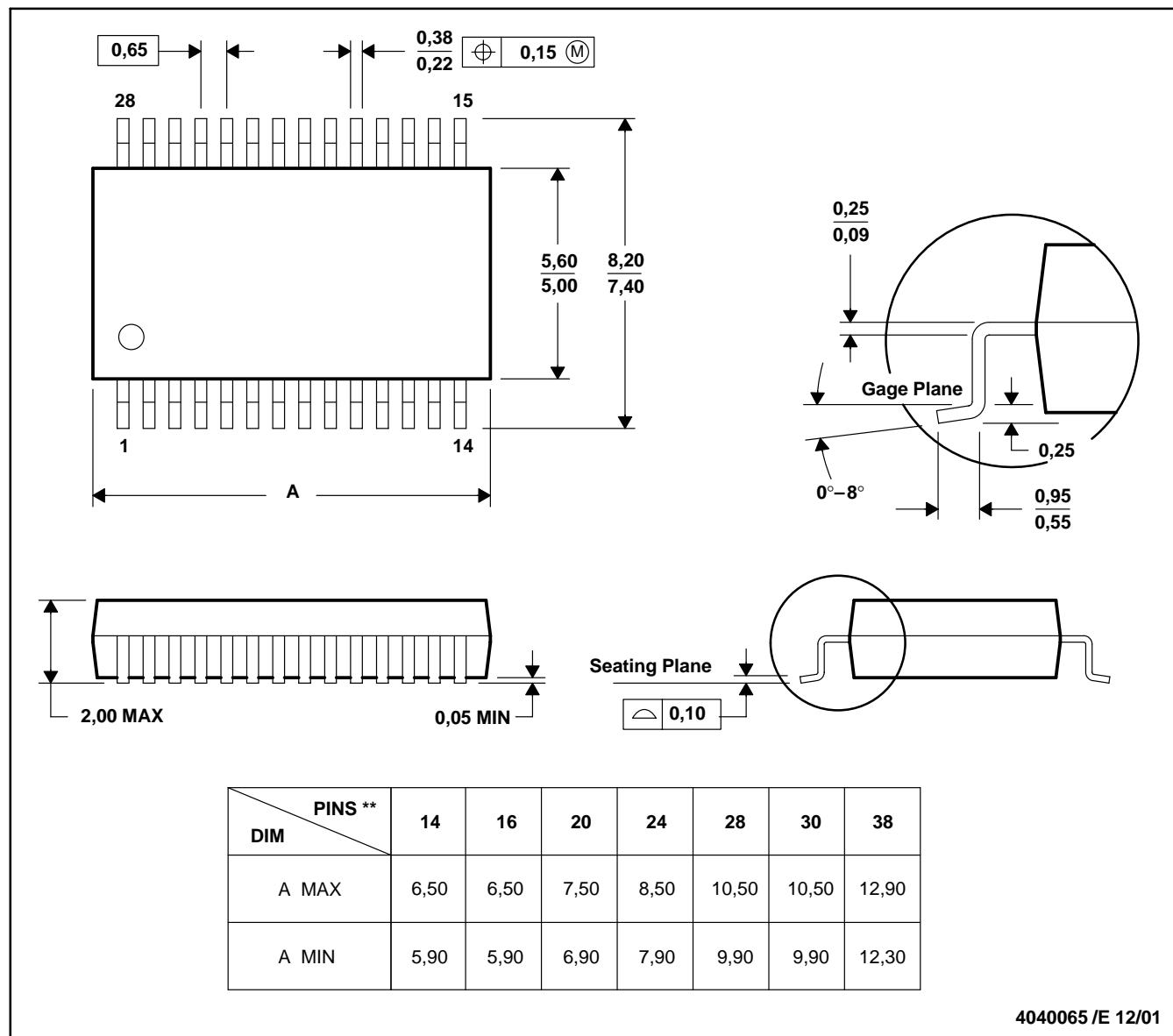
- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

4040062/C 03/03

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN

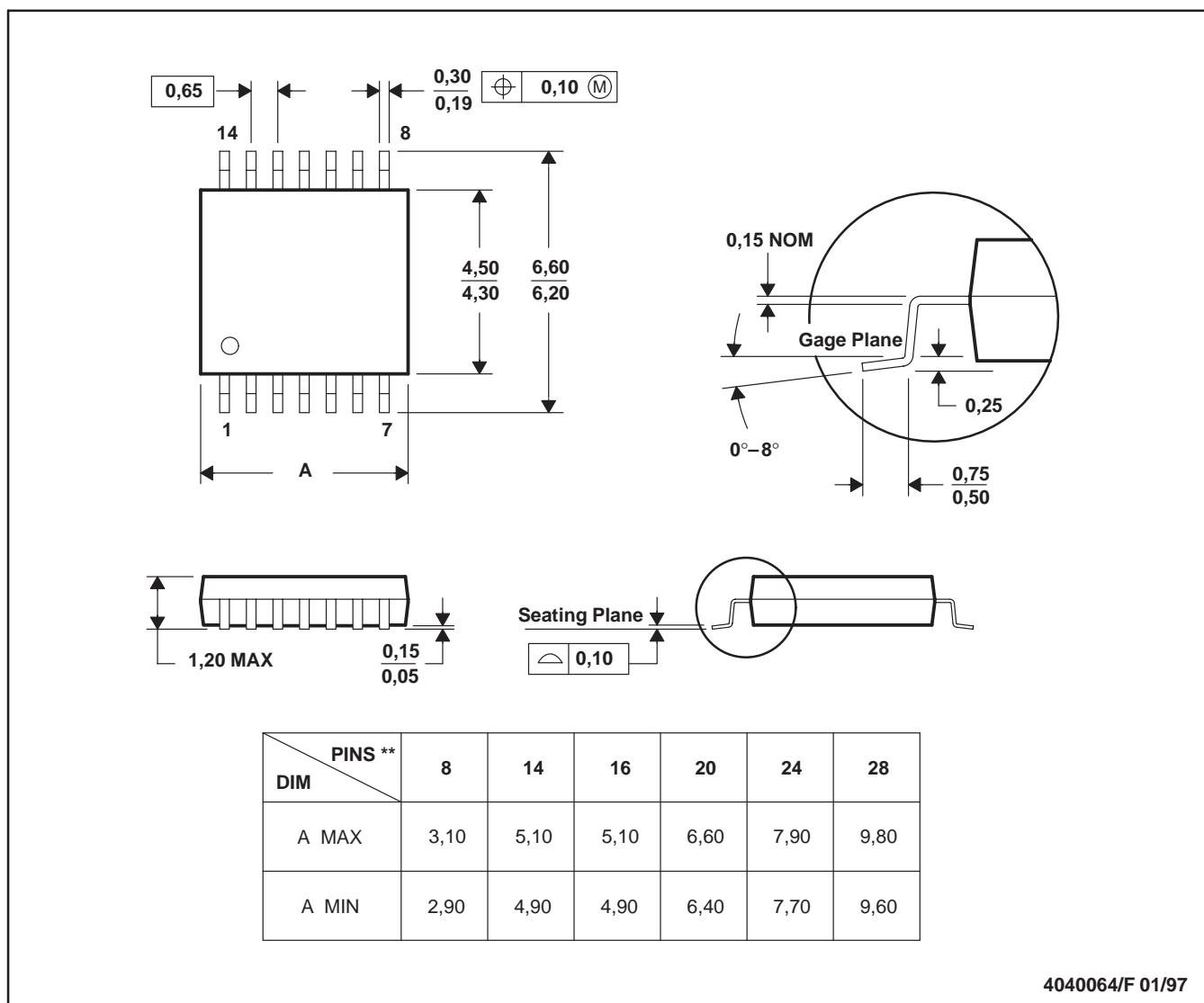


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - D. Falls within JEDEC MO-150

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - Falls within JEDEC MO-153

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Mailing Address:    Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265

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