- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 6.5 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})

- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
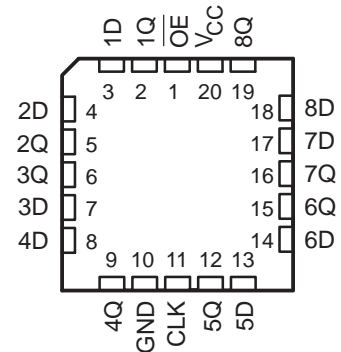 - 1000-V Charged-Device Model (C101)

SN54LVC374A . . . J OR W PACKAGE
SN74LVC374A . . . DB, DGV, DW, N, NS, OR PW PACKAGE
(TOP VIEW)

Pin			Pin
$\overline{OE}$	1	20	V_{CC}
1Q	2	19	8Q
1D	3	18	8D
2D	4	17	7D
2Q	5	16	7Q
3Q	6	15	6Q
3D	7	14	6D
4D	8	13	5D
4Q	9	12	5Q
GND	10	11	CLK
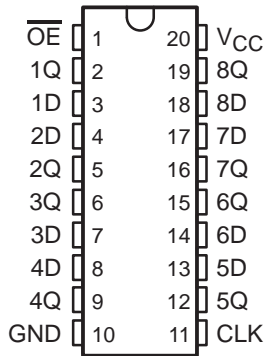
SN74LVC374A . . . RGY PACKAGE
(TOP VIEW)

		$\overline{OE}$ 1	V_{CC} 20		
1Q	2			19	8Q
1D	3			18	8D
2D	4			17	7D
2Q	5			16	7Q
3Q	6			15	6Q
3D	7			14	6D
4D	8			13	5D
4Q	9			12	5Q
		GND 10	CLK 11		
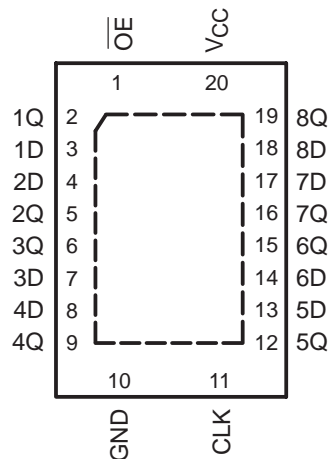
SN54LVC374A . . . FK PACKAGE
(TOP VIEW)

Top pins: 1D(3) 1Q(2) $\overline{OE}$(1) V_{CC}(20) 8Q(19)

2D	4		18	8D
2Q	5		17	7D
3Q	6		16	7Q
3D	7		15	6Q
4D	8		14	6D

Bottom pins: 4Q(9) GND(10) CLK(11) 5Q(12) 5D(13)

description/ordering information

The SN54LVC374A octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC374A octal edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, input/output (I/O) ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

description/ordering information (continued)

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 20	SN74LVC374AN	SN74LVC374AN
	QFN – RGY	Reel of 1000	SN74LVC374ARGYR	LC374A
	SOIC – DW	Tube of 25	SN74LVC374ADW	LVC374A
		Reel of 2000	SN74LVC374ADWR	
	SOP – NS	Reel of 2000	SN74LVC374ANSR	LVC374A
	SSOP – DB	Reel of 2000	SN74LVC374ADBR	LC374A
	TSSOP – PW	Tube of 70	SN74LVC374APW	LC374A
		Reel of 2000	SN74LVC374APWR	
		Reel of 250	SN74LVC374APWT	
	TVSOP – DGV	Reel of 2000	SN74LVC374ADGVR	LC374A
–55°C to 125°C	CDIP – J	Tube of 20	SNJ54LVC374AJ	SNJ54LVC374AJ
	CFP – W	Tube of 85	SNJ54LVC374AW	SNJ54LVC374AW
	LCCC – FK	Tube of 55	SNJ54LVC374AFK	SNJ54LVC374AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic diagram (positive logic)
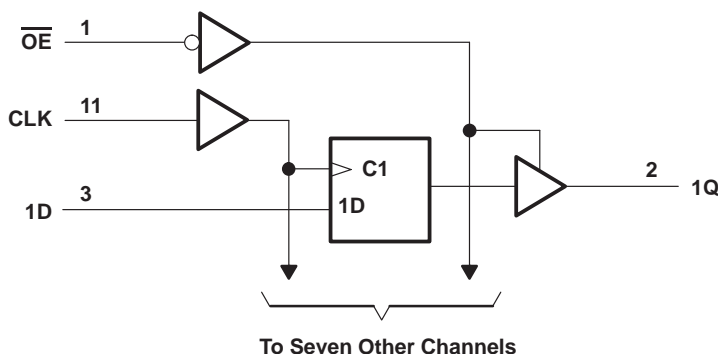
To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 6.5 V

Input voltage range, V_I (see Note 1) . . . . −0.5 V to 6.5 V

Voltage range applied to any output in the high-impedance or power-off state, V_O
   (see Note 1) . . . . −0.5 V to 6.5 V

Voltage range applied to any output in the high or low state, V_O
   (see Notes 1 and 2) . . . . −0.5 V to V_{CC} + 0.5 V

Input clamp current, I_{IK} (V_I < 0) . . . . −50 mA

Output clamp current, I_{OK} (V_O < 0) . . . . −50 mA

Continuous output current, I_O . . . . ±50 mA

Continuous current through V_{CC} or GND . . . . ±100 mA

Package thermal impedance, θ_{JA} (see Note 3): DB package . . . . 70°C/W
                                                  (see Note 3): DGV package . . . . 92°C/W
                                                  (see Note 3): DW package . . . . 58°C/W
                                                  (see Note 3): N package . . . . 69°C/W
                                                  (see Note 3): NS package . . . . 60°C/W
                                                  (see Note 3): PW package . . . . 83°C/W
                                                  (see Note 4): RGY package . . . . 37°C/W

Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
            2. The value of V_{CC} is provided in the recommended operating conditions table.
            3. The package thermal impedance is calculated in accordance with JESD 51-7.
            4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

			SN54LVC374A		SN74LVC374A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V			$0.65 \times V_{CC}$		V
		V_{CC} = 2.3 V to 2.7 V			1.7		
		V_{CC} = 2.7 V to 3.6 V	2		2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V				$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V				0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8		0.8	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
		3-state	0	5.5	0	5.5	
I_{OH}	High-level output current	V_{CC} = 1.65 V				−4	mA
		V_{CC} = 2.3 V				−8	
		V_{CC} = 2.7 V		−12		−12	
		V_{CC} = 3 V		−24		−24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V				4	mA
		V_{CC} = 2.3 V				8	
		V_{CC} = 2.7 V		12		12	
		V_{CC} = 3 V		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	SN54LVC374A			SN74LVC374A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	$I_{OH} = -100\ \mu A$		1.65 V to 3.6 V				$V_{CC}-0.2$			V
			2.7 V to 3.6 V	$V_{CC}-0.2$						
	$I_{OH} = -4\ mA$		1.65 V				1.2			
	$I_{OH} = -8\ mA$		2.3 V				1.7			
	$I_{OH} = -12\ mA$		2.7 V	2.2			2.2			
			3 V	2.4			2.4			
	$I_{OH} = -24\ mA$		3 V	2.2			2.2			
V_{OL}	$I_{OL} = 100\ \mu A$		1.65 V to 3.6 V						0.2	V
			2.7 V to 3.6 V			0.2				
	$I_{OL} = 4\ mA$		1.65 V						0.45	
	$I_{OL} = 8\ mA$		2.3 V						0.7	
	$I_{OL} = 12\ mA$		2.7 V			0.4			0.4	
	$I_{OL} = 24\ mA$		3 V			0.55			0.55	
I_I	$V_I = 0$ to 5.5 V		3.6 V			±5			±5	μA
I_{off}	V_I or $V_O = 5.5$ V		0						±10	μA
I_{OZ}	$V_O = 0$ to 5.5 V		3.6 V			±15			±10	μA
I_{CC}	$V_I = V_{CC}$ or GND	$I_O = 0$	3.6 V			10			10	μA
	$3.6\ V \le V_I \le 5.5\ V$‡					10			10	
ΔI_{CC}	One input at $V_{CC} - 0.6$ V, Other inputs at V_{CC} or GND		2.7 V to 3.6 V			500			500	μA
C_i	$V_I = V_{CC}$ or GND		3.3 V		4	12		4		pF
C_o	$V_O = V_{CC}$ or GND		3.3 V		5.5	12		5.5		pF

† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25°C$.
‡ This applies in the disabled state only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVC374A				UNIT
		$V_{CC} = 2.7$ V		$V_{CC} = 3.3$ V ± 0.3 V		
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		80		100	MHz
t_w	Pulse duration, CLK high or low	3.3		3.3		ns
t_{su}	Setup time, data before CLK↑	2		2		ns
t_h	Hold time, data after CLK↑	1.5		1.5		ns

SN54LVC374A, SN74LVC374A
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS

SCAS296N – JANUARY 1993 – REVISED AUGUST 2003

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN74LVC374A								UNIT
		V_{CC} = 1.8 V $\pm$ 0.15 V		V_{CC} = 2.5 V $\pm$ 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V $\pm$ 0.3 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		†		†		80		100	MHz
t_w	Pulse duration, CLK high or low	†		†		3.3		3.3		ns
t_{su}	Setup time, data before CLK↑	†		†		2		2		ns
t_h	Hold time, data after CLK↑	†		†		1.5		1.5		ns

† This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC374A				UNIT
			V_{CC} = 2.7 V		V_{CC} = 3.3 V $\pm$ 0.3 V		
			MIN	MAX	MIN	MAX	
f_{max}			80		100		MHz
t_{pd}	CLK	Q		9.5	1	8.5	ns
t_{en}	$\overline{OE}$	Q		9.5	1	8.5	ns
t_{dis}	$\overline{OE}$	Q		8	1	7	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC374A								UNIT
			V_{CC} = 1.8 V $\pm$ 0.15 V		V_{CC} = 2.5 V $\pm$ 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V $\pm$ 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			†		†		80		100		MHz
t_{pd}	CLK	Q	†	†	†	†		8.1	1.5	7	ns
t_{en}	$\overline{OE}$	Q	†	†	†	†		8.5	1.5	7.5	ns
t_{dis}	$\overline{OE}$	Q	†	†	†	†		7.1	1.5	6.5	ns
$t_{sk(o)}$										1	ns

† This information was not available at the time of publication.

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
			TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	†	†	54.5	pF
		Outputs disabled	†	†	13.5	

† This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION
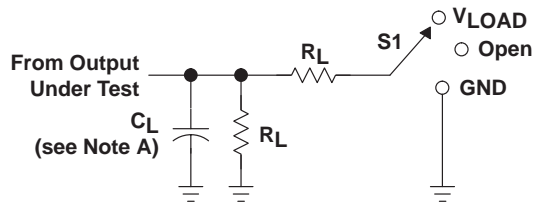
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V $\pm$ 0.15 V	V_{CC}	$\leq$2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V $\pm$ 0.2 V	V_{CC}	$\leq$2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq$2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V $\pm$ 0.3 V	2.7 V	$\leq$2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
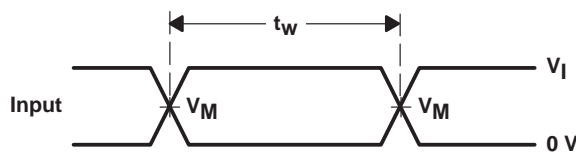
VOLTAGE WAVEFORMS
PULSE DURATION
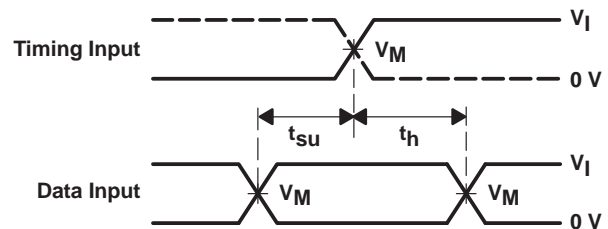
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
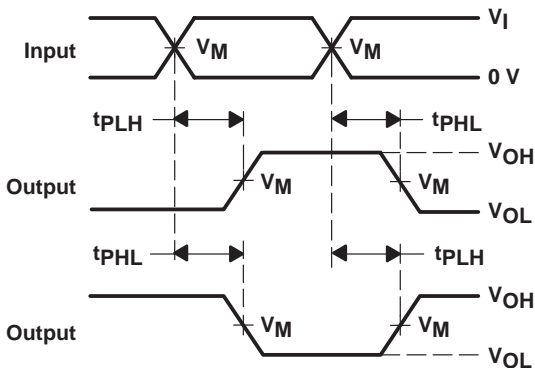
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS
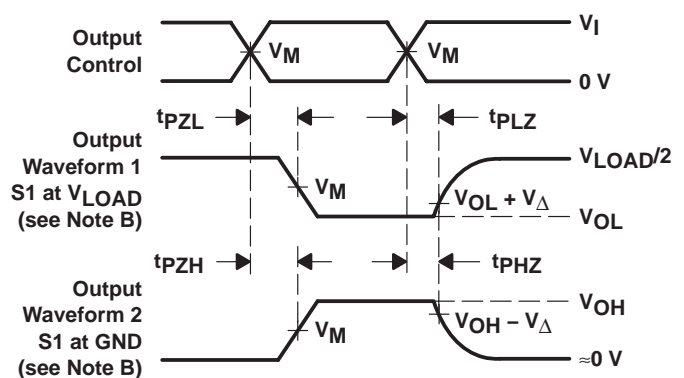
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°−15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
B.   This drawing is subject to change without notice.
C.   This package is hermetically sealed with a ceramic lid using glass frit.
D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E.   Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

W (R-GDFP-F20)   **CERAMIC DUAL FLATPACK**

0.300 (7,62) / 0.245 (6,22)

Base and Seating Plane

0.045 (1,14) / 0.026 (0,66)

0.100 (2,54) / 0.045 (1,14)

0.009 (0,23) / 0.004 (0,10)

0.320 (8,13) MAX

0.022 (0,56) / 0.015 (0,38)

0.540 (13,72) MAX

0.050 (1,27)

0.005 (0,13) MIN 4 Places

0.370 (9,40) / 0.250 (6,35)

4040180-4/D 07/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil-Std 1835 GDFP2-F20

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

FK (S-CQCC-N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

0.020 (0,51) / 0.010 (0,25)

0.020 (0,51) / 0.010 (0,25)

0.080 (2,03) / 0.064 (1,63)

0.055 (1,40) / 0.045 (1,14)

0.045 (1,14) / 0.035 (0,89)

0.028 (0,71) / 0.022 (0,54)
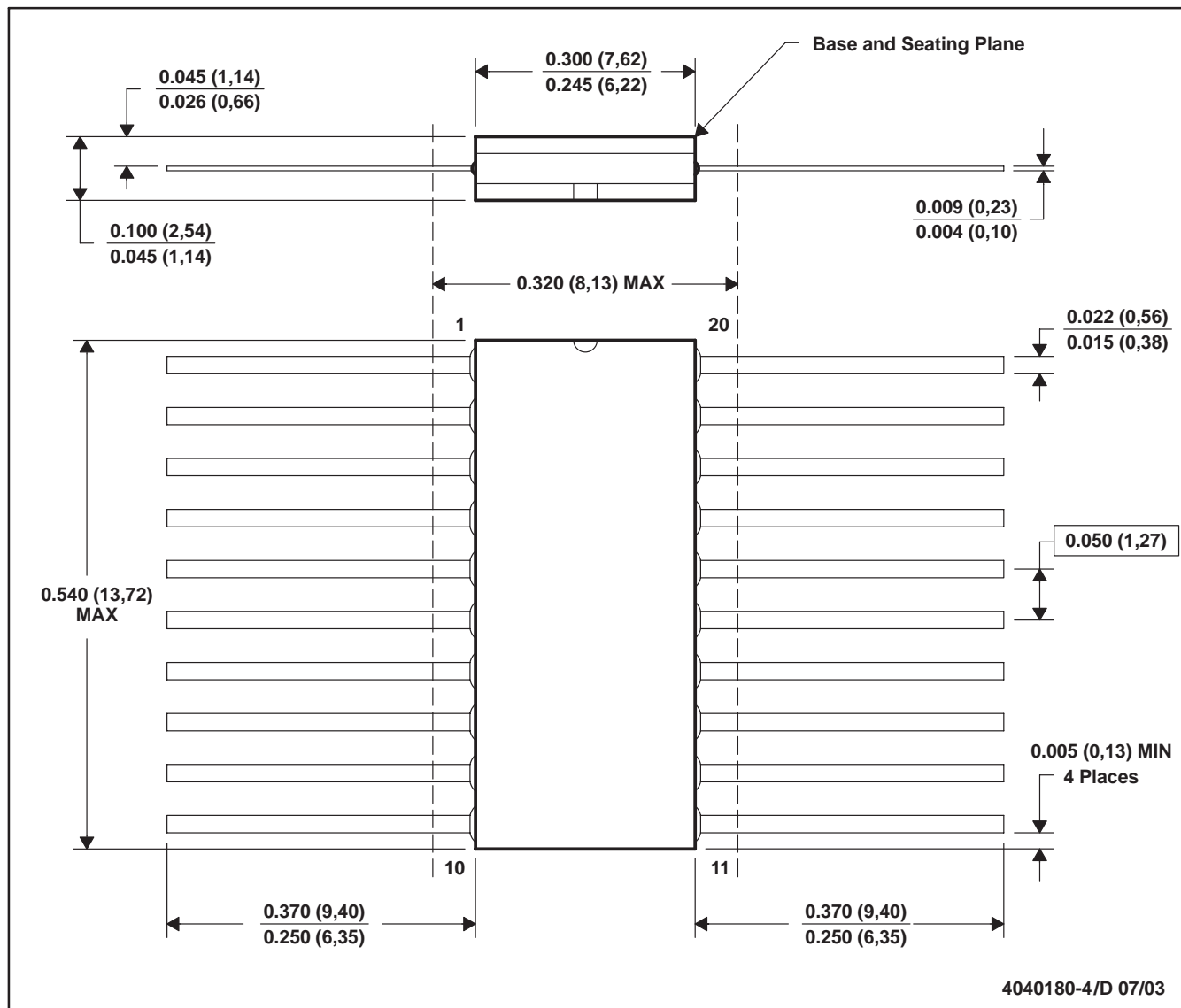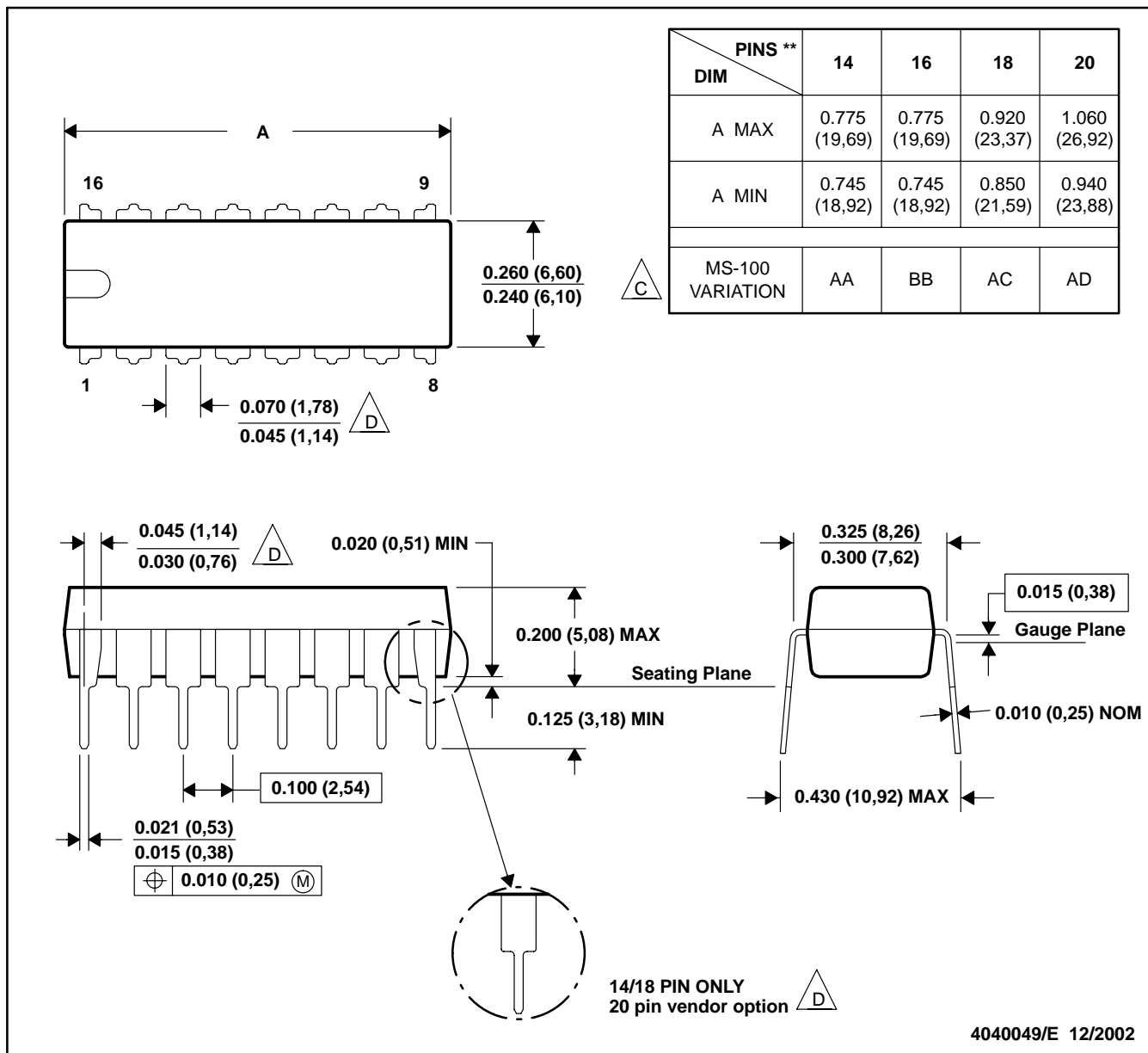
0.045 (1,14) / 0.035 (0,89)

0.050 (1,27)

4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

MECHANICAL

N (R-PDIP-T**)   **PLASTIC DUAL-IN-LINE PACKAGE**

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-100 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60) / 0.240 (6,10)

1   8

0.070 (1,78) / 0.045 (1,14) D

0.045 (1,14) / 0.030 (0,76) D

0.020 (0,51) MIN

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.010 (0,25) NOM

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

$\oplus$ 0.010 (0,25) (M)

0.430 (10,92) MAX

14/18 PIN ONLY
 20 pin vendor option D

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).

        B. This drawing is subject to change without notice.

    C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body lrngth (Dim A).

    D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

DGV (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

0,40

0,23
0,13   ⊕   0,07 Ⓜ

24   13

4,50
4,30

6,60
6,20

1   12

A

0,16 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌒ 0,08

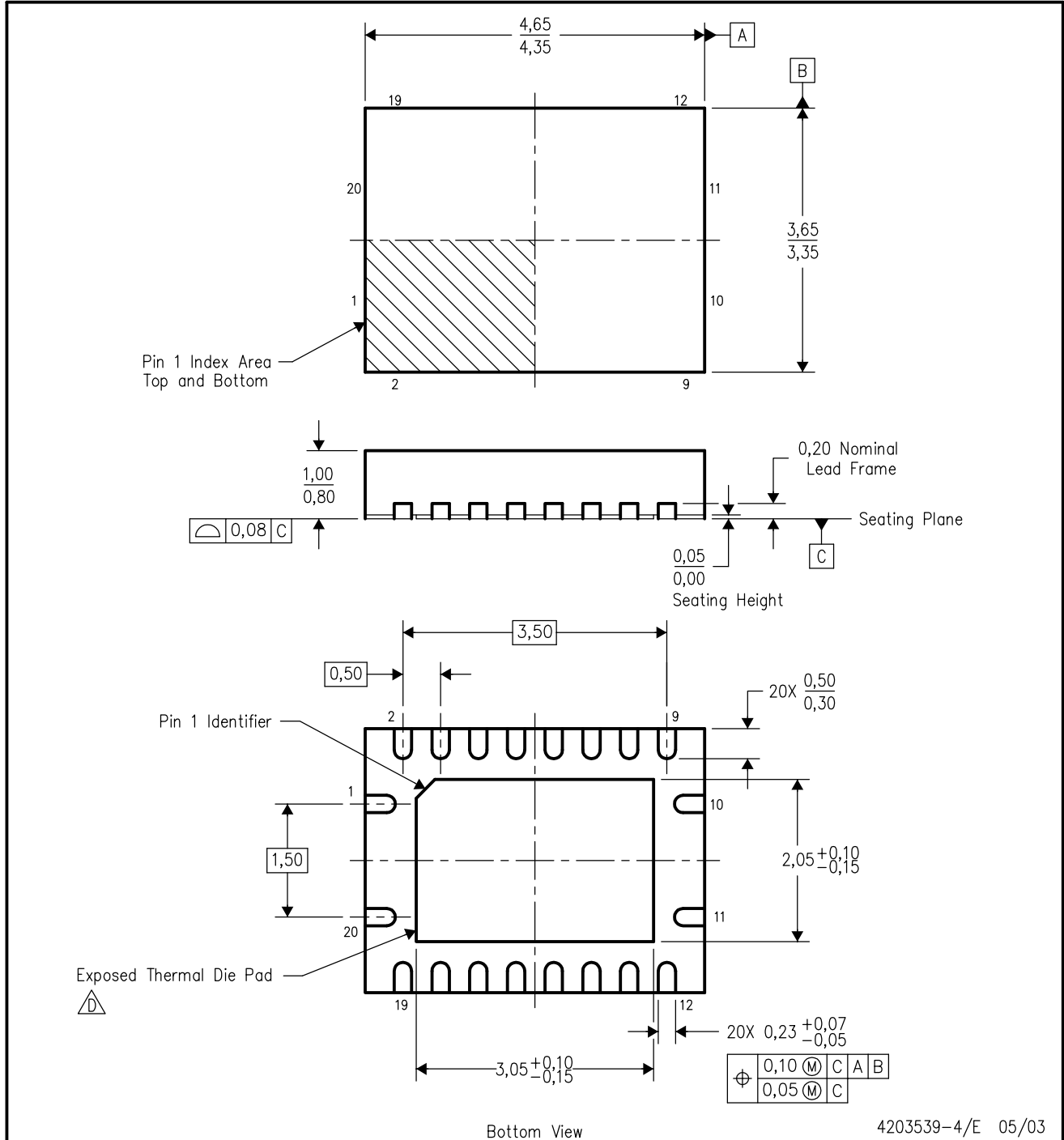| PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
         D. Falls within JEDEC: 24/48 Pins – MO-153
                            14/16/20/56 Pins – MO-194

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RGY (R–PQFP–N20)   **PLASTIC QUAD FLATPACK**

Bottom View

4203539–4/E 05/03
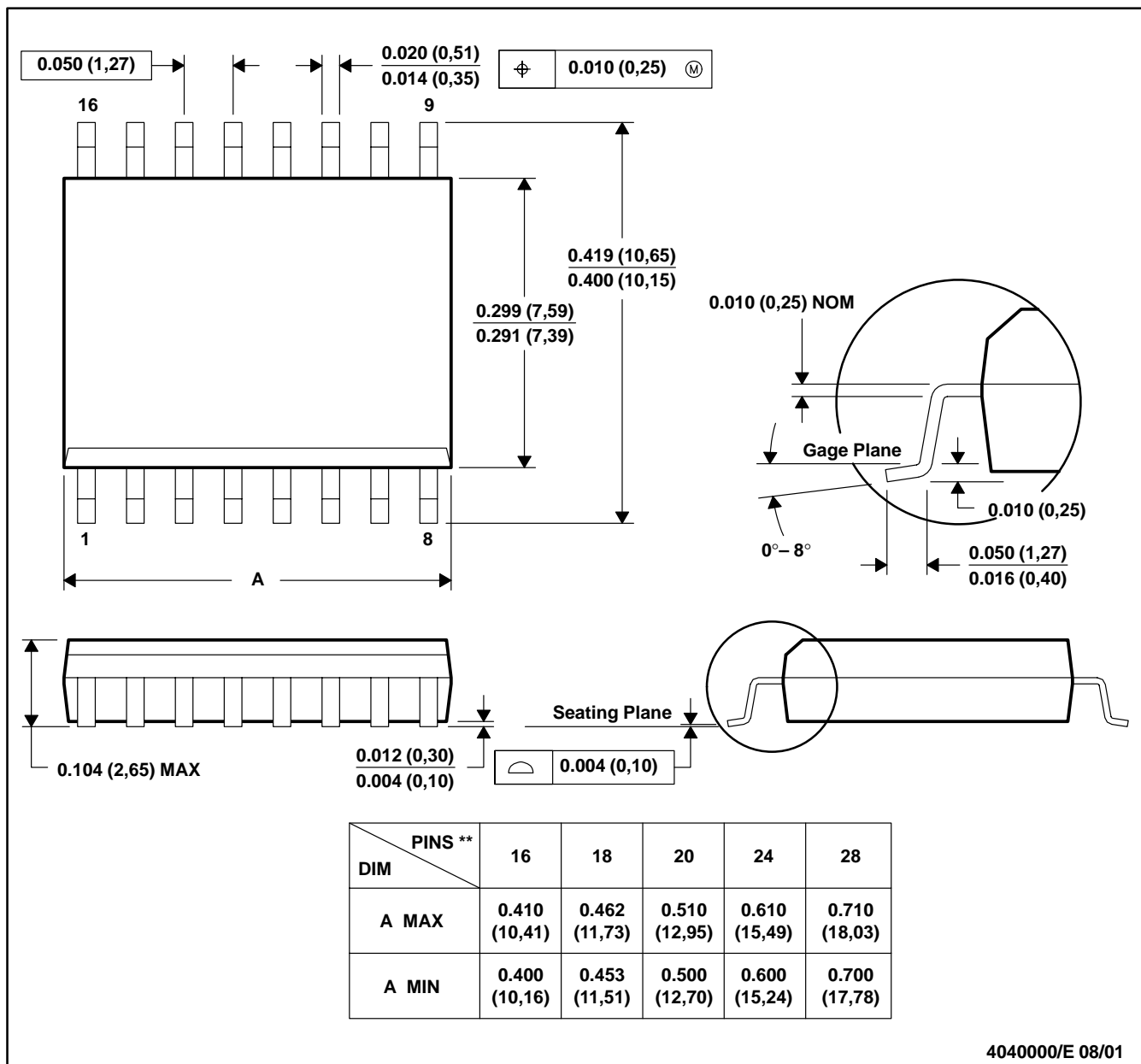
NOTES: A. All linear dimensions are in millimeters.
           B. This drawing is subject to change without notice.
           C. QFN (Quad Flatpack No–Lead) package configuration.

      ⚠D The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane.
            This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
           E. Package complies to JEDEC MO–241 variation BC.

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DW (R-PDSO-G)** PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN

PINS ** DIM	16	18	20	24	28
A MAX	0.410 (10,41)	0.462 (11,73)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.453 (11,51)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4040000/E 08/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

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MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
B.   This drawing is subject to change without notice.
C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)**   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

0,65

$\dfrac{0,38}{0,22}$ ⊕ 0,15 Ⓜ

28   15

$\dfrac{5,60}{5,00}$ $\dfrac{8,20}{7,40}$

1   14

A

$\dfrac{0,25}{0,09}$

Gage Plane

0,25

0°−8° $\dfrac{0,95}{0,55}$

2,00 MAX   0,05 MIN

Seating Plane

⌒ 0,10

DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
  B. This drawing is subject to change without notice.
  C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  D. Falls within JEDEC MO-150

PW (R-PDSO-G**) **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

	PINS **	8	14	16	20	24	28
DIM							
A MAX		3,10	5,10	5,10	6,60	7,90	9,80
A MIN		2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
        D. Falls within JEDEC MO-153

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