

SCAS619E-OCTOBER 1998-REVISED AUGUST 2007

FEATURES

- Member of the Texas Instruments Widebus+™
 Family
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.5 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C

- I_{off} Supports Partial-Power-Down Mode Operation
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input and Output Voltages With 3.3-V V_{CC})
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17

DESCRIPTION/ORDERING INFORMATION

This 32-bit edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVCH32374A is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as four 8-bit flip-flops, two 16-bit flip-flops, or one 32-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

OE does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
–40°C to 85°C	LFBGA – GKE		SN74LVCH32374AGKER	CH374A	
-40 C 10 65°C	LFBGA – ZKE (Pb-free)	Tape and reel	SN74LVCH32374AZKER	- CH3/4A	

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

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Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





GKE OR ZKE PACKAGE (TOP VIEW)

		1	2	3	4	5	6
Α	/	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\circ
В		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
С		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
D		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
Е		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
F		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
G		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
н		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
J		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
κ		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
L		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
М		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
N		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
Р		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
R		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
Т		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc

TERMINAL ASSIGNMENTS

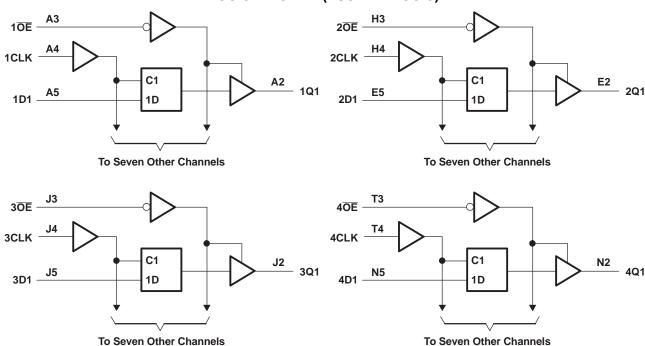
	1	2	3	4	5	6
Α	1Q2	1Q1	1 OE	1CLK	1D1	1D2
В	1Q4	1Q3	GND	GND	1D3	1D4
С	1Q6	1Q5	V_{CC}	V_{CC}	1D5	1D6
D	1Q8	1Q7	GND	GND	1D7	1D8
Е	2Q2	2Q1	GND	GND	2D1	2D2
F	2Q4	2Q3	V _{CC}	V _{CC}	2D3	2D4
G	2Q6	2Q5	GND	GND	2D5	2D6
Н	2Q7	2Q8	2 OE	2CLK	2D8	2D7
J	3Q2	3Q1	3 OE	3CLK	3D1	3D2
K	3Q4	3Q3	GND	GND	3D3	3D4
L	3Q6	3Q5	V _{CC}	V _{CC}	3D5	3D6
M	3Q8	3Q7	GND	GND	3D7	3D8
N	4Q2	4Q1	GND	GND	4D1	4D2
Р	4Q4	4Q3	V _{CC}	V _{CC}	4D3	4D4
R	4Q6	4Q5	GND	GND	4D5	4D6
T	4Q7	4Q8	4 OE	4CLK	4D8	4D7

FUNCTION TABLE (EACH FLIP-FLOP)

	INPUTS	OUTPUT	
ŌĒ	CLK	D	Q
L	1	Н	Н
L	↑	L	L
L	H or L	Χ	Q_0
Н	Χ	Χ	Z



LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	6.5	V
VI	Input voltage range ⁽²⁾		-0.5	6.5	V
Vo	Voltage range applied to any output in the h	nigh-impedance or power-off state (2)	-0.5	6.5	V
Vo	Voltage range applied to any output in the h	nigh or low state (2)(3)	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
l _{ok}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through each V _{CC} or GN	ND		±100	mA
θ_{JA}	Package thermal impedance (4)	GKE/ZKE package		40	°C/W
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The value of V_{CC} is provided in the recommended operating conditions table.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.

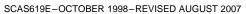




Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
17	Cumply voltage	Operating	1.65	3.6	V
V _{CC}	Supply voltage	Data retention only	1.5		V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
V_{IH}	High-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7		V
		V _{CC} = 2.7 V to 3.6 V	2		
		V _{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	
V _{IL} I	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
		V _{CC} = 2.7 V to 3.6 V		0.8	
VI	Input voltage	·	0	5.5	V
\/	Outrot valta sa	High or low state	0	V _{CC}	V
Vo	Output voltage	3-state	0	5.5	
		V _{CC} = 1.65 V		-4	
	High layed output ourrent	V _{CC} = 2.3 V		-8	mA
I _{OH}	High-level output current	V _{CC} = 2.7 V		-12	mA
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ 0 High or low state 0 3-state 0 $V_{CC} = 1.65 \text{ V}$ $V_{CC} = 2.3 \text{ V}$	-24		
		V _{CC} = 1.65 V		4	
	Lave lavel autout avenue	V _{CC} = 2.3 V		8	A
l _{OL}	Low-level output current	V _{CC} = 2.7 V	1		mA
		V _{CC} = 3 V			
Δt/Δν	Input transition rise or fall rate	·		10	ns/V
T _A	Operating free-air temperature		-40	85	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.





Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITI	IONS	V _{CC}	MIN TYP ⁽¹⁾	MAX	UNIT	
	I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} - 0.2			
	$I_{OH} = -4 \text{ mA}$		1.65 V	1.2			
V _{OH}	$I_{OH} = -8 \text{ mA}$		2.3 V	1.7		V	
V OH	l = 12 mΛ	I _{OH} = -12 mA				V	
	I _{OH} = -12 IIIA						
	$I_{OH} = -24 \text{ mA}$	3 V	2.2				
	I _{OL} = 100 μA		1.65 V to 3.6 V		0.2		
	I _{OL} = 4 mA	1.65 V		0.45			
V _{OL}	I _{OL} = 8 mA	2.3 V		0.7	V		
	I _{OL} = 12 mA	2.7 V		0.4			
	I _{OL} = 24 mA	3 V		0.55			
I _I	V _I = 0 to 5.5 V		3.6 V		±5	μA	
	V _I = 0.58 V	1 CE V	25				
	V _I = 1.07 V	1.65 V	-25				
	V _I = 0.7 V	2.3 V	45				
I _{I(hold)}	V _I = 1.7 V	2.3 V	-45		μΑ		
	V _I = 0.8 V	V _I = 0.8 V					
	V _I = 2 V		3 V	- 75			
	$V_I = 0$ to 3.6 $V^{(2)}$		3.6 V		±500		
l _{off}	V_I or $V_O = 5.5 \text{ V}$		0		±10	μΑ	
I _{OZ}	$V_{O} = 0 \text{ to } 5.5 \text{ V}$		3.6 V		±10	μΑ	
	V _I = V _{CC} or GND	0	261/		40		
I _{CC}	$3.6 \text{ V} \le \text{V}_{\text{I}} \le 5.5 \text{ V}^{(3)}$	U	3.6 V		40 µA		
ΔI _{CC}	One input at V _{CC} – 0.6 V, Othe	r inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μA	
C _i	$V_I = V_{CC}$ or GND		3.3 V	5		pF	
Co	$V_O = V_{CC}$ or GND		3.3 V	6.5		pF	

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V _{CC} = ± 0.1		V _{CC} = ± 0.2		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		(1)		(1)		150		150	MHz
t _w	Pulse duration, CLK high or low	(1)		(1)		3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	(1)		(1)		1.9		1.9		ns
t _h	Hold time, data after CLK↑	(1)		(1)		1.1		1.1		ns

⁽¹⁾ This information was not available at the time of publication.

All typical values are at V_{CC} = 3.3 V, T_A = 25°C. This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

This applies in the disabled state only.

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Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		2.7 V	V _{CC} = 3.3 V ± 0.3 V		UNIT
	(INPUT)	(0011-01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			(1)		(1)		150		150		MHz
t _{pd}	CLK	Q	(1)	(1)	(1)	(1)		4.9	1.5	4.5	ns
t _{en}	ŌĒ	Q	(1)	(1)	(1)	(1)		5.3	1.5	4.6	ns
t _{dis}	ŌĒ	Q	(1)	(1)	(1)	(1)		6.1	1.5	5.5	ns
t _{sk(o)}										1.5	ns

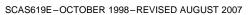
⁽¹⁾ This information was not available at the time of publication.

Operating Characteristics

 $T_A = 25^{\circ}C$

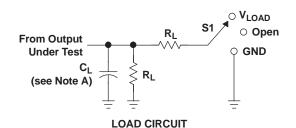
PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT		
_	Power dissipation capacitance Output		f = 10 MHz	(1)	(1)	58	pF	
C _{pd}	per flip-flop	Outputs disabled	I = IU MINZ	(1)	(1)	24	рF	

⁽¹⁾ This information was not available at the time of publication.



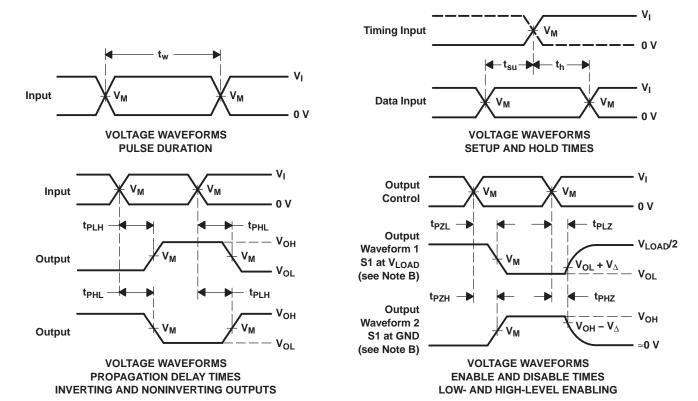


PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

V	INI	PUTS	V		_	Б	V
V _{CC}	V_{I}	t _r /t _f	V _M	V _{LOAD}	CL	R _L	V_Δ
1.8 V \pm 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V_{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V \pm 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_0 = 50 Ω .
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVCH32374AGKER	NRND	LFBGA	GKE	96	1000	TBD	SNPB	Level-2-235C-1 YEAR
SN74LVCH32374AZKER	ACTIVE	LFBGA	ZKE	96	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

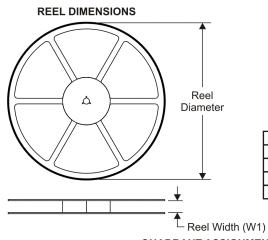
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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCH32374AGKER	LFBGA	GKE	96	1000	330.0	24.4	5.7	13.7	2.0	8.0	24.0	Q1
SN74LVCH32374AZKER	LFBGA	ZKE	96	1000	330.0	24.4	5.7	13.7	2.0	8.0	24.0	Q1

PACKAGE MATERIALS INFORMATION

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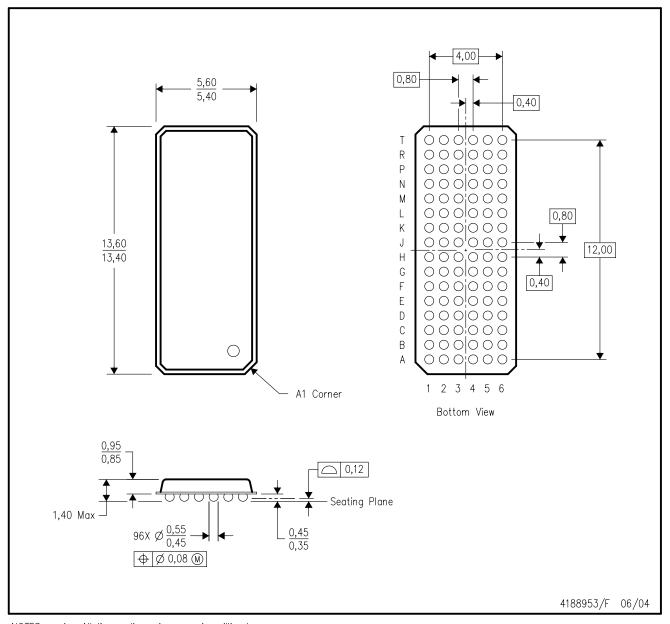


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCH32374AGKER	LFBGA	GKE	96	1000	333.2	345.9	31.8
SN74LVCH32374AZKER	LFBGA	ZKE	96	1000	333.2	345.9	31.8

GKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



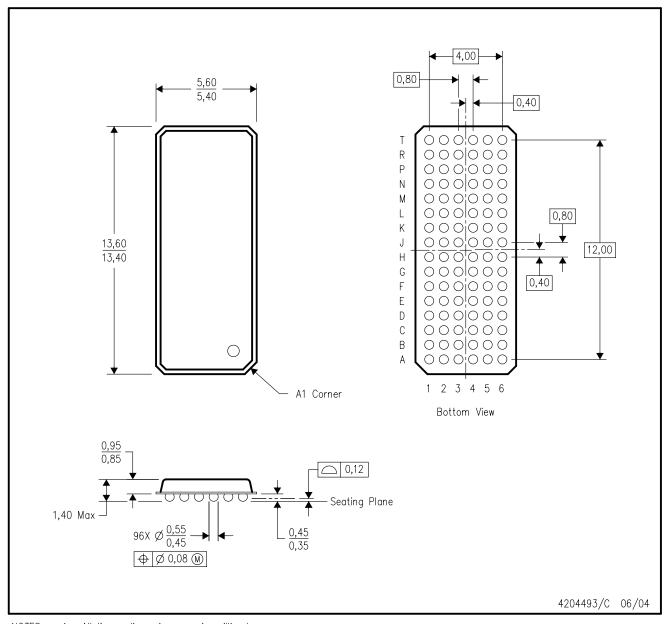
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-205 variation CC.
- D. This package is tin-lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead-free.



ZKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-205 variation CC.
- D. This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).



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