

# SN55173, SN65173, SN75173 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

SLLS144E – OCTOBER 1980 – REVISED APRIL 2000

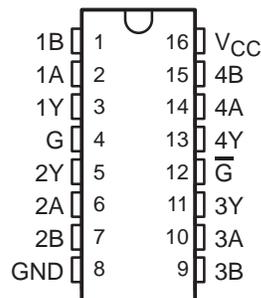
- Meet or Exceed the Requirements of TIA/EIA-422-B, TIA/EIA-423-B, and TIA/EIA-485-A and ITU Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Input Voltage Range of  $-12\text{ V}$  to  $12\text{ V}$
- Input Sensitivity . . .  $\pm 200\text{ mV}$
- Input Hysteresis . . .  $50\text{ mV Typ}$
- High Input Impedance . . .  $12\text{ k}\Omega\text{ Min}$
- Operate From Single 5-V Supply
- Low Power Requirements
- Pin-to-Pin Replacement for AM26LS32

## description

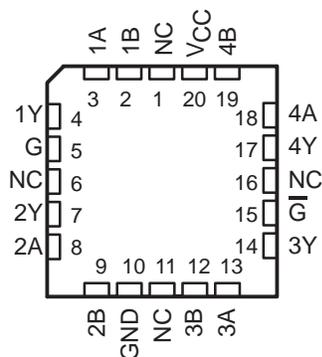
The SN55173, SN65173, and SN75173 are monolithic quadruple differential line receivers with 3-state outputs. They are designed to meet the requirements of TIA/EIA-422-B, TIA/EIA-423-B, TIA/EIA-485-A, and several ITU recommendations. The standards are for balanced multipoint bus transmission at rates up to 10 megabits per second. The four receivers share two OR enable inputs, one active when high, the other active when low. These devices feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of  $\pm 200\text{ mV}$  over a common-mode input voltage range of  $-12\text{ V}$  to  $12\text{ V}$ . Fail-safe design specifies that if the inputs are open circuited, the outputs are always high. The SN65173 and SN75173 are designed for optimum performance when used with the SN75172 or SN75174 quad differential line drivers.

The SN55173 is characterized over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN65173 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ . The SN75173 is characterized for operation from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ .

SN55173 . . . J PACKAGE  
SN65173, SN75173 . . . D OR N PACKAGE  
(TOP VIEW)



SN55173 . . . FK PACKAGE  
(TOP VIEW)



NC—No internal connection

**THE SN55173 IS NOT RECOMMENDED  
FOR NEW DESIGNS.**



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# SN55173, SN65173, SN75173 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

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## AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGED DEVICES			
	PLASTIC SMALL OUTLINE (D)	PLASTIC CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	SN75173D	—	—	SN75173N
–40°C to 85°C	SN65173D	—	—	SN65173N
–55°C to 125°C	—	SN55173FK	SN55173J	—

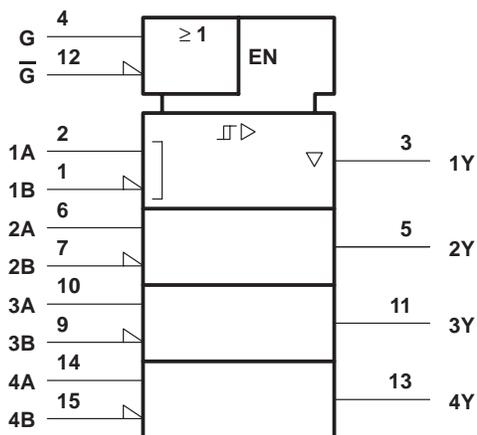
The D package is available taped and reeled. Add the suffix R to the device type (e.g., SN75173DR).

## FUNCTION TABLE (each receiver)

DIFFERENTIAL A–B	ENABLES		OUTPUT Y
	G	$\bar{G}$	
$V_{ID} \geq 0.2 V$	H	X	H
	X	L	H
$-0.2 V < V_{ID} < 0.2 V$	H	X	?
	X	L	?
$V_{ID} \leq -0.2 V$	H	X	L
	X	L	L
X	L	H	Z
Open circuit	X	L	H
	H	X	H

H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

## logic symbol †

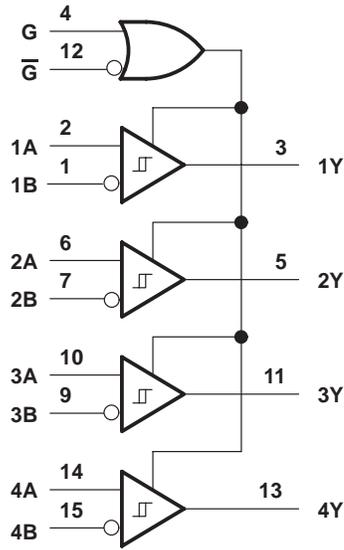


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

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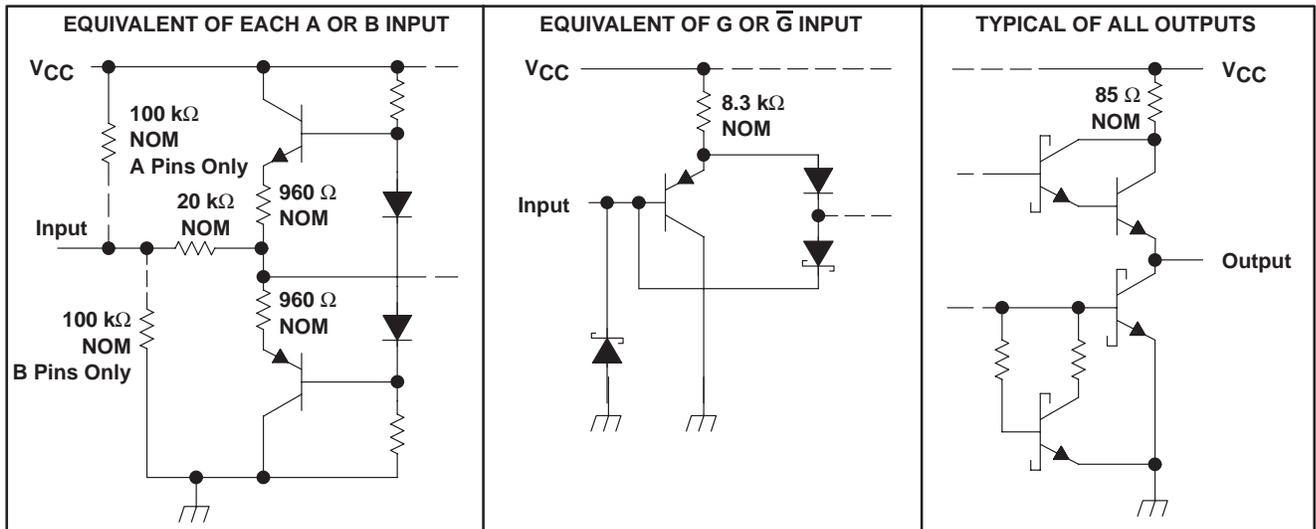
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## logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

## schematics of inputs and outputs



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage ( $V_I$ or B inputs)	$\pm 25$ V
Differential input voltage, $V_{ID}$ (see Note 2)	$\pm 25$ V
Enable input voltage, $V_I$	7 V
Low-level output current, $I_{OL}$	50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package	73°C/W
N package	67°C/W
Continuous total dissipation	See Dissipation Rating Table
Case temperature for 60 seconds, $T_C$ : FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential input voltage, are with respect to network ground terminal.
  2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
  3. The package thermal impedance is calculated in accordance with JESD 51.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
FK	1375 mW	11 mW/°C	880 mW	275 mW
J	1375 mW	11 mW/°C	880 mW	275 mW

## recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$	SN55173	4.5	5	5.5	V
	SN65173, SN75173	4.75	5	5.25	V
Common-mode input voltage, $V_{IC}$				$\pm 12$	V
Differential input voltage, $V_{ID}$				$\pm 12$	V
High-level enable-input voltage, $V_{IH}$		2			V
Low-level enable-input voltage, $V_{IL}$				0.8	V
High-level output current, $I_{OH}$				-400	$\mu\text{A}$
Low-level output current, $I_{OL}$				16	mA
Operating free-air temperature, $T_A$	SN55173	-55		125	°C
	SN65173	-40		85	
	SN75173	0		70	



# SN55173, SN65173, SN75173 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

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**electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature**

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>†</sup>	MAX	UNIT
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>O</sub> = 2.7 V,	I <sub>O</sub> = -0.4 mA			0.2	V
V <sub>IT-</sub>	Negative-going input threshold voltage	V <sub>O</sub> = 0.5 V,	I <sub>O</sub> = 16 mA	-0.2 <sup>‡</sup>			V
V <sub>hys</sub>	Hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> )	See Figure 4			50		mV
V <sub>IK</sub>	Enable-input clamp voltage	I <sub>I</sub> = -18 mA				-1.5	V
V <sub>OH</sub>	High-level output voltage	V <sub>ID</sub> = 200 mV,	I <sub>OH</sub> = -400 μA	SN55173		2.5	V
				SN65173, SN75173		2.7	V
V <sub>OL</sub>	Low-level output voltage	V <sub>ID</sub> = -200 mV,	See Figure 1	I <sub>OL</sub> = 8 mA		0.45	V
				I <sub>OL</sub> = 16 mA		0.5	
I <sub>OZ</sub>	High-impedance-state output current	V <sub>O</sub> = 0.4 V to 2.4 V				±20	μA
I <sub>I</sub>	Line input current	Other input at 0 V,	See Note 3	V <sub>I</sub> = 12 V		1	mA
				V <sub>I</sub> = -7 V		-0.8	
I <sub>IH</sub>	High-level enable-input current	V <sub>IH</sub> = 2.7 V				20	μA
I <sub>IL</sub>	Low-level enable-input current	V <sub>IL</sub> = 0.4 V				-100	μA
r <sub>i</sub>	Input resistance				12		kΩ
I <sub>OS</sub>	Short-circuit output current			-15		-85	mA
I <sub>CC</sub>	Supply current	Outputs disabled				70	mA

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>‡</sup> The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.

NOTE 3: Refer to TIA/EIA-422-B and TIA/EIA-423-B for exact conditions.

## switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

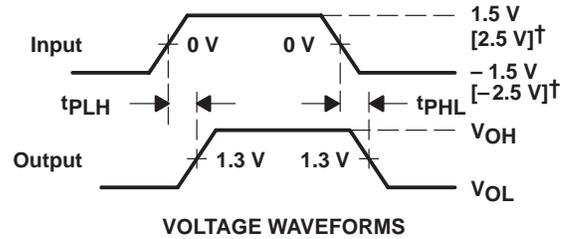
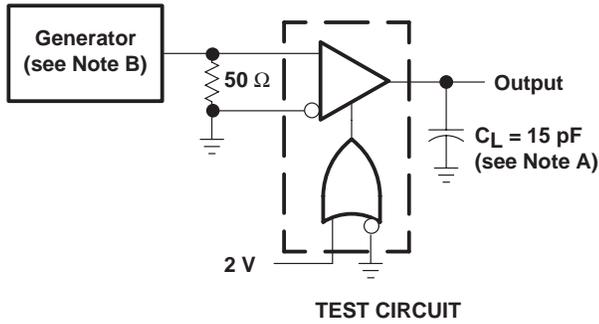
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output	V <sub>ID</sub> = -1.5 V to 1.5 V,			20	35	ns
t <sub>PHL</sub>	Propagation delay time, high-to-low-level output	C <sub>L</sub> = 15 pF,	See Figure 1		22	35	
t <sub>pZH</sub>	Output enable time to high level	C <sub>L</sub> = 15 pF,	See Figure 2		17	22	ns
t <sub>pZL</sub>	Output enable time to low level	C <sub>L</sub> = 15 pF,	See Figure 3		20	25	ns
t <sub>PHZ</sub>	Output disable time from high level	C <sub>L</sub> = 5 pF,	See Figure 2		21	30	ns
t <sub>P LZ</sub>	Output disable time from low level	C <sub>L</sub> = 5 pF,	See Figure 3		30	40	ns



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## PARAMETER MEASUREMENT INFORMATION

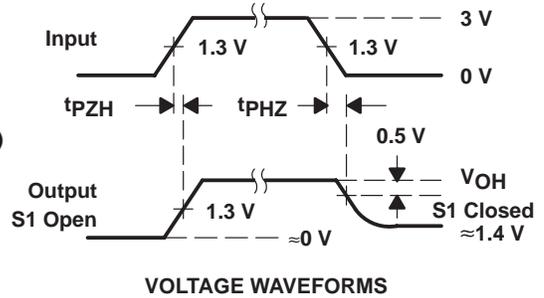
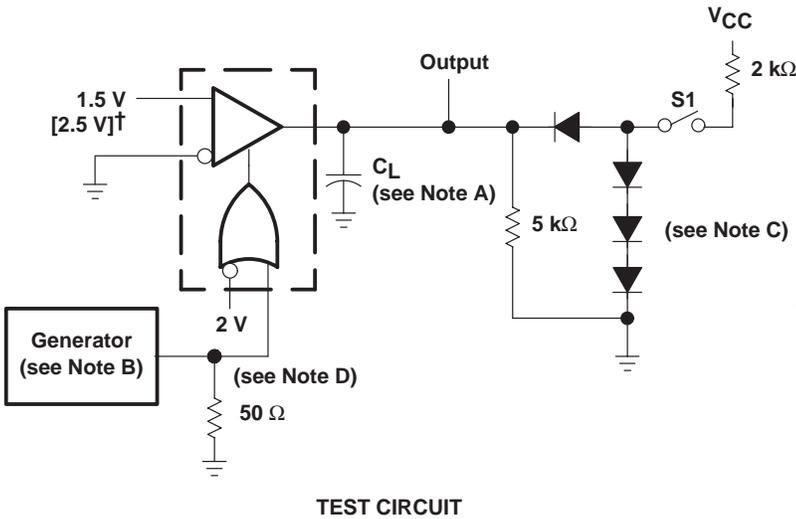


† Voltage for the SN55173 only.

NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_0 = 50 \Omega$ .

Figure 1.  $t_{PLH}$ ,  $t_{PHL}$  Test Circuit and Voltage Waveforms



† Voltage for the SN55173 only.

NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_0 = 50 \Omega$ .

C. All diodes are 1N916, or equivalent.

D. To test the active-low enable  $\overline{G}$ , ground G and apply an inverted input waveform to  $\overline{G}$ .

Figure 2.  $t_{PHZ}$ ,  $t_{PZH}$  Test Circuit and Voltage Waveforms



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## TYPICAL CHARACTERISTICS†

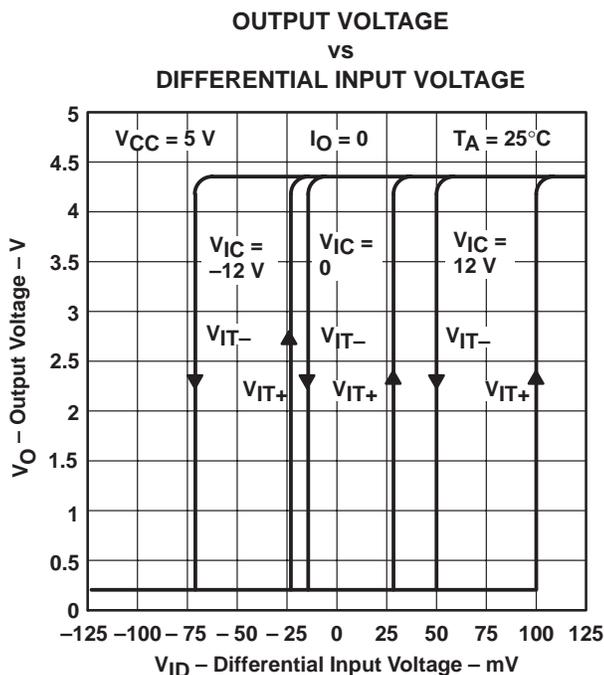


Figure 4

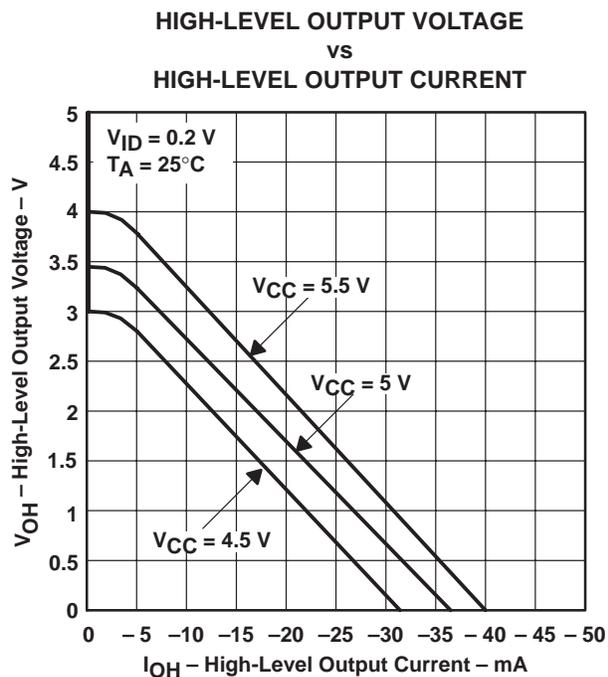


Figure 5

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

TYPICAL CHARACTERISTICS†

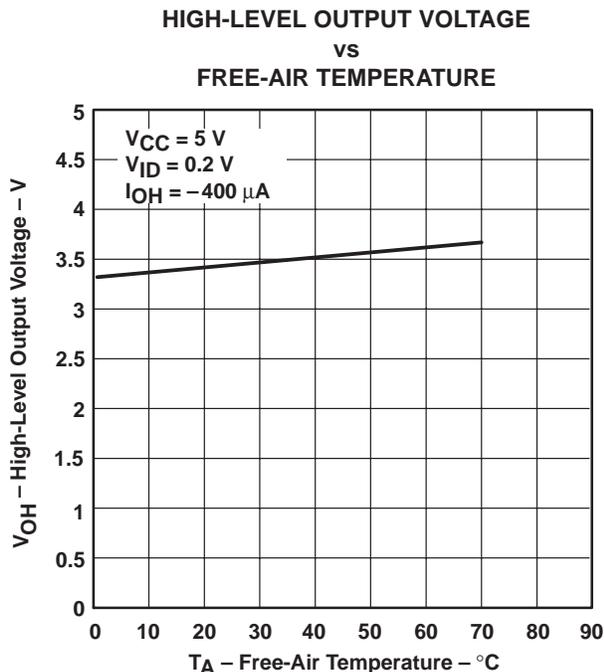


Figure 6

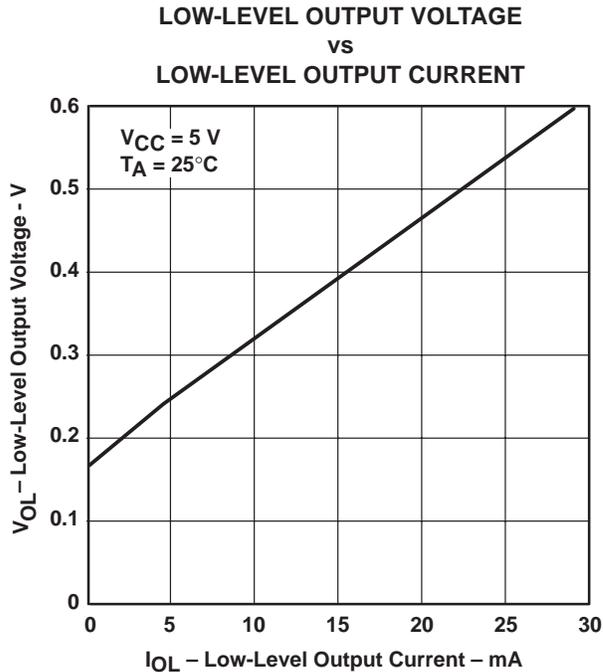


Figure 7

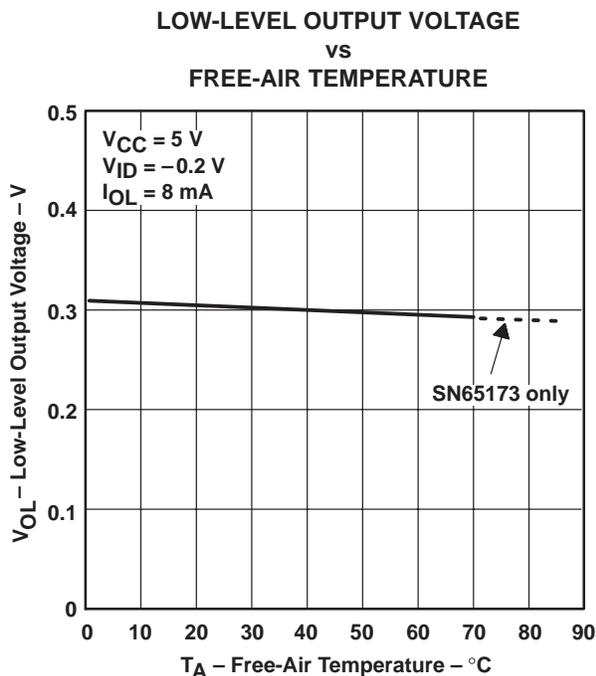


Figure 8

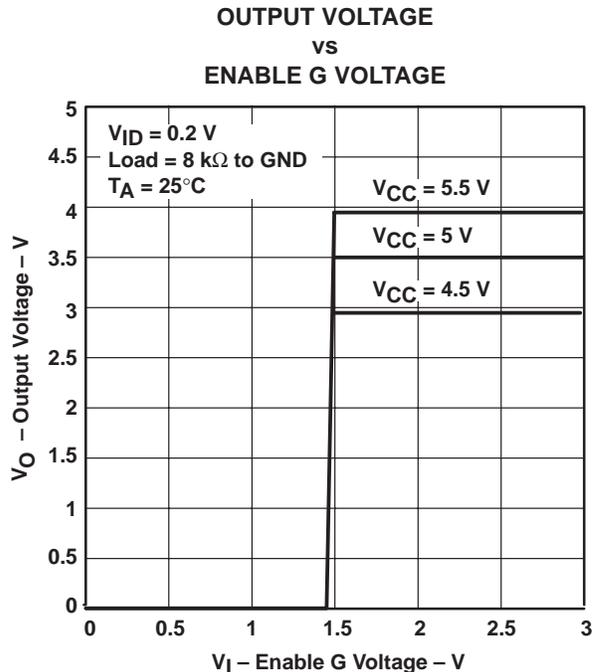


Figure 9

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

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## TYPICAL CHARACTERISTICS

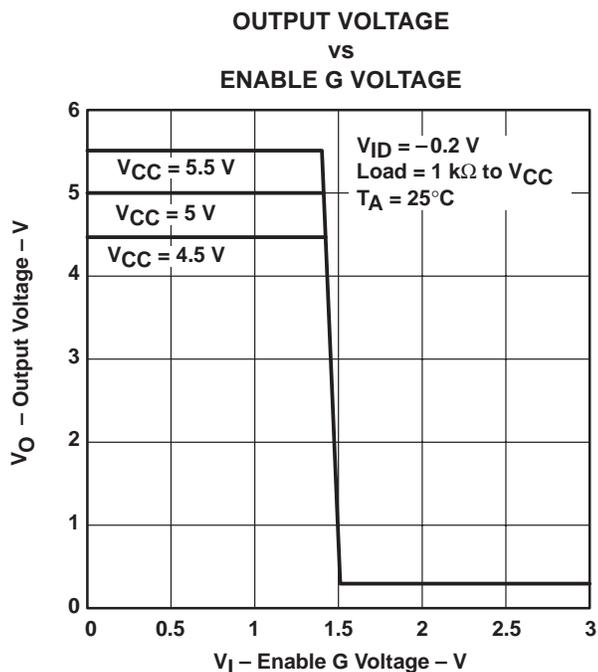


Figure 10

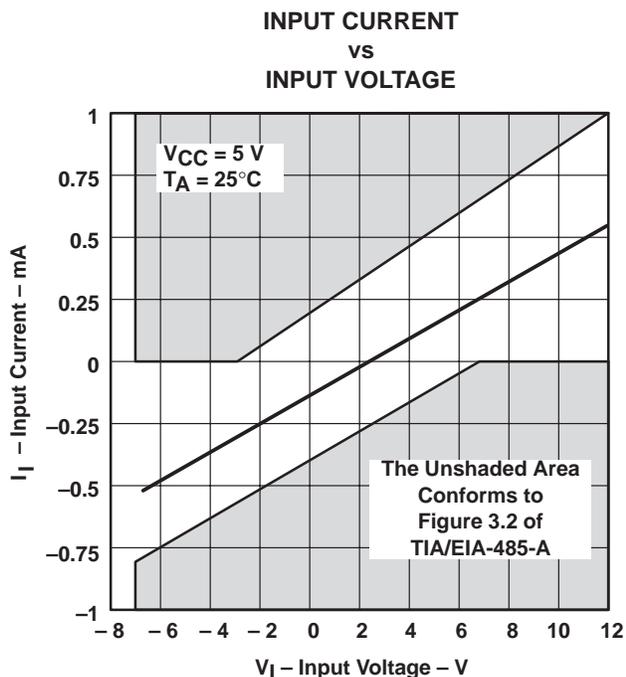
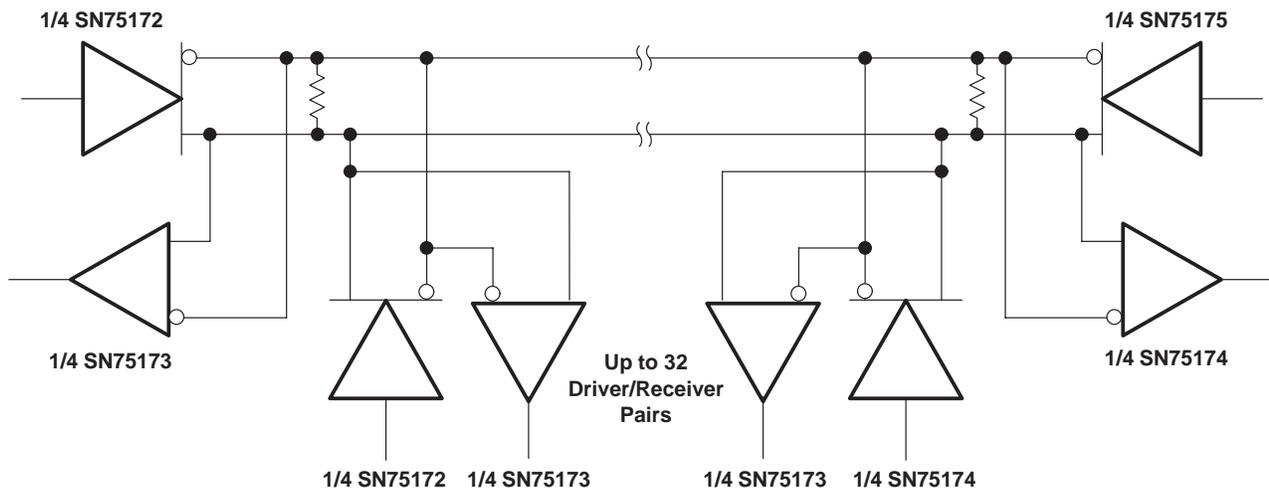


Figure 11

## APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

Figure 12. Typical Application Circuit

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PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN55173J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN65173D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN65173DR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN65173N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN75173D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75173DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75173DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75173DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75173DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75173DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75173J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN75173N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75173NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75173NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75173NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75173NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ55173FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ55173J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

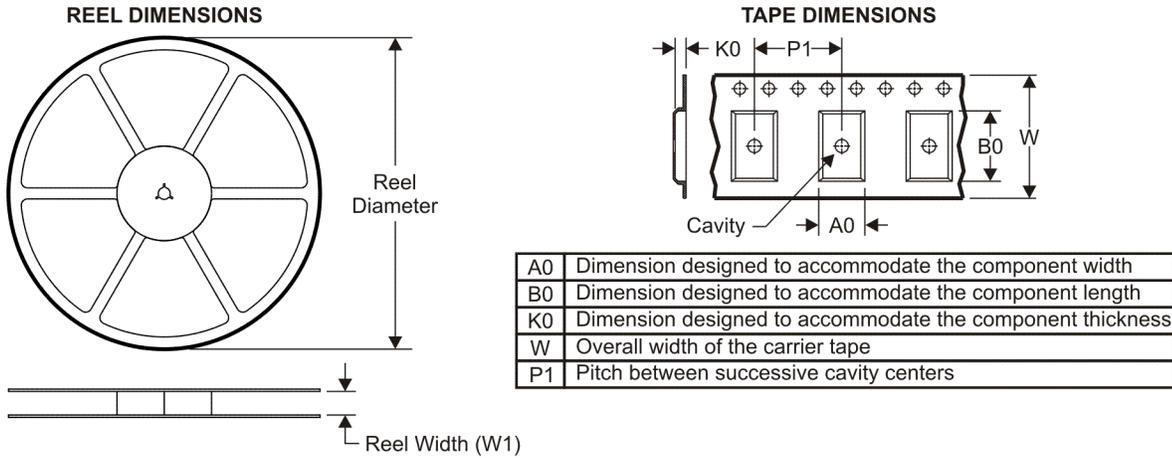
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

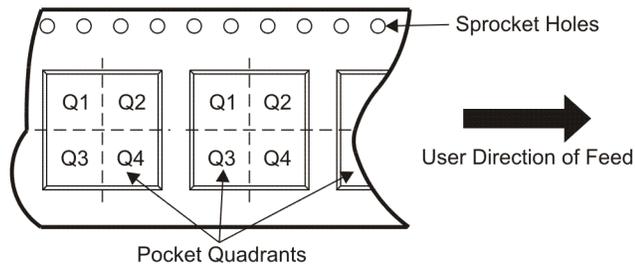
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**TAPE AND REEL INFORMATION**



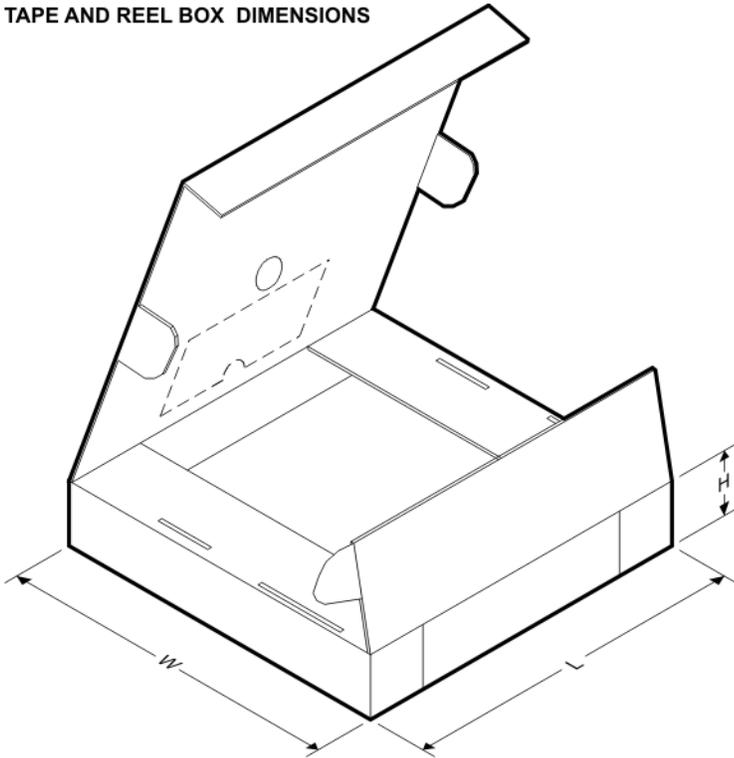
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75173DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75173NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



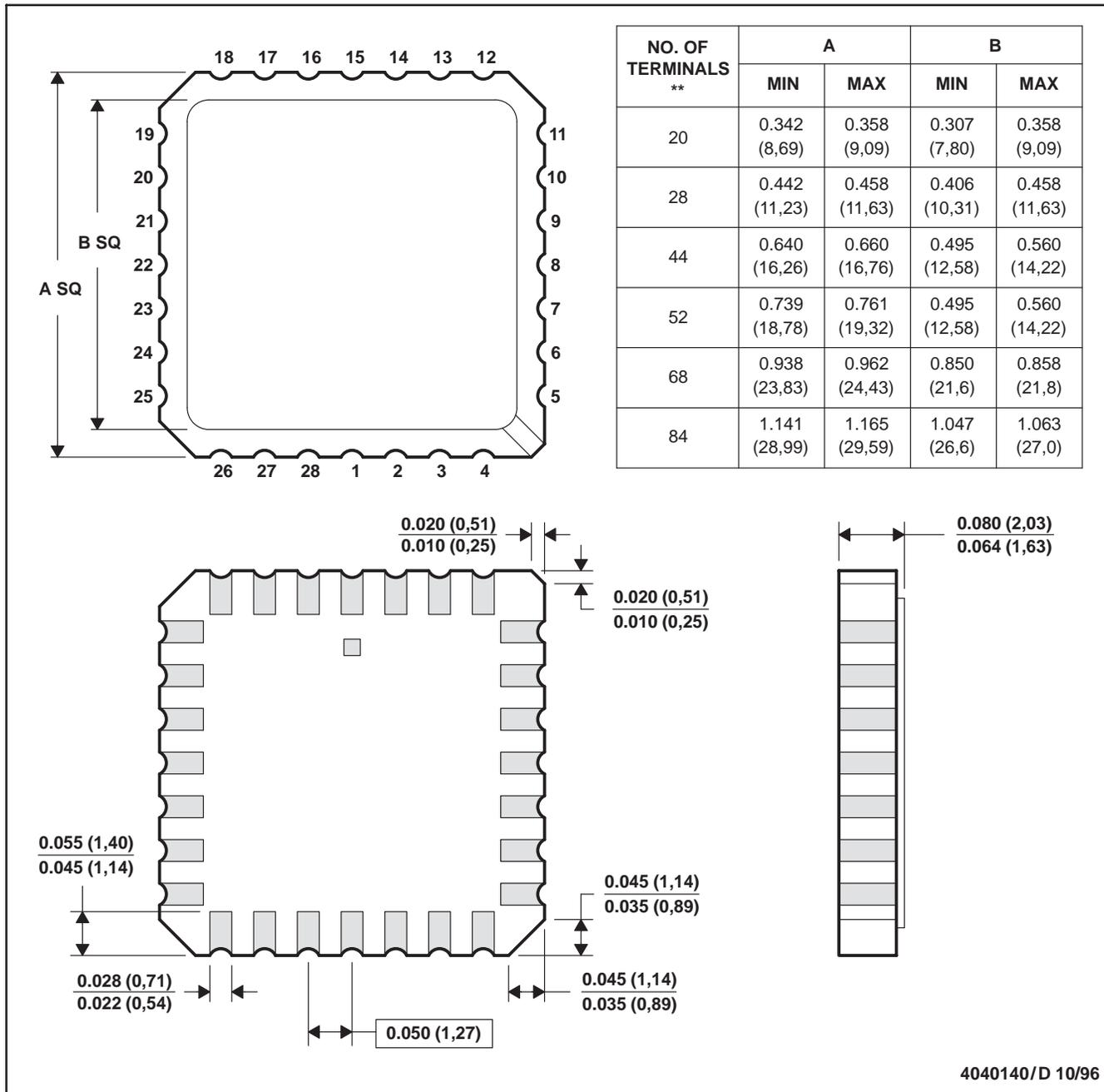
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75173DR	SOIC	D	16	2500	333.2	345.9	28.6
SN75173NSR	SO	NS	16	2000	346.0	346.0	33.0

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

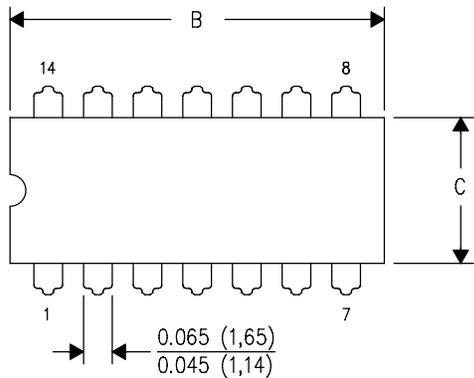


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

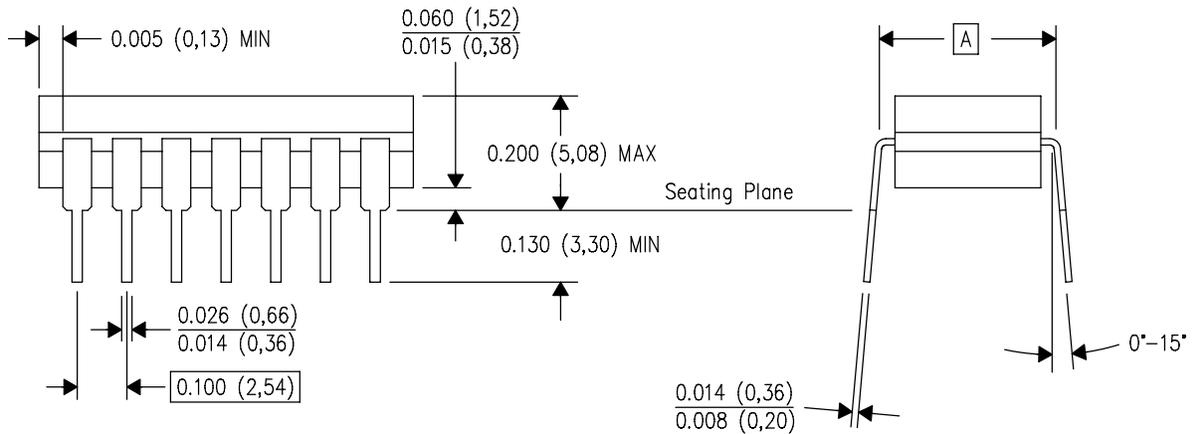
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

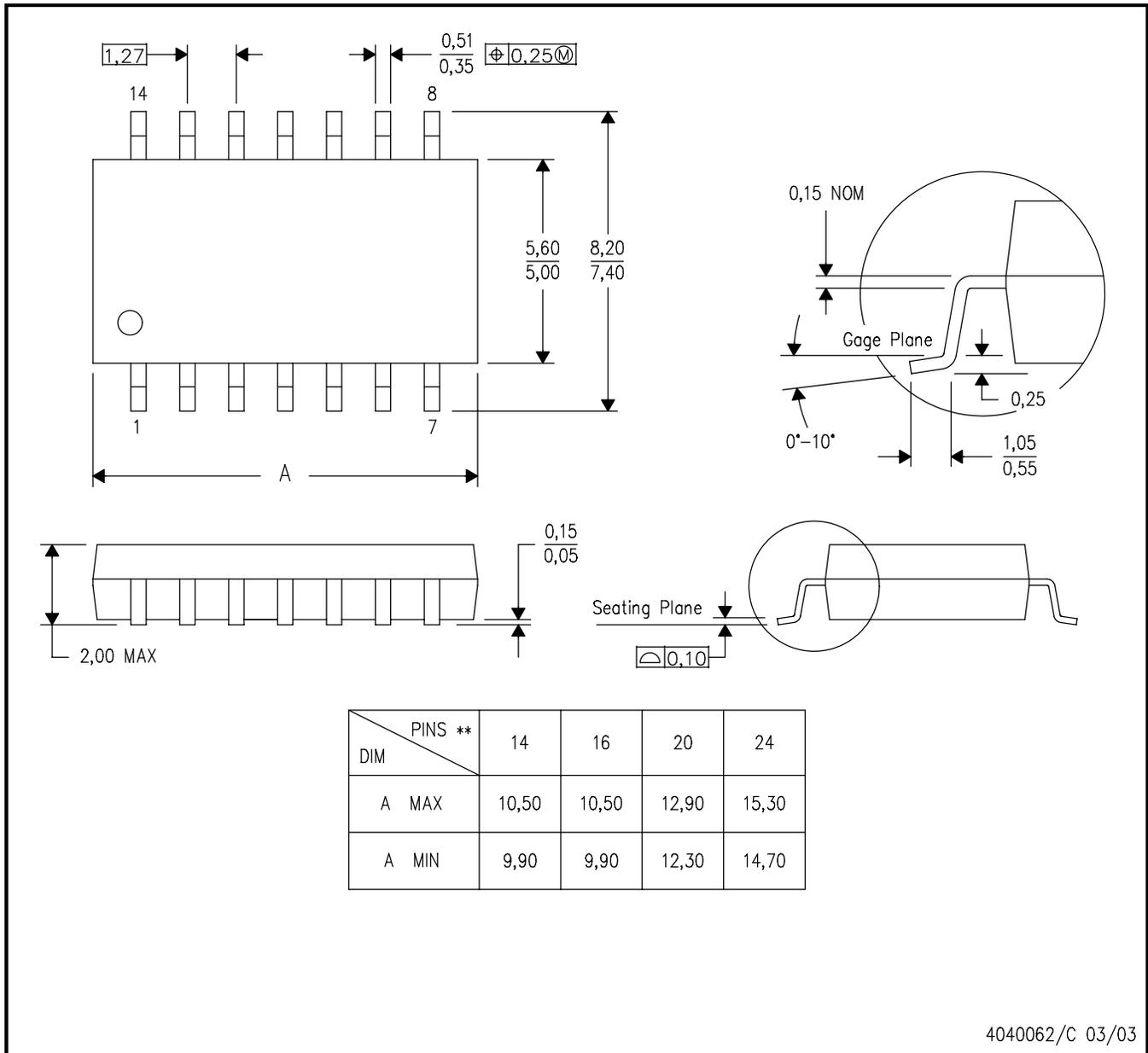
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

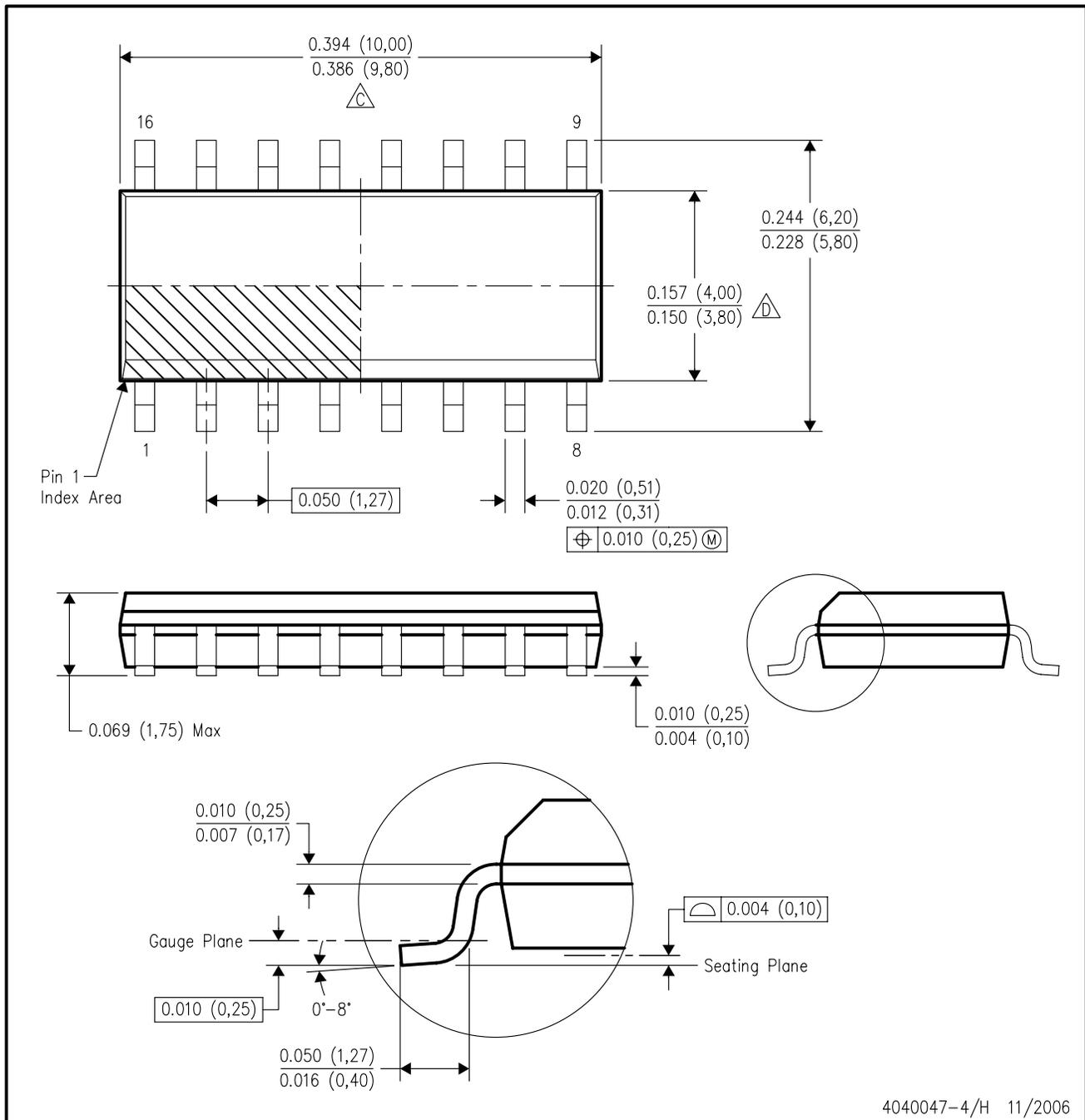
14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE

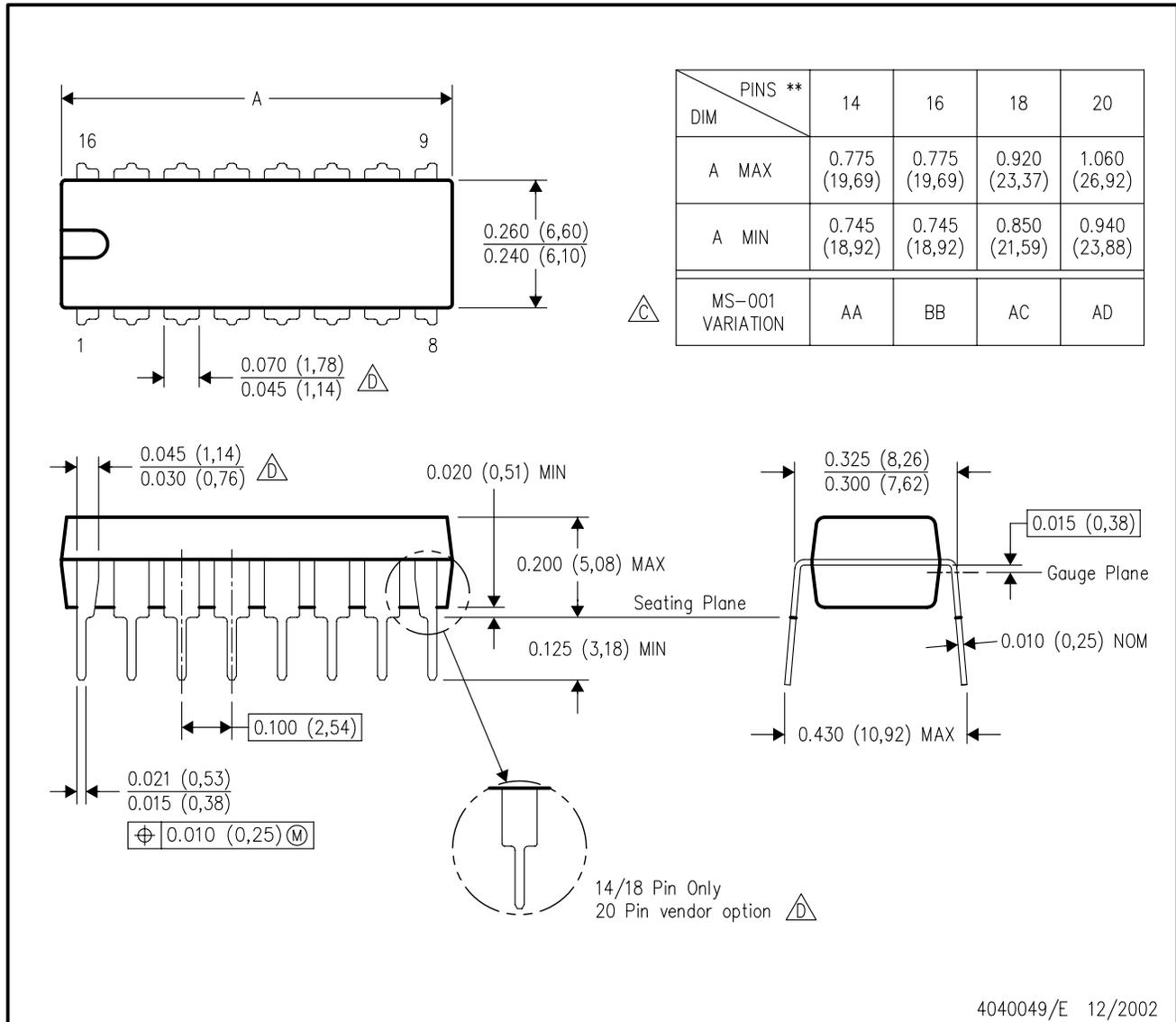


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AC.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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