

Features

- Single 5-V Supply
- 3-State Driver Output Circuitry
- TTL-Compatible Driver Inputs
- TTL-Compatible Receiver Output
- Differential Line Operation
- Receiver Output Strobe
- Designed for Party-Line (Data-Bus) Applications
- Independent Driver and Receiver
- Choice of Open-Collector or Totem-Pole Outputs on Both Driver and Receiver
- Dual Data Inputs on Driver
- Optional Line-Termination Resistor in Receiver
- ± 15 -V Receiver Common-Mode Capability
- Receiver Frequency-Response Control

description

This integrated circuit is designed for use in interfacing between TTL-type digital systems and differential data-transmission lines. It is especially useful for party-line (data-bus) applications. This circuit type combines in one package a 3-state differential line driver and a differential-input line receiver, both of which operate from a single 5-V power supply. The driver inputs and the receiver outputs are TTL compatible. The driver employed is similar to the SN55113 and SN75113 3-state line drivers and the receiver is similar to the SN55115 and SN75115 line receivers.

The SN55116 offers all the features of the SN55113 and SN75113 drivers and the SN55115 and SN75115 receivers combined. The driver performs the dual input AND and NAND functions when enabled or presents a high impedance to the load when in the disabled state. The driver output stages are similar to TTL totem-pole outputs, but have the current-sinking portion separated from the current-sourcing portion and both are brought out to adjacent package terminals. This feature allows the user the option of using the driver in the open-collector output configuration or, by connecting the adjacent source and sink terminals together, using the driver in the normal totem-pole output configuration.

The receiver portion of the SN55116 features a differential-input circuit having a common-mode voltage range of ± 15 V. An internal $130\text{-}\Omega$ equivalent resistor also is provided, which optionally can be used to terminate the transmission line. A frequency-response control terminal allows the user to reduce the speed of the receiver or to improve differential noise immunity. The receiver of the SN55116 has an output strobe and a split totem-pole output. The receiver section of the circuit is independent of the driver section, except for the V_{CC} and ground terminals.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

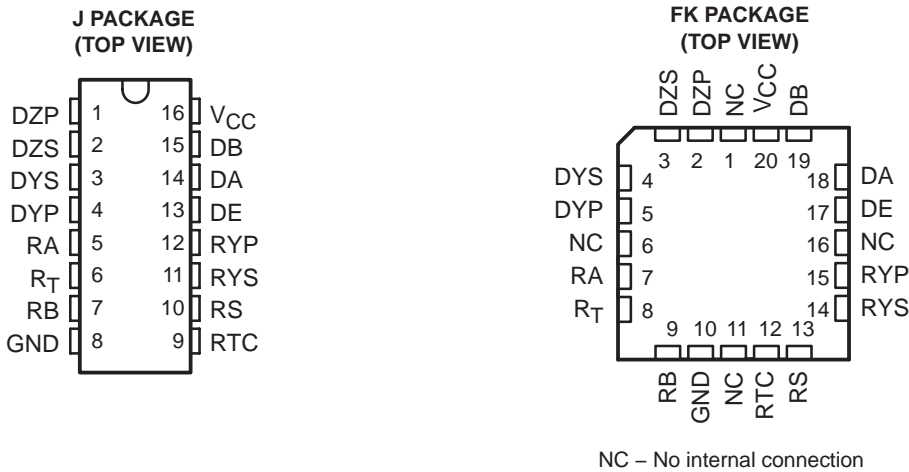
SN55116

DIFFERENTIAL LINE TRANSCEIVERS

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description (continued)

The SN55116 is characterized for operation over the full military temperature range of –55°C to 125°C.



AVAILABLE OPTIONS		
T _A	CHIP CARRIER (FK)	CERAMIC DIP (J)
–55°C to 125°C	SN55116FK	SN55116J

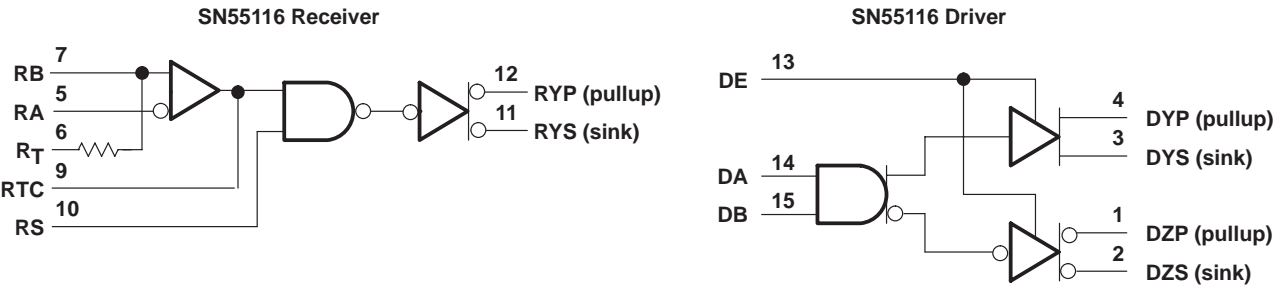
Function Tables

SN55116 DRIVER				
INPUTS			OUTPUTS	
DE	DA	DB	DY	DZ
L	X	X	Z	Z
H	L	X	L	H
H	X	L	L	H
H	H	H	H	L

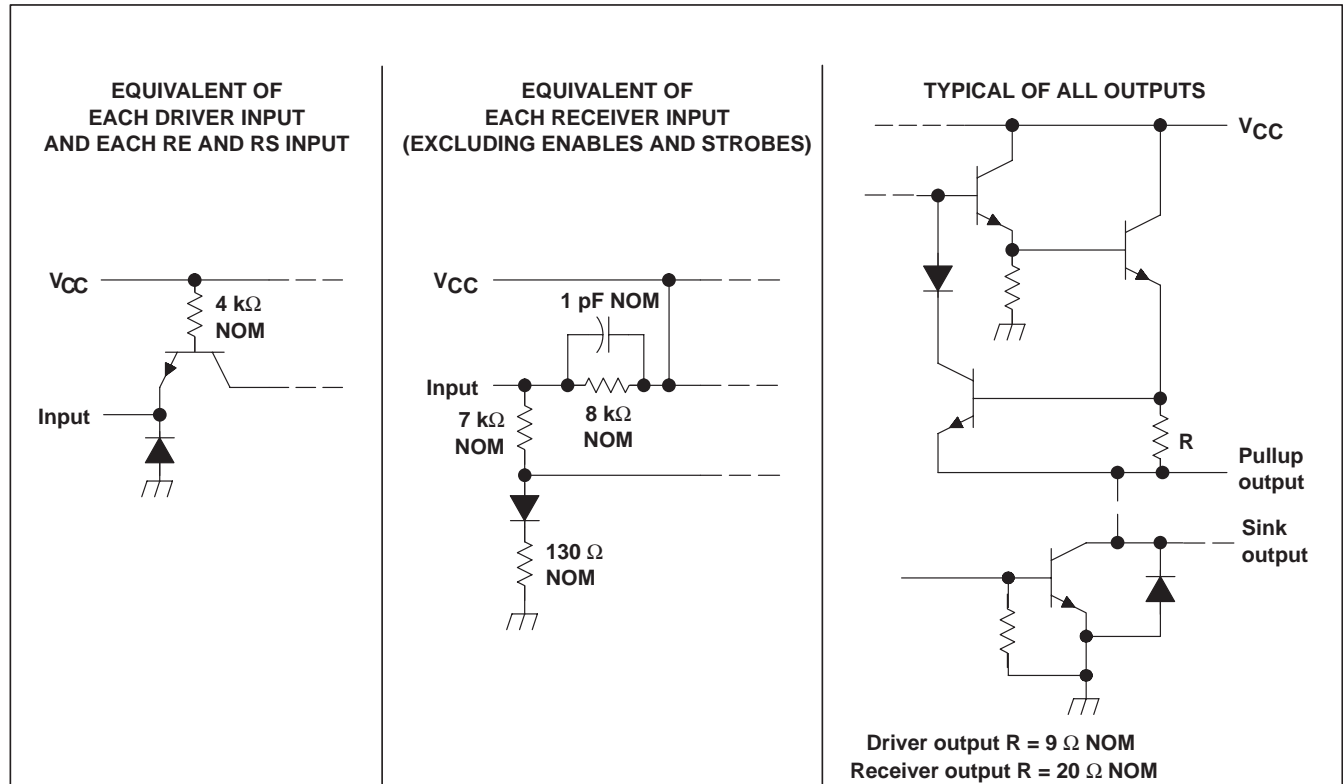
'SN55116 RECEIVER		
RS/RE	DIFF INPUT	OUTPUTS RY
L	X	H
H	L	H
H	H	L

H = high level ($V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max), L = low level ($V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max), X = irrelevant, Z = high impedance (off)

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1 and Note 2)	7 V
Input voltage, V_I : DA, DB, DE, DI, RE, and RS	5.5 V
RA, RB, R_T	$\pm 25\text{ V}$
Off-state voltage applied to open-collector outputs:	12 V
Continuous total power dissipation (see Note 2)	See Dissipation Rating Table
Case temperature for 60 seconds, T_C : FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to the network ground terminal.
2. In the FK and J packages, the SN55116 chip is alloy mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
FK	1375 mW	11 mW/°C	880 mW	275 mW
J	1375 mW	11 mW/°C	880 mW	275 mW

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recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.5	5	5.5	V
V _{IH}	High-level input voltage	All inputs except differential inputs	2			V
V _{IL}	Low-level input voltage				0.8	V
I _{OH}	High-level output current	Drivers			−40	mA
		Receivers			−5	
I _{OL}	Low-level output current	Drivers			40	mA
		Receivers			15	
V _I	Receiver input voltage			±15		V
V _{ICR}	Common-mode receiver input voltage			±15		V
T _A	Operating free-air temperature		−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

driver section

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$,	$I_I = -12 \text{ mA}$	-0.9	-1.5		V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{IH} = 2 \text{ V}$	$T_A = 25^\circ\text{C}$	$I_{OH} = -10 \text{ mA}$	2.4	3.4	V
				$I_{OH} = -40 \text{ mA}$	2	3	
		$T_A = -55^\circ\text{C}$ to 125°C		$I_{OH} = -10 \text{ mA}$	2		
				$I_{OH} = -40 \text{ mA}$	1.8		
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$,	$V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 40 \text{ mA}$			0.4	V
V_{OK}	Output clamp voltage	$V_{CC} = \text{MAX}$,	$I_O = -40 \text{ mA}$, DE at 0.8 V			-1.5	V
$I_{O(\text{off})}$	Off-state open-collector output current	$V_{CC} = \text{MAX}$, $V_O = 12 \text{ V}$	$T_A = 25^\circ\text{C}$		1	10	μA
			$T_A = \text{MAX}$			200	
I_{OZ}	Off-state (high-impedance state) output current	$V_{CC} = \text{MAX}$, DE at 0.8 V, $T_A = \text{MAX}$	$V_O = 0$ to V_{CC} , DE at 0.8 V, $T_A = 25^\circ\text{C}$			±10	μA
			$V_O = 0$			-300	
			$V_O = 0.4 \text{ V}$ to V_{CC}			±150	
I_I	Input current at maximum input voltage	Driver or enable input	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High-level input current		$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			45	
I_{IL}	Low-level input current		$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1.6	
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$,	$V_O = 0$, $T_A = 25^\circ\text{C}$	-40		-120	mA
I_{CC}	Supply current (driver and receiver combined)	$V_{CC} = \text{MAX}$,	$T_A = 25^\circ\text{C}$		42	60	mA

† All parameters, with the exception of off-state open-collector output current, are measured with the active pullup connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}$, $C_L = 30 \text{ pF}$, $T_A = 25^\circ\text{C}$

driver section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation-delay time, low-to-high level output	See Figure 13		14	30	ns
t_{PHL}	Propagation-delay time, high-to-low level output			12	30	
t_{PZH}	Output-enable time to high level	$R_L = 180 \Omega$, See Figure 14		8	20	ns
t_{PHZ}	Output-disable time from high level	$R_L = 180 \Omega$, See Figure 14		16	30	ns



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

receiver section

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IT+} Positive-going threshold voltage §		$V_O = 0.4 \text{ V}$, $I_{OL} = 15 \text{ mA}$	$V_{CC} = \text{MIN}$, V_I $CR = 0$, See Note 3			0.5	V
			$V_{CC} = 5 \text{ V}$, V_I $CR = \text{MAX}$, See Note 4			1	
V_{IT-} Negative-going threshold voltage §		$V_O = 2.4 \text{ V}$, $I_{OL} = -5 \text{ mA}$	$V_{CC} = \text{MIN}$, V_I $CR = 0$, See Note 3	-0.5¶			V
			$V_{CC} = 5 \text{ V}$, V_I $CR = \text{MAX}$, See Note 4	-1¶			
V_I Input voltage range #		$V_{CC} = 5 \text{ V}$, $V_{ID} = -1 \text{ V}$ or 1 V		15	-15		V
V_{OH} High-level output voltage		$I_{OH} = -5 \text{ mA}$	$V_{CC} = \text{MIN}$, $V_{ID} = -1 \text{ V}$, $V_{ICR} = 0$, See Note 3	2.4			V
			$V_{CC} = 5 \text{ V}$, $V_{ID} = -1 \text{ V}$, $V_{ICR} = \text{MAX}$, See Note 5	2.4			
V_{OL} Low-level output voltage		$I_{OL} = 15 \text{ mA}$	$V_{CC} = \text{MIN}$, $V_{ID} = 1 \text{ V}$, $V_{ICR} = 0$, See Note 3			0.4	V
			$V_{CC} = 5 \text{ V}$, $V_{ID} = 1 \text{ V}$, See $V_{ICR} = \text{MAX}$, Note 5			0.4	
$I_{I(\text{rec})}$ Receiver input current		$V_{CC} = \text{MAX}$	$V_I = 0$, Other input at 0 V	-0.5	-0.9		mA
			$V_I = 0.4 \text{ V}$, Other input at 2.4 V	-0.4	-0.7		
			$V_I = 2.4 \text{ V}$, Other input at 0.4 V	0.1	0.3		
I_I Input current at maximum input voltage	Strobe	$V_{CC} = \text{MIN}$, $V_{ID} = -0.5 \text{ V}$, $V_{\text{strobe}} = 4.5 \text{ V}$				5	μA
I_I Low-level input current	Strobe	$V_{CC} = \text{MAX}$, $V_{ID} = 1 \text{ V}$, $V_{\text{strobe}} = 0.4 \text{ V}$, See Note 3				-2.4	mA
$I_{(\text{RTC})}$ Response-time-control current (RTC)		$V_{CC} = \text{MAX}$, RC at 0 V ,	$V_{ID} = 1 \text{ V}$, See Note 3	$T_A = 25^\circ\text{C}$	-1.2		mA
$I_{O(\text{off})}$ Off-state open-collector output current		$V_{CC} = \text{MAX}$, $V_O = 12 \text{ V}$, $V_{ID} = -1 \text{ V}$	$T_A = 25^\circ\text{C}$		1	10	μA
			$T_A = \text{MAX}$			200	
R_T Line-terminating resistance		$V_{CC} = 5 \text{ V}$	$T_A = 25^\circ\text{C}$		77	167	Ω
I_{OS} Short-circuit output current§		$V_{CC} = \text{MAX}$, $V_{ID} = -0.5 \text{ V}$,	$V_O = 0$, See Note 3	$T_A = 25^\circ\text{C}$	-15	-80	mA
I_{CC} Short current (driver and receiver combined)		$V_{CC} = \text{MAX}$, $V_{ID} = 0.5 \text{ V}$, See Note 3		$T_A = 25^\circ\text{C}$	42	60	mA

† Unless otherwise noted, $V_{\text{strobe}} = 2.4 \text{ V}$. All parameters, with the exception of off-state open-collector output current, are measured with the active pullup connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$, and $V_{IC} = 0$.

§ Differential voltages are at the B input terminal with respect to the A input terminal.

¶ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.

Input voltage range is the voltage range that, if exceeded at either input, will cause the receiver to cease functioning properly.

NOTES: 3. This applies with the less-positive receiver input grounded.

4. This applies with the more-positive receiver input at 15 V or the more negative receiver input at -15 V .



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switching characteristics, $V_{CC} = 5\text{ V}$, $C_L = 30\text{ pF}$, $T_A = 25^\circ\text{C}$

receiver section

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation-delay time, low to high-level output	$R_L = 400\ \Omega$, See Figure 15			20	75	ns
t_{PHL}	Propagation-delay time, high to low-level output				17	75	ns
t_{PZH}	Output-enable time to high level	$R_L = 480\ \Omega$, See Figure 14			9	20	ns
t_{PHZ}	Output-disable time from high level	$R_L = 480\ \Omega$, See Figure 14			12	30	ns



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TYPICAL CHARACTERISTICS†

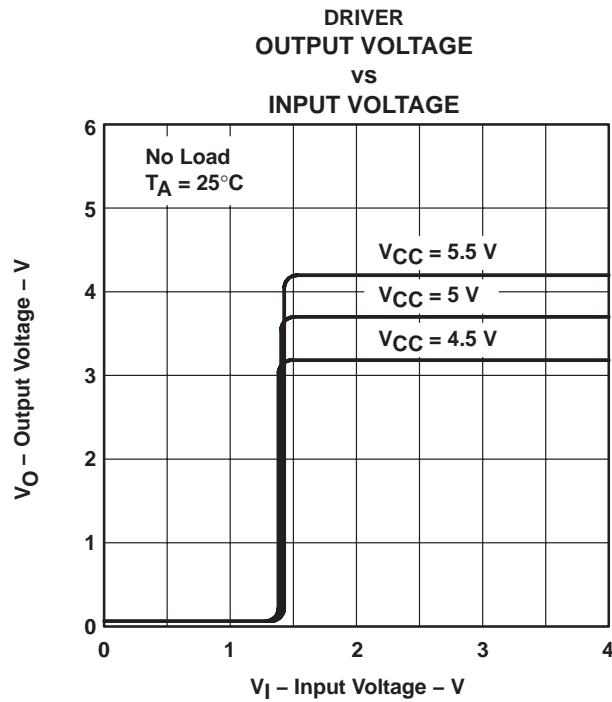


Figure 1

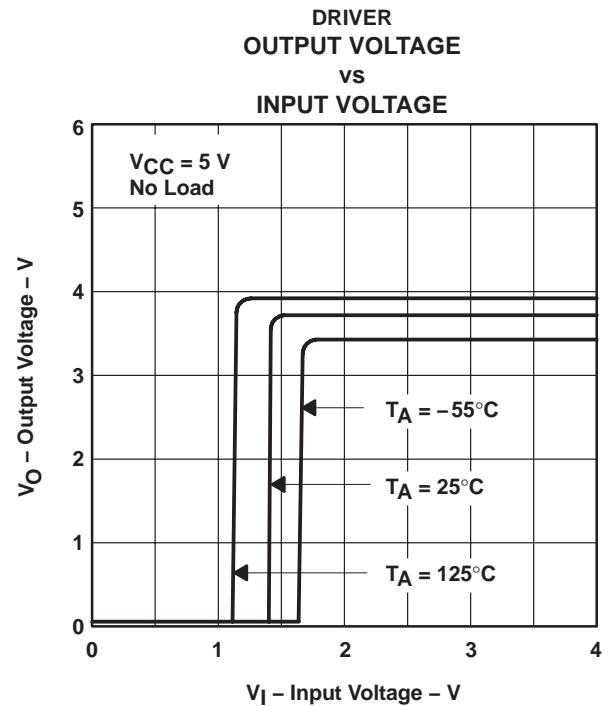


Figure 2

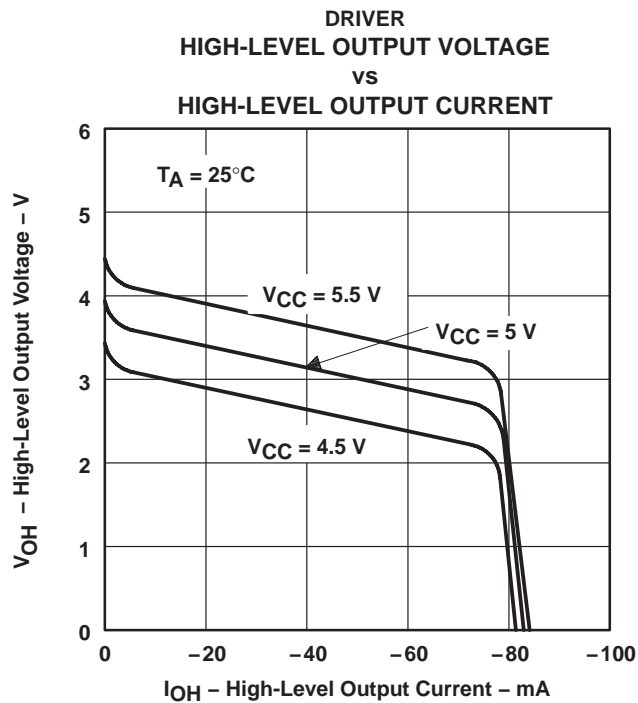


Figure 3

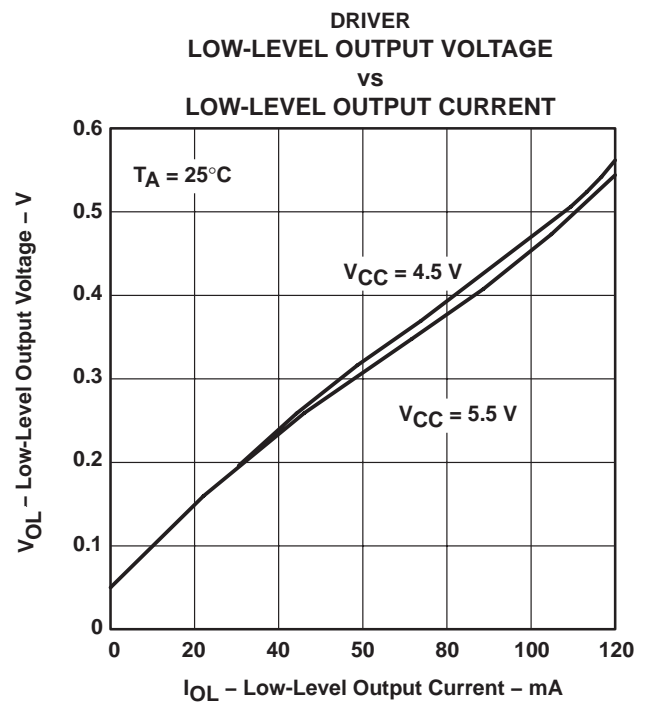


Figure 4

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

TYPICAL CHARACTERISTICS†

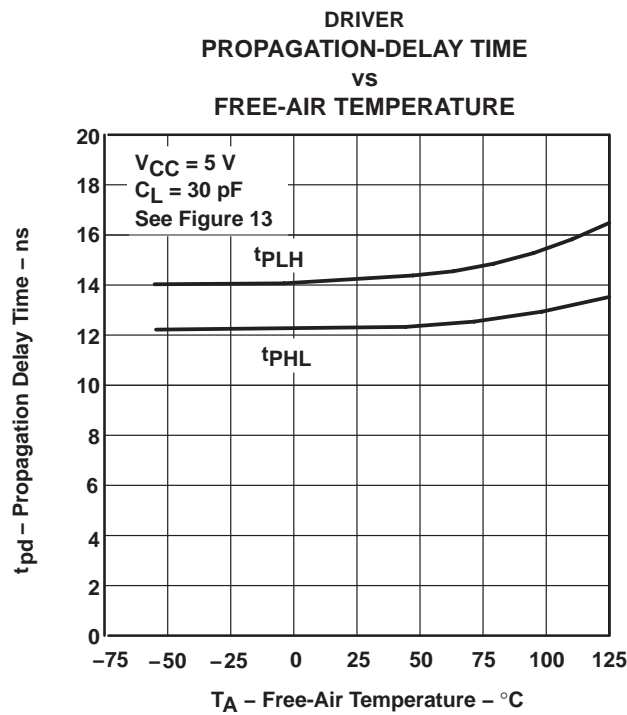


Figure 5

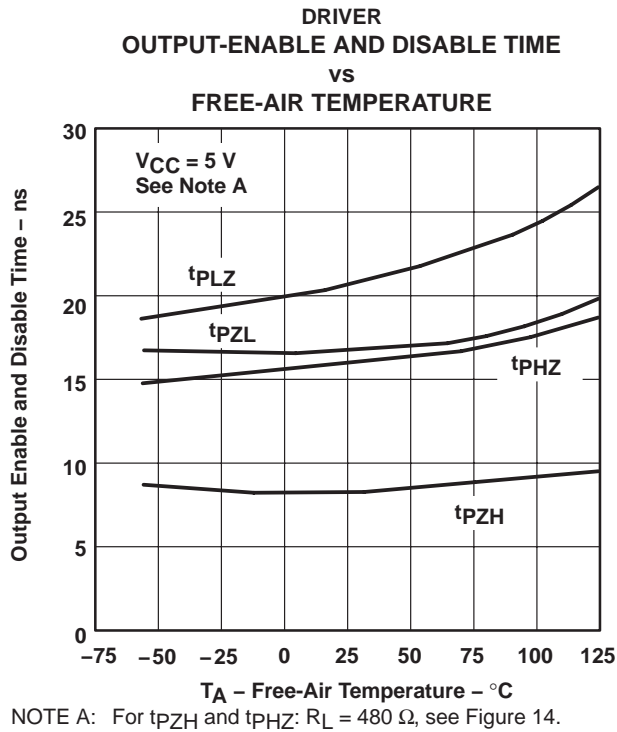


Figure 6

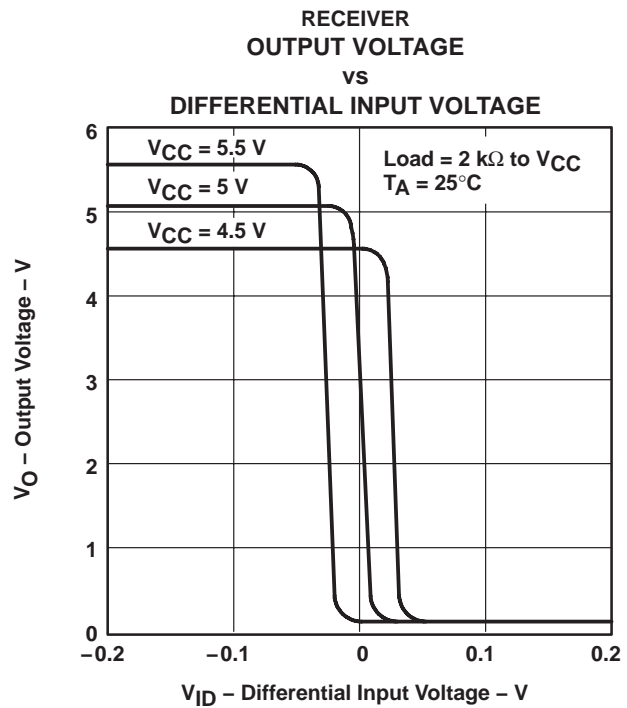


Figure 7

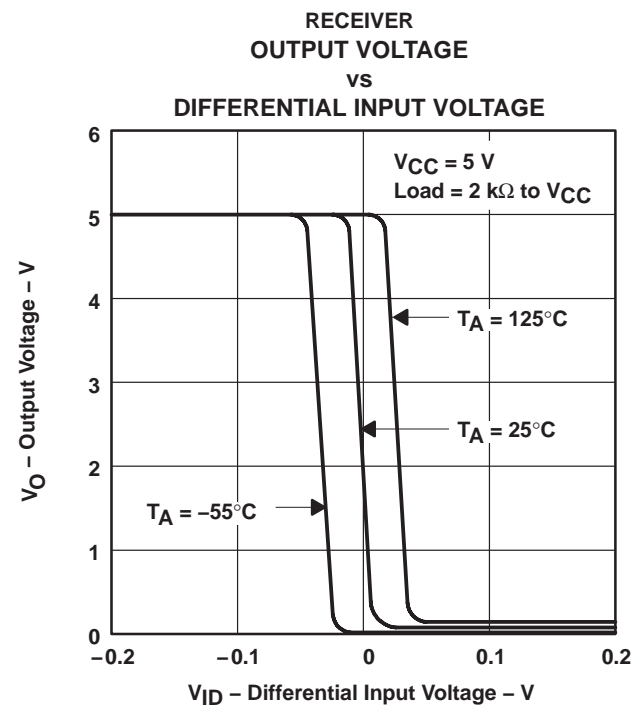


Figure 8

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

TYPICAL CHARACTERISTICS†

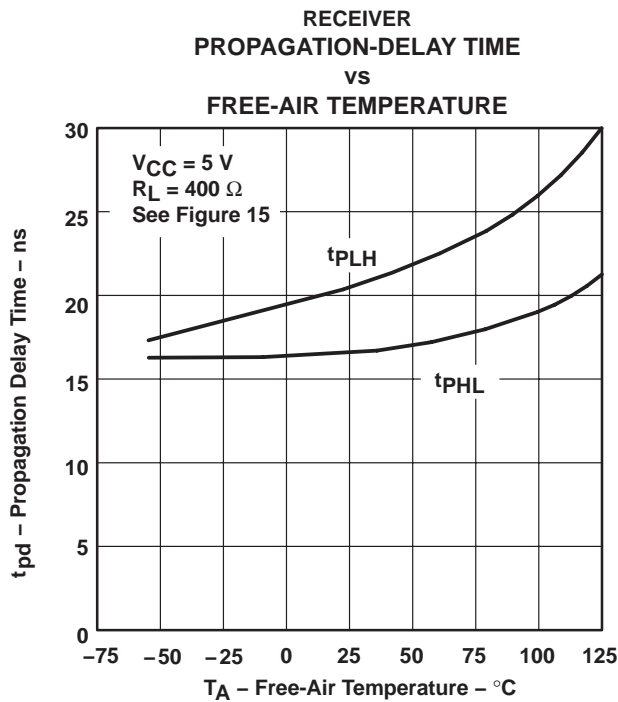


Figure 9

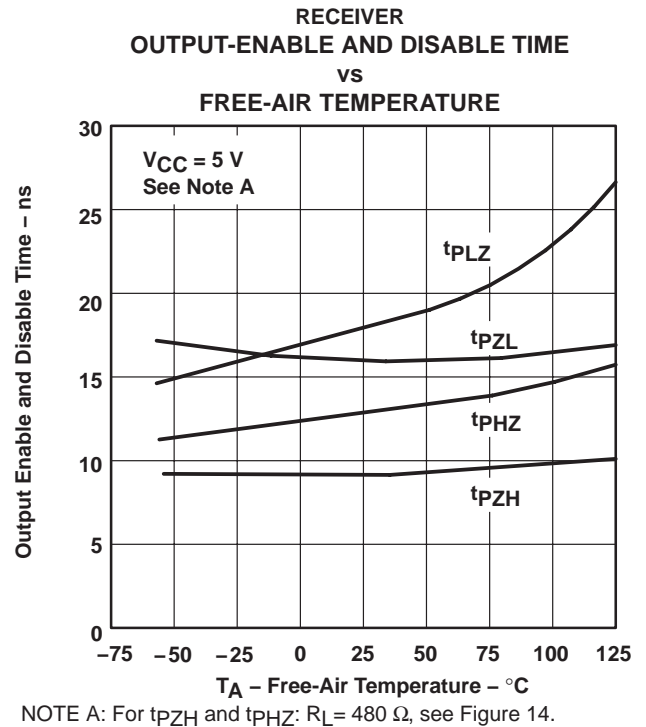


Figure 10

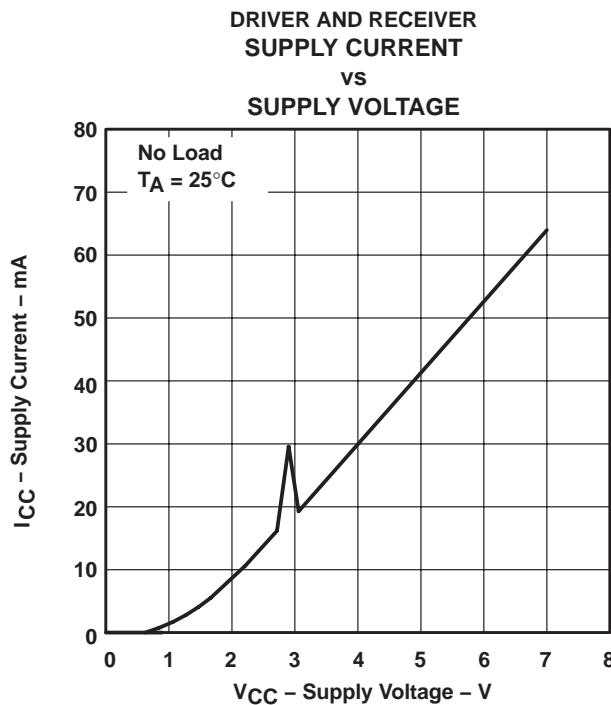


Figure 11

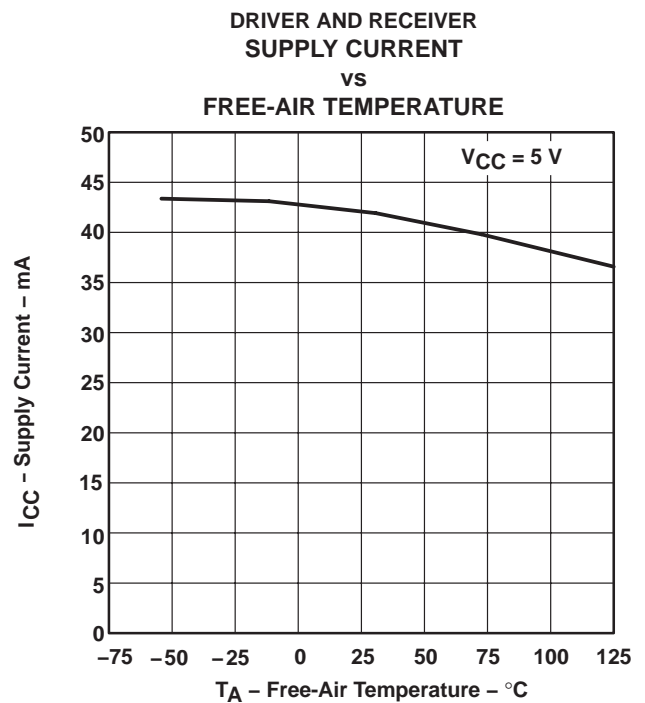


Figure 12

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

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PARAMETER MEASUREMENT INFORMATION

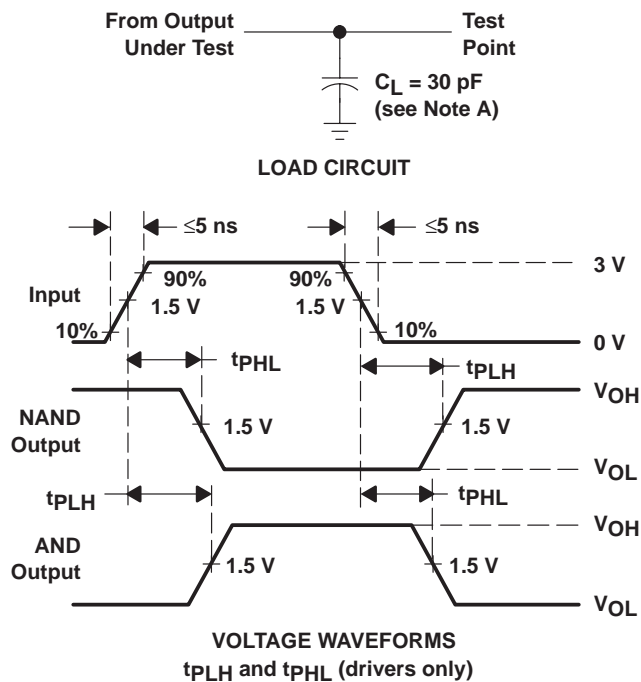


Figure 13

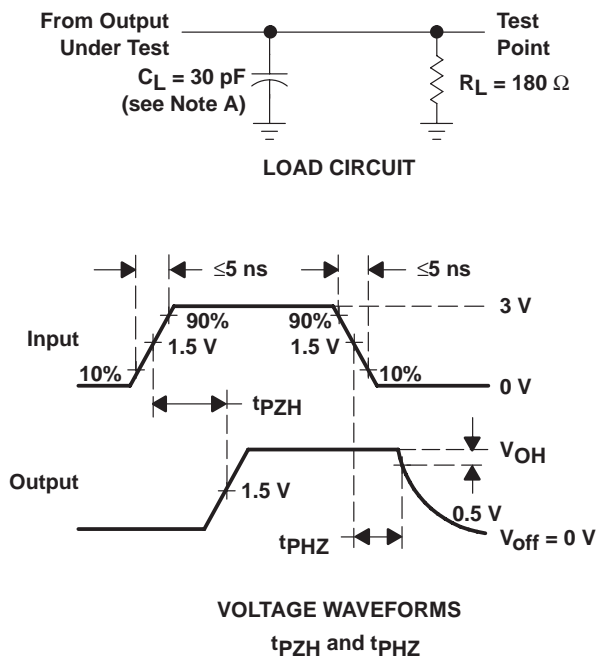


Figure 14

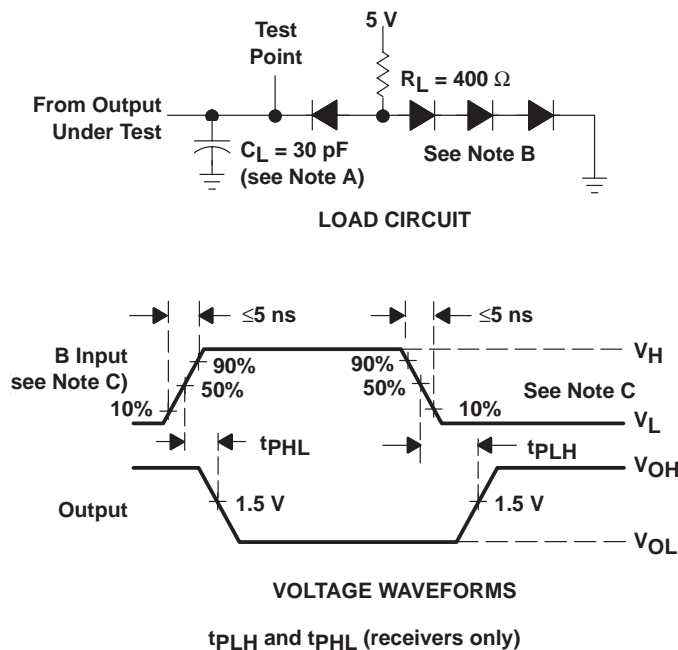


Figure 15

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. All diodes are 1N3064 or equivalent.
 - C. $V_H = 3 \text{ V}$, $V_L = -3 \text{ V}$, the A input is at 0 V.
 - D. When testing the receiver sections, the response-time control and the termination-resistor pins are left open.



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-88511012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8851101EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
SN55116J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SNJ55116FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ55116J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN55116 :

- Catalog: [SN75116](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

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