Voltage Spike Measurement Technique and Specification

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ABSTRACT

As an extension to the voltage ratings given in the Absolute Maximum Ratings section of TAS5111, TAS5112, TAS5121 and TAS5122 data sheets this application note gives a more explicit description of the maximum limit for peak voltage vs. time on the BST and OUT pins. Additionally, a measurement technique and test setup is described and application design guidelines given on how to avoid exceeding the device voltage limitation defined as envelope curves.

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1 Introduction

TAS5111, TAS5112, TAS5121 and TAS5122 devices are all Class-D amplifier output stages designed to provide high-power output at high efficiency and low harmonic distortion. As typically seen in high-speed power devices the voltage potential on specific pins swing high (and low) with very large dv/dt leaving artifacts that it are important to consider while designing the environment (i.e., PCB and external components) for the power stage device.

The issue addressed in this apps note, in particular, is the voltage overshoot that is likely to occur when current is flowing into a half-bridge during a low-to-high transition.

2 Background

In a normal Class-D amplifier configuration the half-bridge output sees a demodulation filter and a load (loudspeaker). Typically, the demodulation filter is a second order L-C filter, i.e., there is at least some amount of inductance in series with the half-bridge output. This inductance, independent of a high-to-low or low-to-high transition, keeps the output current constant in the period around the transition moment.

The transition of interest in this context is the low-to-high transition that occurs while current is flowing **into** the half-bridge (hereafter referred to as *negative current*). Before the transition, the low-side device (LSD) is on and current is flowing into the half-bridge, through the LSD channel, out through the GND pin, and into the GND net (plane) on the PCB. At the same time, the high-side device (HSD) is off and **no** current is flowing from the power supply into half-bridge power pin (HSD drain), i.e., the voltage potential on the power supply pin is identical to the DC potential of the power supply.

Approaching the transition moment, the LSD is turned off and the HSD is turned on; the half-bridge current continues to flow due to the de-modulation filter inductance. The only path the current can take is up through the HSD (and/or HSD body diode) and out through the power supply pin. However, there will always be some amount inductance (stray or purposely inserted) associated with the power supply pin/net. In the recommended TAS51xx power stage configuration, the only initial path the current can take is through the TT-snubber R and C, as a result the voltage potential on the power supply pin is increased and hereby the voltage potential on the half-bridge output pin. Eventually (in a matter of nanoseconds), the inductance in the power supply path will carry the current and the power supply pin voltage flattens out around the DC value of the power supply.

As explained, *a negative-current*, *low-to-high transition* causes: a voltage peak on the power supply pin and a voltage overshoot on the output pin. It is easy to realize that last mentioned effect also creates a voltage overshoot on the bootstrap supply pin (BST) due to the capacitive coupling between the output pin and the bootstrap pin.

Obviously, there is a limit to how much voltage the power stage device can handle on the power supply, output pin, and the bootstrap pin without physical damage. These limits are listed in the Absolute Maximum Ratings section of the device data sheets. The information in this apps note is an extension to the ratings already given in the data sheets.

3 Absolute Maximum Voltage vs. Time

Throughout the device characterization the individual components within the device under test has been analyzed. Usually, the individual components are rated at DC voltage but there is actually a second dimension: time. Very simply, some components are less likely to fail when the duration of a pulse is short compared to long. This characteristic has been carefully studied and based on process distribution data, device characterization and weeks of life-testing it has been possible to determine the specifications for the absolute maximum voltage vs. time allowed on the pins of interest.

This application note focuses on two situations of operation and specifies the maximum allowed voltage vs. time in each situation. The data presented relates to *commercial temperature range devices.*

The results are shown for the bootstrap pins (BST) only. The limits for the power supply pins (PVDD) and output pins (OUT) are typically **10 V lower** than what is shown for BST.

3.1 Absolute Maximum Voltage vs. Time on BST_X, Normal Operation

The voltage vs. time curve shown in Figure 1 is the most conservative of the limit curves presented in this application note. Think of it as an *envelope curve*, i.e., as long at the voltage over time measurement in the actual application falls **on or below** the envelope curve the application is reliable with regard to voltage overshoot on rising edge transitions.

The term *Normal Operation* is defined as: any situation likely to happen as part of daily operation of the end equipment (application) that will **not** trigger the fault protection system within the device. This includes power supply variation, load impedance drops (dynamic behavior of speaker), power-up/down etc.

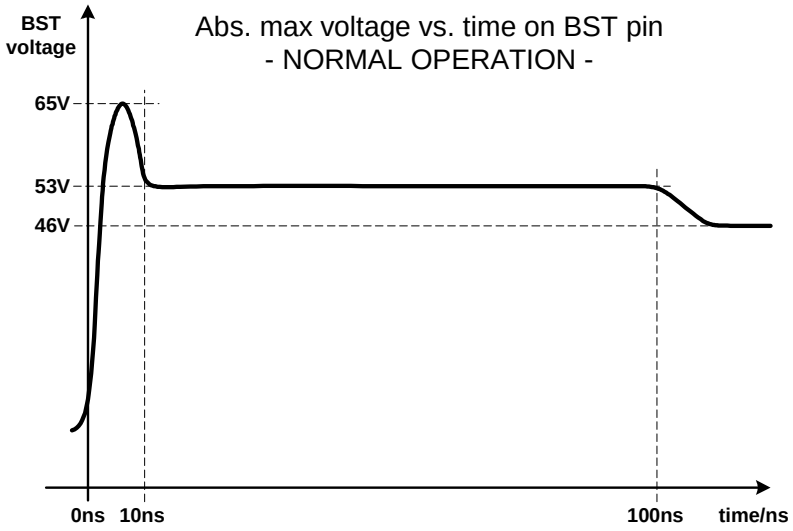

Figure 1 Absolute Maximum Voltage vs. Time, Rising Edge Transition on BST, Normal Operation

If the application can be designed such that the normal operation envelope curve is not exceeded in **any** situation **including** fault situations the application is also safe with regard to voltage overshoot.

3.2 Absolute Maximum Voltage vs. Time on BST_X, Fault Situation

If the application can not be designed such that the normal operation envelope curve is not exceeded in fault situations, i.e., any situation_that **will** trigger the fault protection_system within the device, a less conservative envelope curve has been specified (see Figure 2). If compared to Figure 1 it can be seen that slightly higher voltage is accepted in a fault situation, however, the duration must be shorter.

If the voltage vs. time measurement, in a fault situation, for the actual application falls **on or below** the envelope curve the application is reliable with regard to voltage overshoot. There are, however, certain requirements for external components (see section 5.2) if the extra voltage margin in fault situations is exploited.

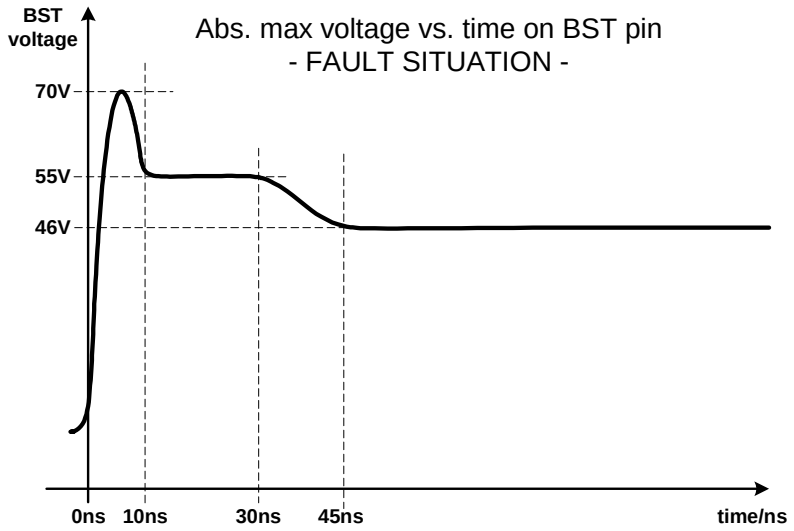

Figure 2 Absolute Maximum Voltage vs. Time, Rising Edge Transition on BST, Fault Situation

4 Voltage Spike Measurement Technique

Now that the envelope curves for different situations of overshoot have been defined a more practical issue arises: how can the actual voltage overshoot in the application be measured with sufficient accuracy?

Obviously, a fast oscilloscope it the answer to this question but, as it turns out, there is more to it than this.

4.1 Equipment (Oscilloscope and Probes)

It is of paramount importance to use an oscilloscope with sufficient bandwidth. The signal that needs to be measured (rising edge transition on the BST bin) typically has **very** high dv/dt (rise time). If the oscilloscope has too low bandwidth, the measurements will be inaccurate. It is recommended to use oscilloscopes with bandwidth greater than 1 GHz.

The next step is selecting the right probe. Obviously, the probe should not limit the bandwidth of the scope and it must have a sufficient voltage rating. This combination of speed and voltage range can make probe selection is difficult because most high bandwidth probes are limited in voltage range.

Once a suitable probe has been located, it is recommended to perform a probe calibration prior to the actual measurement. Typically, probe calibration involves connecting the probe to a reference signal (usually an output from the oscilloscope) and tuning the capacitive voltage divider ratio between the probe and the scope to match the resistive voltage divider ratio between the probe and the scope. Trustworthy measurements are contingent upon a highly accurate tuned probe. For more detail on how to calibrate/tune probes, read through the help information provided with most oscilloscopes.

Unfortunately most probes (even high-bandwidth probes) are delivered with long ground wires (typically 4 inches of black wire with an alligator clip). **Never** use those ground wires for high frequency measurements.

It is mandatory to always use a short ground wire for the measurements described in this application note. See Figure 3 for an example of a suitable clip.

Figure 3 This is how the ground wire should look

4.2 Test Setup

As explained previously, there are two categories of operation for the device under test (DUT).

1. Normal Operation (DUT protection system **not** activated)
2. Fault situations (DUT protection system activated)

The following sections describe the test setups **most likely** to reveal the worst case voltage over time. It is, however, difficult to generalize – some applications might behave different than other applications.

4.2.1 How to Make the Measurement

Independent of application type, it is important to follow a few simple guidelines on how to probe the signal of interest (see Figure 4).

1. Always probe as close to the pin as possible.
2. Always use a short ground clip, referenced as close to the DUT GND pin(s) as possible.

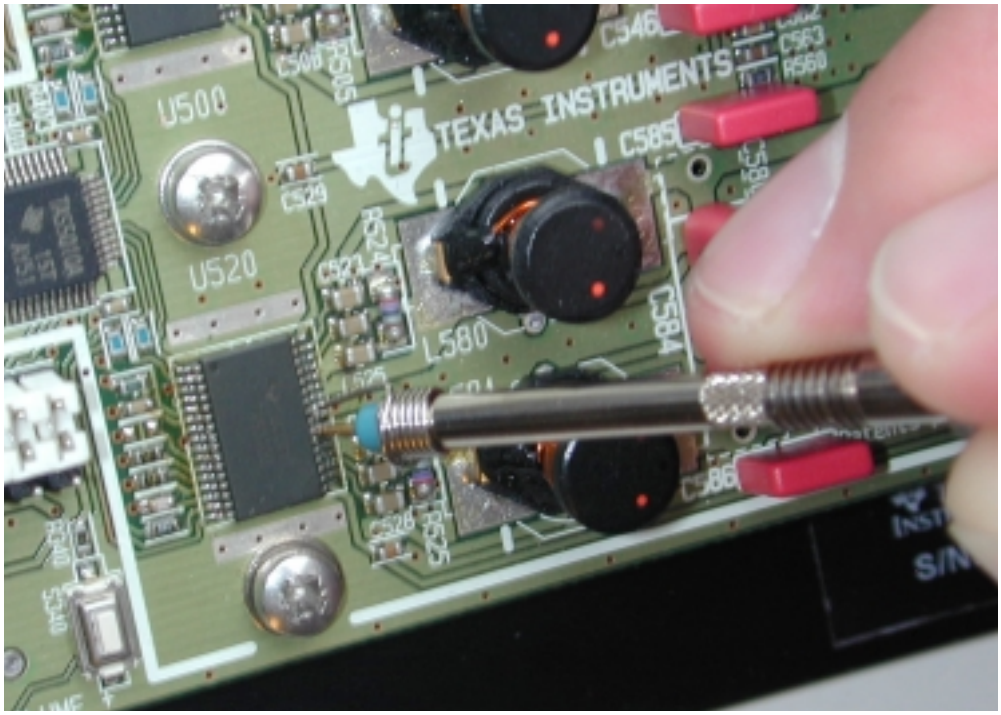

Figure 4 Probe as close to the pin as possible

Figure 4 shows the ideal measurement technique. Unfortunately, this approach can be impractical for PAD-UP devices (heat slug on the top side of the package) **unless** the PCB has been prepared for this measurement. For more detail on PCB layout see Section 5.1.

4.2.2 Normal Operation - Test Setup

Normal operation was defined as: any situation likely to happen as part of daily operation of the end equipment (application) that will **not** trigger the fault protection system within the device.

Generally, the worst case situation with regard to voltage overshoot is low-to-high transitions with high negative current. The following test procedure should ensure a waveform capture in the worst case situation:

1. Prepare the measurement equipment; connect the probe(s).
    a. Adjust the oscilloscope to a suitable voltage/time scale (e.g., 10V/div, 10ns/div).
    b. Set trigger to rising edge.
    c. (Enable “Digital Phosphorus Storage (DPO)” or “Infinite Persistence” function if possible)
2. Adjust the power supply voltage to the highest potential typically seen in the application.
3. Connect a resistive dummy-load corresponding to the lowest dynamic resistance seen in the application.
4. Attach the application heatsink (or control the DUT temperature according to typically seen in the application)
5. Apply a 1-kHz full-scale sinewave input (or the highest amplitude signal typically seen in the application).
6. Adjust the oscilloscope trigger to capture only the highest overshoot transitions.
    a. Stop the trigger when the worst-case transition has been captured (typically after a few hundred data acquisitions).
7. Use the oscilloscope measure or cursor functions to verify that the target envelope limit is not exceeded.

NOTE: *It is recommended to experiment with the test setup in the search for other situations that could cause worse voltage overshoot as compared to what was captured in the previously described sequence.*

4.2.3 Fault Situation - Test Setup

A fault situation was defined as: any situation that **will** trigger the fault protection system within the device.

Usually, the worst case situation with regard to voltage overshoot is the last low-to-high transition preceding an over-current (OC) shutdown due to a speaker terminal short to power supply occurrence. (In case the application is not designed to be reliable against shorts to power supply, the worst case situation is likely to be OC shutdown due to speaker terminal-to-terminal shorts or load impedance drops.)

The following test procedure should ensure a waveform capture in the worst case (highest voltage overshoot amplitude) situation:

1. Prepare the measurement equipment; connect the probe(s).
    a. Adjust the oscilloscope to a suitable voltage/time scale (e.g., 10V/div, 10ns/div).
    b. Probe DUT showdown output (/SD).
    c. Set trigger to falling edge of /SD.
    d. Enable “Voltage Peak Measurement” function if available on the oscilloscope.
    e. (Enable “Digital Phosphorus Storage (DPO)” or “Infinite Persistence” function if available on the oscilloscope).
2. Adjust the power supply voltage to the highest potential typically seen in the application.
3. Attach the application heatsink (or control the DUT temperature according to typically seen in the application)
4. Apply a 1-kHz full-scale sinewave input (or the highest amplitude signal typically seen in the application).
5. Short-circuit the speaker terminal to the power supply (or short-circuit the two speaker terminals)
6. Repeat Step 5. many times to ensure that the worst-case transition has been captured.
7. Use the oscilloscope “measure” or “cursor” functions to verify that the target envelope limit is not exceeded.

NOTE: *It is recommended to experiment with the test setup in the search for other situations that could cause worse voltage overshoot as compared to what was captured in the previously described sequence.*

5 Recommended Configuration

In general, it is highly recommended to follow application schematics and layout guidelines as given in device datasheets and other TI documentation. Additionally, this section gives a few important tips on how to do design a reliable application.

5.1 PCB Layout

A few basic guidelines:

1. Keep the ground plane as solid (unbroken) as possible below and around the power stage section of the PCB.
2. Keep the inductance in the R-C part of the TT-snubber[1] loop as low as possible. (see datasheet application schematic for more detail).
3. Prepare the PCB for voltage overshoot measurement on all BST pins:
    a. Place a via (and maybe a small probe pad) right below the BST pins. These pads will allow the test engineer to probe the pin of interest (through minimal inductance) from the bottom side of the PCB, away from the heat sink.
    b. Ensure access to the ground plane directly below the GND pins.

5.2 Bootstrap series resistor

Some application schematics show a resistor (1R5) connected in series with the bootstrap capacitor. This resistor is:

- Highly recommended in applications that fall within the normal operation envelope curve even in a fault situation.
- Mandatory in applications that exploit the extra voltage margin provided by the fault situation envelope curve.

Additionally, it is recommended to limit the BST capacitor size to 6.8 nF.

[1] The TT-snubber is the R-C network located between the PVDD_x pin and GND_x pin.

5.3 Transient Voltage Suppressors (TVS)

In case the application does not fall within envelope curves given, it is recommended to improve the PCB layout generally by:

- Reducing inductance in the R_C part of the TT-snubber loop
- Improving the ground plane.
- Ensuring that the TT-snubber inductance (the inductance between the PVDD pin and the power supply de-coupling capacitor) is designed properly.

If the application still fails the voltage overshoot test, the solution could be to implement transient voltage suppressors (TVS) components between the device output pin and ground. (For more detail see the power stage device datasheet.) However, it should be noted that even with TVS components in place, it is still **very** important to optimize the PCB layout. Use of TVSs is not a guarantee for operation within the envelope curves given in this application note.

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