# TAS5755M 2 × 50W (2 × 19W + 1 × 50W) Digital Input Audio Amplifier With Integrated Audio Processor and 2.1 Mode Support

## 1 Features

- Reduced Solution Size and BOM Cost:
  - Single-chip 2.1, 2.0 and Mono Mode Capable
  - Single-filter in Mono (PBTL) Mode.
  - Pad-up Package and 80 mΩ $R_{DSON}$ Enhances Thermal Performance
- High Output Power capable:
  - 2 × 19 W +1 × 50 W in 2.1 mode (2 × 4 Ω + 1 × 6 Ω, 24 V)
  - 2 × 50 W in 2.0 mode (2 × 6 Ω, 24 V)
  - 1 × 100 W in Mono Mode (1 × 2 Ω, 24 V)
  - Wide Voltage Range: 8 V to 26.4 V
- Audio Performance Audio:
  - THD+N ≤ 0.05% at 1 kHz ($R_{SPK}$ = 8 Ω, POUT = 1 W, PVDD = 18 V)
  - ICN ≤ 50 µVRMS
  - Crosstalk ≤ - 67 dB
  - SNR ≥ 104 dB
  - BD Modulation Available, for Improved Audio Performance and Efficiency.
- Integrated Audio Processing:
  - 2 × 8 + 1 × 2 Biquads
  - Two-band + Single-band configurable Dynamic Range Control (DRC)
  - License-Free 3D Effects
  - Signal Mixing and DC blocking filter
  - Automatic Rate Detection
- Integrated Self-protection
  - Thermal Protection
  - Over-current Limit Protection
  - Under-voltage Protection

## 2 Applications

- DTV, UHD and Multi-Purpose Monitors
- Sounds Bars, PC Audio
- General Purpose Audio Equipment

## 3 Description

The TAS5755M is a single-chip flexible digital audio solution with integrated processing that supports 2.1 (2 speakers + subwoofer), 2.0 or stereo (2 speakers) and mono (high power speaker) modes.

Its high efficiency, low 80 mΩ $R_{DSON}$ and pad-up package allows the device to output up to 2 × 50 W or 1 × 100 W.

TAS5755M leverages 2 full H-bridges which are used for each channel in stereo mode. In 2.1 mode, TAS5755M runs 2 independent speaker channels using 2 half-bridges while using a full-bridge to drive a subwoofer. Finally, in mono mode, TAS5755M supports pre-filter parallel bridge tied load (PBTL) using only one filter stage to reduce total system size and cost.

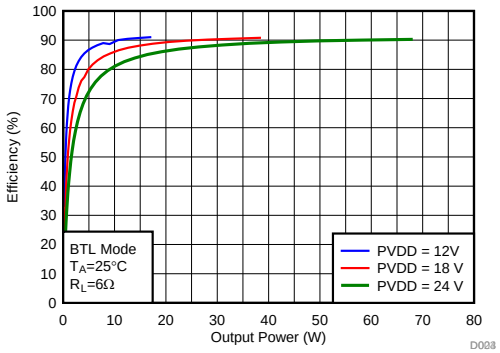
TAS5755M has integrated audio processing. It includes: signal mixing, DC blocking filters, 2 × 8 + 1 × 2 biquads for equalization. Power limiting is implemented by leveraging a two-band log-style DRC and a separate single-band DRC for the subwoofer channel.

**Device Information(1)**

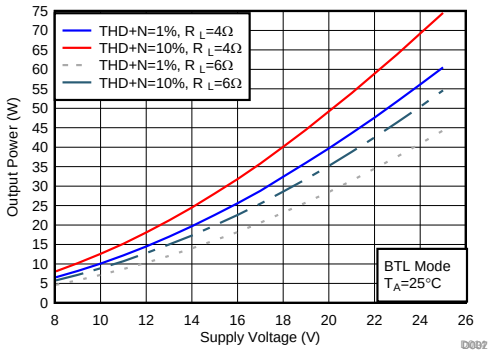
| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TAS5755M | DFD | 14 mm × 6.1 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Efficiency vs Total Output Power**




**Output Power vs Supply Voltage**



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision A (November 2017) to Revision B** — **Page**

- Changed SE Mode, PVDD = 24 V, $R_L$ = 4Ω, 7% THD from 17.1 W to 17.6 W in AC Electrical Characteristics (BTL, PBTL) ... 8
- Changed SE Mode, PVDD = 24 V, $R_L$ = 4Ω, 10% THD from 18.1 W to 19 W in AC Electrical Characteristics (BTL, PBTL) ... 8
- Changed Figure 6 and Figure 7 ... 12
- Changed Figure 19, Figure 20, and Figure 21 ... 15
- Changed Figure 33, Figure 34, and Figure 35 ... 18

**Changes from Original (August 2017) to Revision A** — **Page**

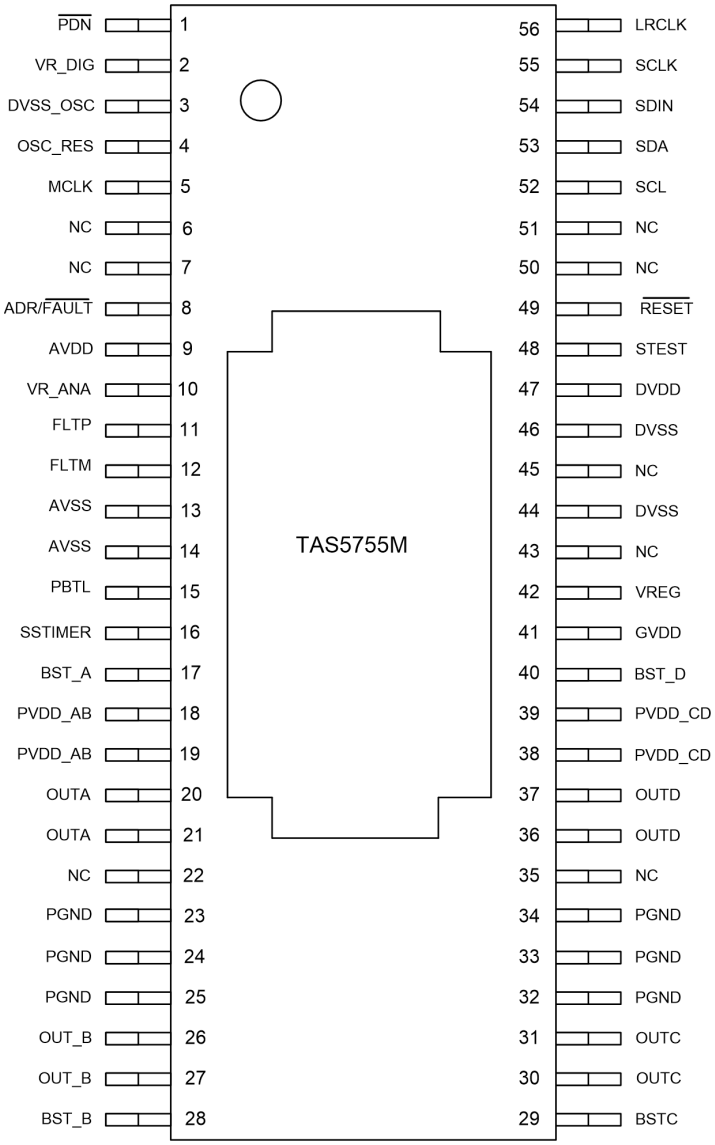
- Released device as Production Data ... 1

# 5 Device Comparison Table

| | TAS5755M | TAS5731M | TAS5729MD | TAS5721 | TAS5717 | TAS5711 |
|---|---|---|---|---|---|---|
| Max Power to Single-Ended Load | 19 | 18 | | 10 | | 16 |
| Max Power to Bridge Tied Load | 50 | 37 | 20 | 15 | 10 | 20 |
| Max Power to Parallel Bridge Tied Load | 100 | 70 | 40 | 30 | | 40 |
| Min Supported Single-Ended Load | 2 | 2 | | 4 | | 4 |
| Min Supported Bridge Tied Load | 4 | 4 | 4 | 8 | 4 | 6 |
| Min Supported Parallel Bridge Tied Load | 2 | 2 | 4 | 4 | | 4 |
| Closed/Open Loop | Open | Open | Open | Open | Open | Open |
| Max Speaker Outputs | 3 | 3 | 2 | 3 | 2 | 3 |
| Headphone Channels | | | Yes | Yes | Yes | |
| Architecture | Class D | Class D | Class D | Class D | Class D | Class D |
| Dynamic Range Control (DRC) | 2-Band | 2-Band | 2-Band AGL | 2-Band | 2-Band AGL | Single-Band |
| Biquads (EQ) | 21 | 21 | 28 | 21 | 28 | 21 |

# 6 Pin Configuration and Functions

**HTSSOP Package**
**56-Pin DFD**
**Top View**




## Pin Functions

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| ADR/FAULT | 8 | DIO | Dual function terminal which sets the LSB of the 7-bit I2C address to "0" if pulled to GND and to "1" if pulled to DVDD. If configured to be a fault output by the methods described in I²C Address Selection and Fault Output, this terminal is pulled low when an internal fault occurs. A pull-up or pull-down resistor is required, as is shown in the Typical Application Circuit Diagrams. If pulled high (to DVDD), a 15-kΩ resistor must be used to minimize in-rush current at power up and to isolate the net if the pin is used as a fault output, as described above. |
| AVDD | 9 | P | 3.3-V analog power supply |
| AVSS | 13,14 | P | Analog 3.3-V supply ground |
| BST_A | 17 | P | High-side bootstrap supply for half-bridge A |
| BST_B | 28 | P | High-side bootstrap supply for half-bridge B |

(1) TYPE: A = analog; D = 3.3-V digital; P = power/ground/decoupling; I = input; O = output

## Pin Functions (continued)

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| BST_C | 29 | P | High-side bootstrap supply for half-bridge C |
| BST_D | 40 | P | High-side bootstrap supply for half-bridge D |
| DVDD | 47 | P | 3.3-V digital power supply |
| DVSS | 44,46 | P | Digital ground |
| DVSS_OSC | 3 | P | Oscillator ground |
| GVDD | 41 | P | Gate drive internal regulator output |
| LRCLK | 56 | P | nput serial audio data left/right clock (sample-rate clock) |
| MCLK | 5 | DI | Master clock input |
| NC | 6,7,22,35, 43,45,50,5 1 | – | No connect |
| OSC_RES | 4 | AO | Oscillator trim resistor. Connect an 18.2-kΩ, 1% resistor to DVSSO. |
| OUT_A | 20,21 | O | Output, half-bridge A |
| OUT_B | 26,27 | O | Output, half-bridge B |
| OUT_C | 30,31 | O | Output, half-bridge C |
| OUT_D | 36,37 | O | Output, half-bridge D |
| PBTL | 15 | DI | Low means BTL mode; high means PBTL mode. Information goes directly to power stage. |
| $\overline{\text{PDN}}$ | 1 | DI | Power down, active-low. $\overline{\text{PDN}}$ prepares the device for loss of power supplies by shutting down the noise shaper and initiating the PWM stop sequence. |
| PGND | 23,24,25, 32,33,34 | P | Power ground for half-bridges A and B |
| FLTM | 12 | AO | PLL negative loop-filter terminal |
| FLTP | 11 | AO | PLL positive loop-filter terminal |
| PVDD_AB | 18,19 | P | Power-supply input for half-bridge output A and B |
| PVDD_CD | 38,39 | P | Power-supply input for half-bridge output C and D |
| $\overline{\text{RESET}}$ | 49 | DI | Reset, active-low. A system reset is generated by applying a logic low to this pin. RESET is an asynchronous control signal that restores the DAP to its default conditions and places the PWM in the hard-mute (high-impedance) state. |
| SCL | 52 | DI | $I^2C$ serial control clock input |
| SCLK | 55 | DI | Serial audio-data clock (shift clock). SCLK is the serial-audio-port input-data bit clock. |
| SDA | 53 | DIO | $I^2C$ serial control data interface input/output |
| SDIN | 54 | DI | Serial audio data input. SDIN supports three discrete (stereo) data formats. |
| SSTIMER | 16 | AI | Controls ramp time of OUT_x to minimize pop. Leave this pin floating for BD mode. Requires capacitor of 2.2 nF to GND in AD mode. The capacitor determines the ramp time. |
| STEST | 48 | DI | Factory test pin. Connect directly to DVSS. |
| VR_ANA | 10 | P | Internally regulated 1.8-V analog supply voltage. This pin must not be used to power external devices. |
| VR_DIG | 2 | P | Internally regulated 1.8-V digital supply voltage. This pin must not be used to power external devices. |
| VREG | 42 | P | Digital regulator output. Not to be used for powering external circuitry. |
| PowerPAD™ | | P | Connect to GND for best system performance. If not connected to GND, leave floating. |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | DVDD, AVDD | –0.3 | 4.2 | V |
| | PVDD_x | –0.3 | 30 | V |
| Input voltage | 3.3-V digital input | –0.5 | DVDD + 0.5 | V |
| | 5-V tolerant(2) digital input (except MCLK) | –0.5 | DVDD + 2.5(3) | |
| | 5-V tolerant MCLK input | –0.5 | AVDD + 2.5(3) | |
| OUT_x to PGND_x | | | 32(4) | V |
| BST_x to PGND_x | | | 39(4) | V |
| Input clamp current, $I_{IK}$ | | –20 | 20 | mA |
| Output clamp current, $I_{OK}$ | | –20 | 20 | mA |
| Operating free-air temperature | | 0 | 85 | °C |
| Operating junction temperature | | 0 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –40 | 125 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) 5-V tolerant inputs are PDN, RESET, SCLK, LRCLK, MCLK, SDIN, SDA, and SCL.
(3) Maximum pin voltage must not exceed 6 V.
(4) DC voltage + peak ac waveform measured at the pin must be below the allowed limit for all conditions.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±250 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Digital/analog supply voltage | DVDD, AVDD | 3 | 3.3 | 3.6 | V |
| | Half-bridge supply voltage | PVDD_x | 8 | | 26.4(1) | V |
| $V_{IH}$ | High-level input voltage | 5-V tolerant | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | 5-V tolerant | | | 0.8 | V |
| $T_A$ | Operating ambient temperature range | | 0 | | 85 | °C |
| $T_J$ (2) | Operating junction temperature range | | 0 | | 125 | °C |
| $R_L$ (PBTL) | Load impedance | Output filter: L = 15 µH, C = 680 nF | 2 | | | Ω |
| $R_L$ (BTL) | Load impedance | Output filter: L = 15 µH, C = 680 nF | 4 | | | Ω |
| $R_L$ (SE) | Load impedance | Output filter: L = 15 µH, C = 680 nF | 2 | | | Ω |
| $L_O$ | Output-filter inductance | Minimum output inductance under short-circuit condition | 10 | | | µH |

(1) For operation at PVDD_x levels greater than 18 V, the modulation limit must be set to 93.8% through the control port register 0x10.
(2) Continuous operation above the recommended junction temperature may result in reduced reliability and/or lifetime of the device.

## 7.4 Thermal Information

| THERMAL METRIC[1] | | TAS5755M DFD HTSSOP 56-PIN | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | — | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 1.13 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | — | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | — | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | — | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 7.5 PWM Operation at Recommended Operating Conditions

| PARAMETER | TEST CONDITIONS | VALUE | UNIT |
|---|---|---|---|
| Output PWM switch frequency | 11.025/22.05/44.1-kHz data rate ±2% | 352.8 | kHz |
| | 48/24/12/8/16/32-kHz data rate ±2% | 384 | |

## 7.6 DC Electrical Characteristics

$T_A$ = 25°, PVDD_x = 18 V, DVDD = AVDD = 3.3 V, $R_L$= 8 Ω, BTL AD mode, $f_S$ = 48 kHz (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | ADR/$\overline{\text{FAULT}}$ and SDA | $I_{OH}$ = –4 mA<br>DVDD = 3 V | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | ADR/$\overline{\text{FAULT}}$ and SDA | $I_{OL}$ = 4 mA<br>DVDD = 3 V | | | 0.5 | V |
| $I_{IL}$ | Low-level input current | | $V_I < V_{IL}$;<br>DVDD = AVDD = 3.6 V | | | 75 | µA |
| $I_{IH}$ | High-level input current | | $V_I > V_{IH}$;<br>DVDD = AVDD = 3.6 V | | | 75[1] | µA |
| $I_{DD}$ | 3.3-V supply current | 3.3-V supply voltage (DVDD, AVDD) | Normal mode | | 49 | 68 | mA |
| | | | Reset ($\overline{\text{RESET}}$ = low, $\overline{\text{PDN}}$ = high) | | 23 | 38 | |
| $I_{PVDD}$ | Supply current | No load (PVDD_x) | Normal mode | | 32 | 50 | mA |
| | | | Reset ($\overline{\text{RESET}}$ = low, $\overline{\text{PDN}}$ = high) | | 4 | 8 | |
| $r_{DS(on)}$ [2] | Drain-to-source resistance, LS | $T_J$ = 25°C, includes metallization resistance | | | 80 | | mΩ |
| | Drain-to-source resistance, HS | $T_J$ = 25°C, includes metallization resistance | | | 80 | | |
| **I/O PROTECTION** | | | | | | | |
| $V_{uvp}$ | Undervoltage protection limit | PVDD falling | | | 6.4 | | V |
| $V_{uvp,hyst}$ | Undervoltage protection limit | PVDD rising | | | 7.1 | | V |
| OTE[3] | Overtemperature error | | | | 150 | | °C |
| $OTE_{HYST}$ [3] | Extra temperature drop required to recover from error | | | | 30 | | °C |
| $I_{OC}$ | Overcurrent limit protection | Output to output short in BTL mode | | | 6 | | A |
| $I_{OCT}$ | Overcurrent response time | | | | 150 | | ns |

(1) $I_{IH}$ for the PBTL pin has a maximum limit of 200 µA due to an internal pulldown on the pin.
(2) This does not include bond-wire or pin resistance.
(3) Specified by design.

## 7.7 AC Electrical Characteristics (BTL, PBTL)

PVDD_x = 18 V, BTL AD mode, $f_S$ = 48 kHz, $R_L$ = 8 Ω, $C_{BST}$ = 10 nF, audio frequency = 1 kHz, AES17 filter, $f_{PWM}$ = 384 kHz, $T_A$ = 25°C (unless otherwise noted). All performance is in accordance with recommended operating conditions (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_O$ | Power output per channel | BTL mode, PVDD = 8 V, $R_L$ = 8 Ω, 7% THD | | 3.9 | | W |
| | | BTL mode, PVDD = 8 V, $R_L$ = 8 Ω,10% THD | | 4.2 | | |
| | | BTL mode, PVDD = 12 V, $R_L$ = 8 Ω, 7% THD | | 8 | | |
| | | BTL mode, PVDD = 12 V, $R_L$ = 8 Ω,10% THD | | 9.6 | | |
| | | BTL mode, PVDD = 18 V, $R_L$ = 8 Ω, 7% THD | | 18.7 | | |
| | | BTL mode, PVDD = 18 V, $R_L$ = 8 Ω, 10% THD | | 21.2 | | |
| | | BTL mode, PVDD = 24 V, $R_L$ = 8 Ω, 7% THD | | 32.6 | | |
| | | BTL mode, PVDD = 24 V, $R_L$ = 8 Ω, 10% THD | | 37.2 | | |
| | | BTL mode, PVDD = 24 V, $R_L$ = 6 Ω, 10% THD | | 50 | | |
| | | PBTL mode, PVDD = 12 V, $R_L$ = 4 Ω, 7% THD | | 16.5 | | |
| | | PBTL mode, PVDD = 12 V, $R_L$ = 4 Ω, 10% THD | | 17.9 | | |
| | | PBTL mode, PVDD = 18 V, $R_L$ = 4 Ω, 7% THD | | 37 | | |
| | | PBTL mode, PVDD = 18 V, $R_L$ = 4 Ω, 10% THD | | 39.6 | | |
| | | PBTL mode, PVDD = 24 V, $R_L$ = 4 Ω, 10% THD | | 66 | | |
| | | PBTL mode, PVDD = 24 V, $R_L$ = 4 Ω, 10% THD | | 69.6 | | |
| | | SE Mode, PVDD = 12 V, RL = 4 Ω, 7% THD | | 4.2 | | |
| | | SE Mode, PVDD = 12 V, RL = 4 Ω, 10% THD | | 4.6 | | |
| | | SE Mode, PVDD = 18 V, RL = 4 Ω, 7% THD | | 9.6 | | |
| | | SE Mode, PVDD = 18 V, RL = 4 Ω, 10% THD | | 10.2 | | |
| | | SE Mode, PVDD = 24 V, RL = 4 Ω, 7% THD | | 17.6 | | |
| | | SE Mode, PVDD = 24 V, RL = 4 Ω, 10% THD | | 19 | | |
| THD+N | Total harmonic distortion + noise | PVDD = 8 V, $P_O$ = 1 W | | 0.15% | | |
| | | PVDD = 12 V, $P_O$ = 1 W | | 0.03% | | |
| | | PVDD = 18 V, $P_O$ = 1 W | | 0.04% | | |
| | | PVDD = 24 V, $P_O$ = 1 W | | 0.1% | | |
| $V_n$ | Output integrated noise (rms) | A-weighted | | 46 | | μV |
| | Cross-talk | $P_O$ = 0.25 W, f = 1 kHz (AD Mode) | | –67 | | dB |
| SNR | Signal-to-noise ratio(1) | A-weighted, f = 1 kHz, maximum power at THD < 1% | | 104 | | dB |

(1) SNR is calculated relative to 0-dBFS input level.

## 7.8 Electrical Characteristics - PLL External Filter Components

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| External PLL filter capacitor C1 | SMD 0603 X7R | | 47 | | nF |
| External PLL filter capacitor C2 | SMD 0603 X7R | | 4.7 | | nF |
| External PLL filter resistor R | SMD 0603, metal film | | 470 | | Ω |

## 7.9 Electrical Characteristic - I²C Serial Control Port Operation

for I²C Interface signals over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $C_L$ | Load capacitance for each bus line | | | | 400 | pF |

## 7.10 Timing Requirements - PLL Input Parameters

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{MCLKI}$ | MCLK frequency | 2.8224 | | 24.576 | MHz |
| | MCLK duty cycle | 40% | 50% | 60% | |
| $t_r/t_{f(MCLK)}$ | Rise/fall time for MCLK | | | 5 | ns |
| | LRCLK allowable drift before LRCLK reset | | | 4 | MCLKs |

## 7.11 Timing Requirements - Serial Audio Ports Slave Mode

over recommended operating conditions (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SCLKIN}$ | Frequency, SCLK 32 × $f_S$, 48 × $f_S$, 64 × $f_S$ | $C_L$ = 30 pF | 1.024 | | 12.288 | MHz |
| $t_{su1}$ | Setup time, LRCLK to SCLK rising edge | | 10 | | | ns |
| $t_{h1}$ | Hold time, LRCLK from SCLK rising edge | | 10 | | | ns |
| $t_{su2}$ | Setup time, SDIN to SCLK rising edge | | 10 | | | ns |
| $t_{h2}$ | Hold time, SDIN from SCLK rising edge | | 10 | | | ns |
| | LRCLK frequency | | 8 | 48 | 48 | kHz |
| | SCLK duty cycle | | 40% | 50% | 60% | |
| | LRCLK duty cycle | | 40% | 50% | 60% | |
| | SCLK rising edges between LRCLK rising edges | | 32 | | 64 | SCLK edges |
| $t_{(edge)}$ | LRCLK clock edge with respect to the falling edge of SCLK | | –1/4 | | 1/4 | SCLK period |
| $t_r/t_f$ | Rise/fall time for SCLK/LRCLK | | | | 8 | ns |

## 7.12 Timing Requirements - I²C Serial Control Port Operation

for I²C Interface signals over recommended operating conditions (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | Frequency, SCL | No wait states | | | 400 | kHz |
| $t_{w(H)}$ | Pulse duration, SCL high | | 0.6 | | | µs |
| $t_{w(L)}$ | Pulse duration, SCL low | | 1.3 | | | µs |
| $t_r$ | Rise time, SCL and SDA | | | | 300 | ns |
| $t_f$ | Fall time, SCL and SDA | | | | 300 | ns |
| $t_{su1}$ | Setup time, SDA to SCL | | 100 | | | ns |
| $t_{h1}$ | Hold time, SCL to SDA | | 0 | | | ns |
| $t_{(buf)}$ | Bus free time between stop and start conditions | | 1.3 | | | µs |
| $t_{su2}$ | Setup time, SCL to start condition | | 0.6 | | | µs |
| $t_{h2}$ | Hold time, start condition to SCL | | 0.6 | | | µs |
| $t_{su3}$ | Setup time, SCL to stop condition | | 0.6 | | | µs |

## 7.13 Timing Requirements - Reset ($\overline{\text{RESET}}$)

Control signal parameters over recommended operating conditions (unless otherwise noted).

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{w(RESET)}$ | Pulse duration, $\overline{\text{RESET}}$ active | 100 | | | µs |
| $t_{d(I2C\_ready)}$ | Time to enable I²C | | | 12 | ms |

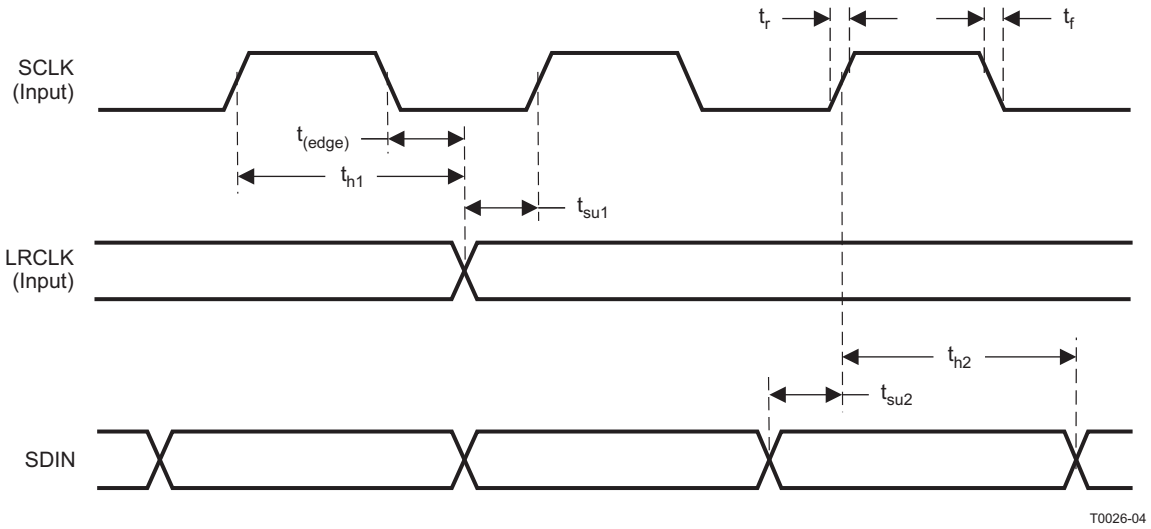



**Figure 1. Slave-Mode Serial Data-Interface Timing**

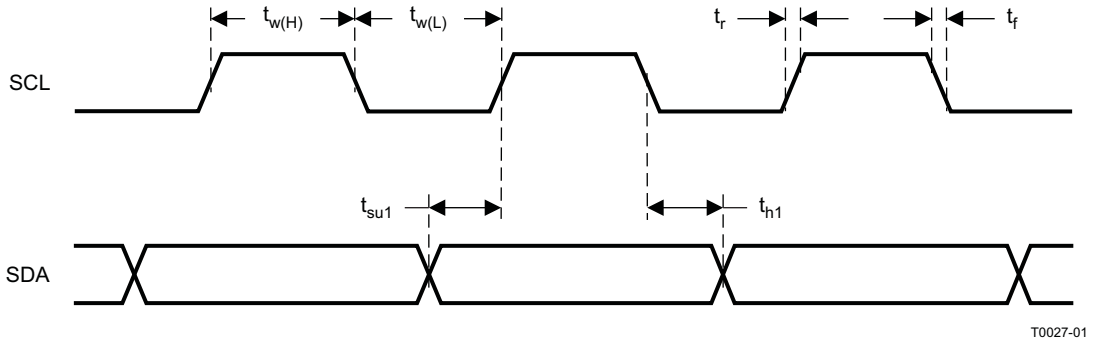



**Figure 2. SCL and SDA Timing**

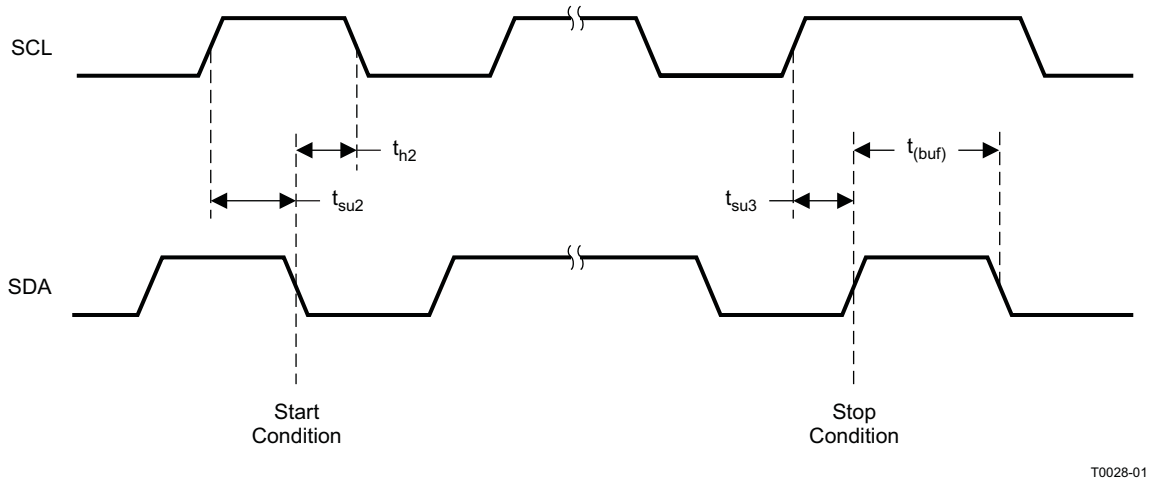
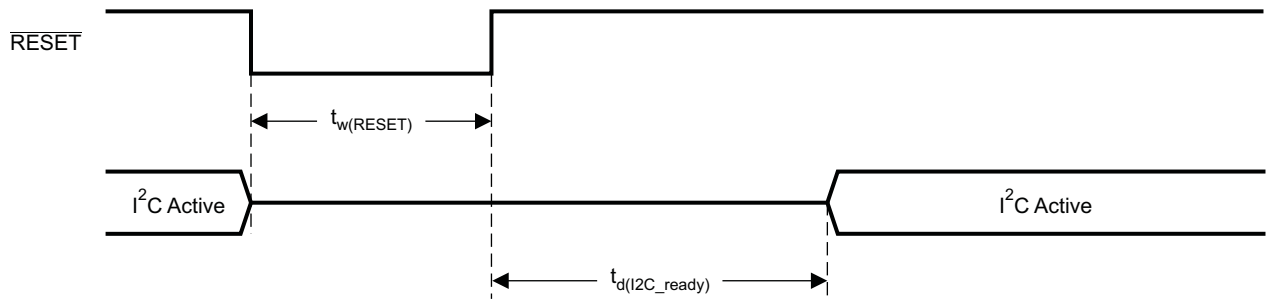



**Figure 3. Start and Stop Conditions Timing**




NOTES: On power up, it is recommended that the TAS5755M $\overline{\text{RESET}}$ be held LOW for at least 100 μs after DVDD has reached 3 V.
If $\overline{\text{RESET}}$ is asserted LOW while $\overline{\text{PDN}}$ is LOW, then $\overline{\text{RESET}}$ must continue to be held LOW for at least 100 μs after $\overline{\text{PDN}}$ is deasserted (HIGH).

**Figure 4. Reset Timing**

## 7.14 Typical Characteristics

### 7.14.1 Typical Characteristics, 2.1 SE Configuration

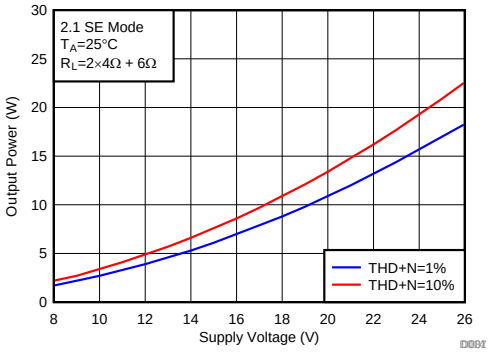



**Figure 5. Output Power vs Supply Voltage**

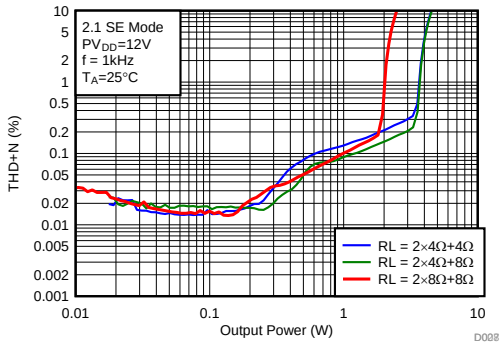



**Figure 6. Total Harmonic Distortion + Noise vs Output Power**

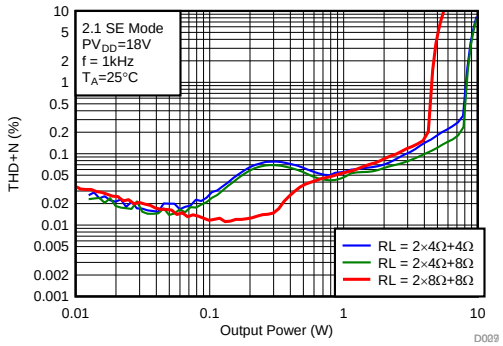



**Figure 7. Total Harmonic Distortion + Noise vs Output Power**

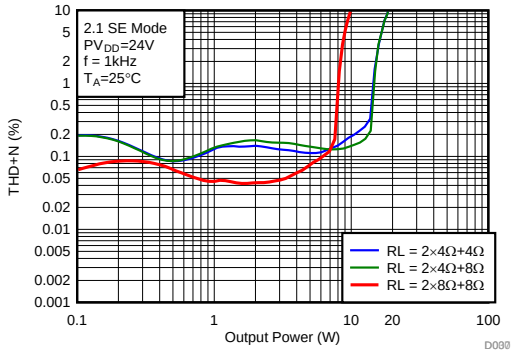



**Figure 8. Total Harmonic Distortion + Noise vs Output Power**

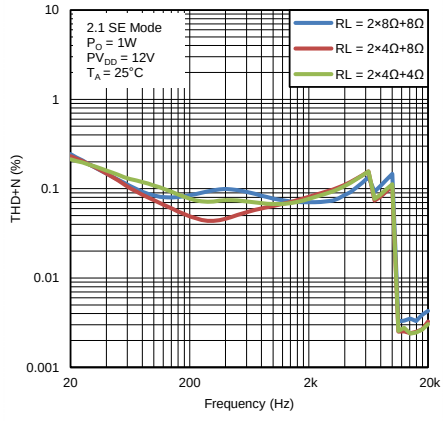



**Figure 9. Total Harmonic Distortion + Noise vs Frequency**

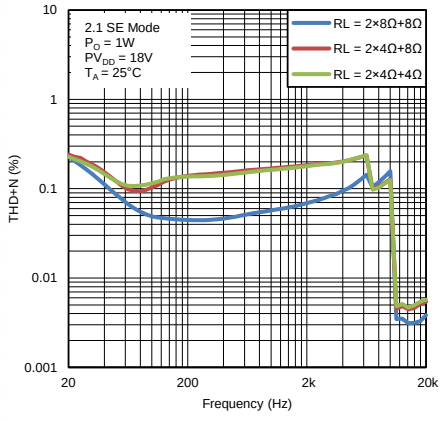



**Figure 10. Total Harmonic Distortion + Noise vs Frequency**

## Typical Characteristics, 2.1 SE Configuration (continued)

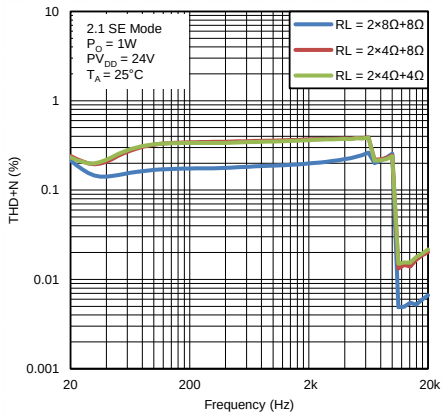



**Figure 11. Total Harmonic Distortion + Noise vs Frequency**

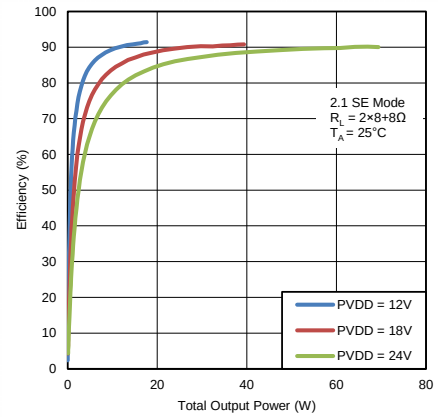



**Figure 12. Efficiency vs Total Output Power**

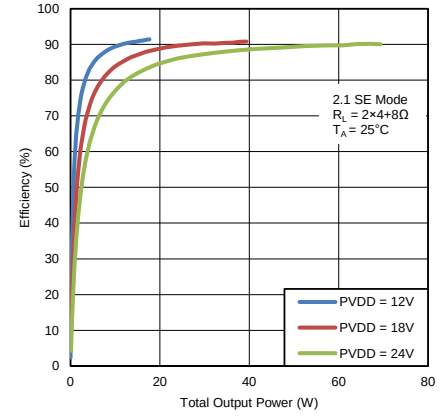



**Figure 13. Efficiency vs Total Output Power**

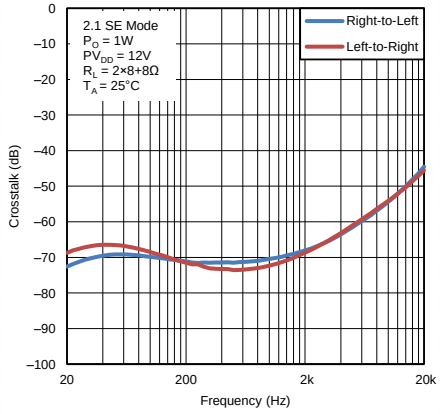



**Figure 14. Crosstalk vs Frequency**

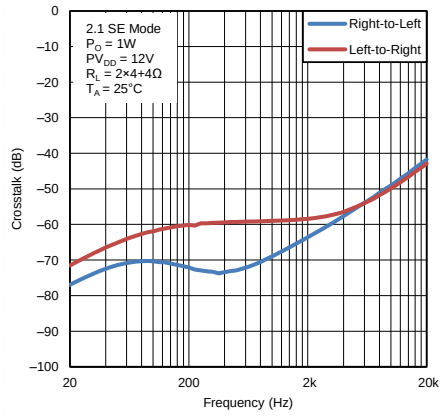



**Figure 15. Crosstalk vs Frequency**

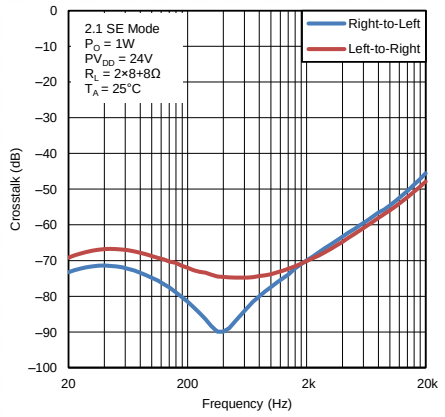



**Figure 16. Crosstalk vs Frequency**

## Typical Characteristics, 2.1 SE Configuration (continued)

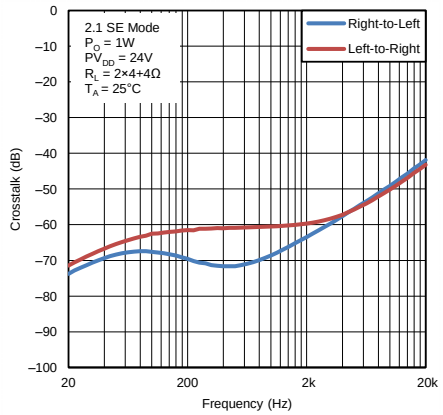



**Figure 17. Crosstalk vs Frequency**

### 7.14.2 Typical Characteristics, 2.0 BTL Configuration

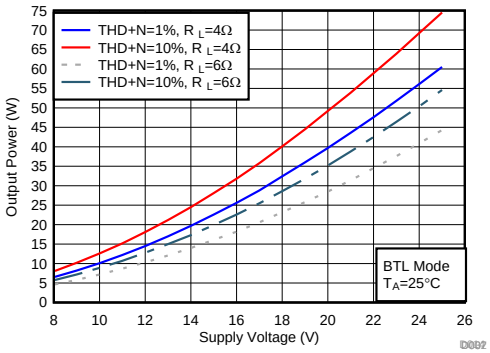



**Figure 18. Output Power vs Supply Voltage**

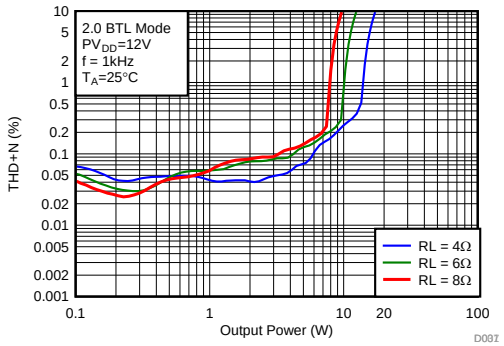



**Figure 19. Total Harmonic Distortion + Noise vs Output Power**

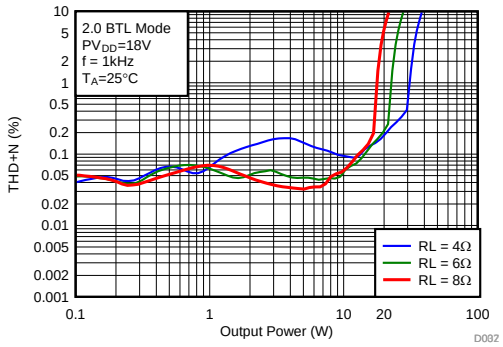



**Figure 20. Total Harmonic Distortion + Noise vs Output Power**

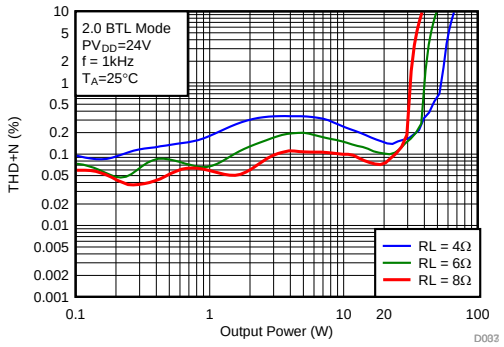



**Figure 21. Total Harmonic Distortion + Noise vs Output Power**

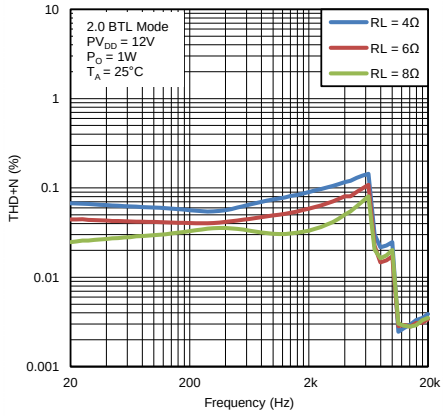



**Figure 22. Total Harmonic Distortion vs Frequency**

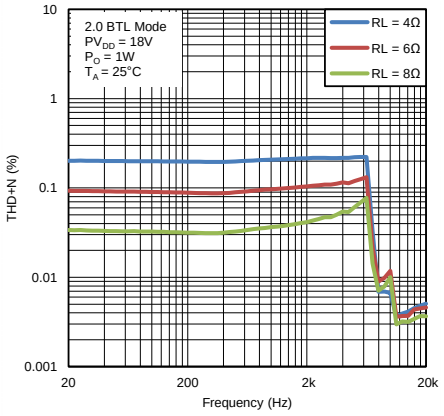



**Figure 23. Total Harmonic Distortion vs Frequency**

## Typical Characteristics, 2.0 BTL Configuration (continued)

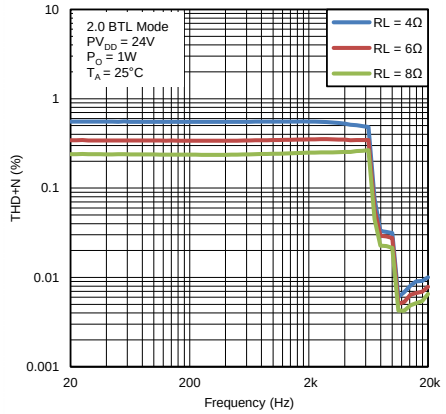



**Figure 24. Total Harmonic Distortion vs Frequency**

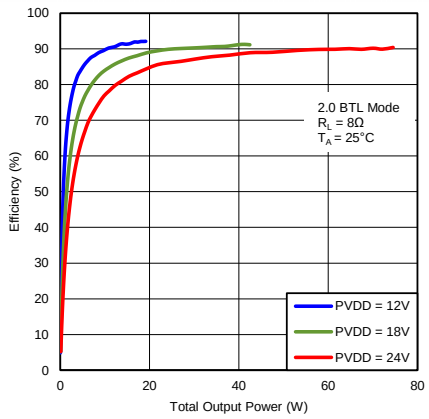



**Figure 25. Efficiency vs Output Power**

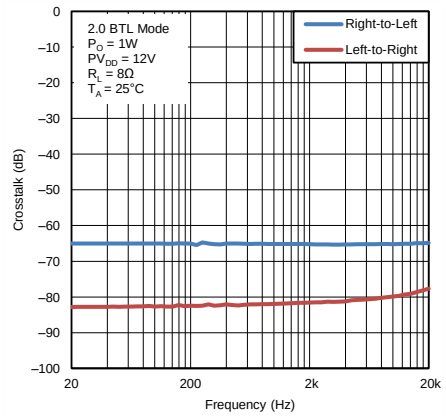



**Figure 26. Crosstalk vs Frequency**

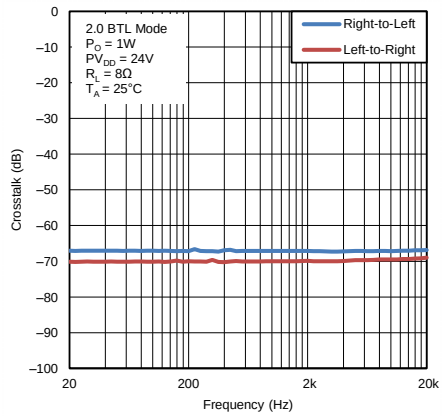



**Figure 27. Crosstalk vs Frequency**

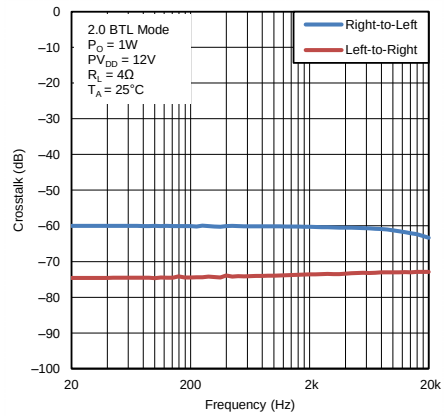



**Figure 28. Crosstalk vs Frequency**

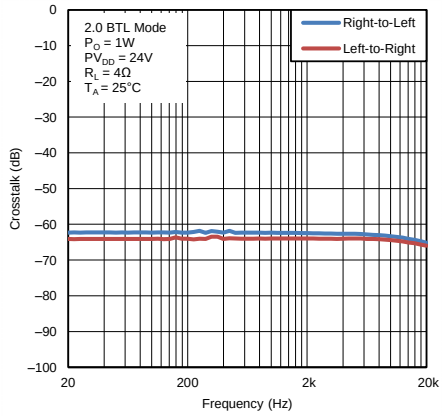



**Figure 29. Crosstalk vs Frequency**

## Typical Characteristics, 2.0 BTL Configuration (continued)

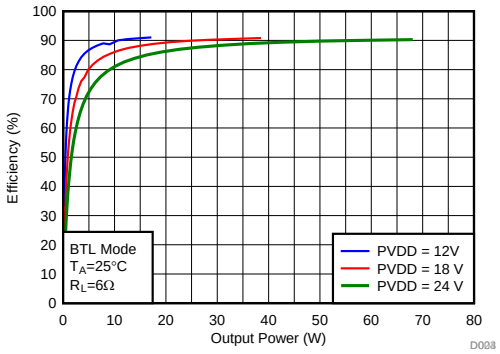



**Figure 30. Power vs Supply Voltage**

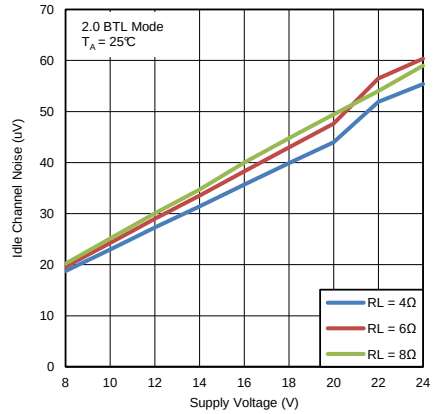



**Figure 31. Idle Channel Noise vs Supply Voltage**

### 7.14.3 Typical Characteristics, PBTL Configuration

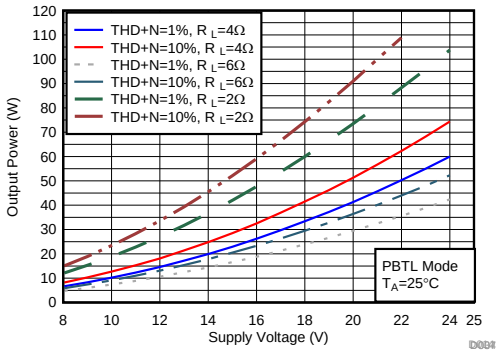



**Figure 32. Output Power vs Supply Voltage**

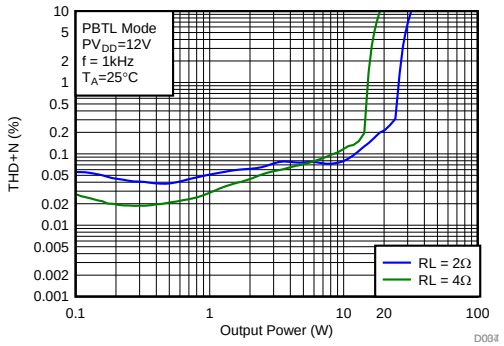



**Figure 33. Total Harmonic Distortion + Noise vs Output Power (PBTL Mode)**

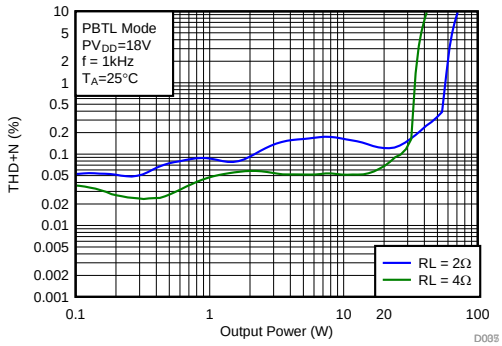



**Figure 34. Total Harmonic Distortion + Noise vs Output Power (PBTL Mode)**

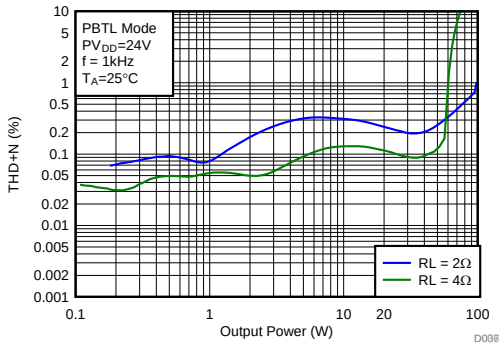



**Figure 35. Total Harmonic Distortion + Noise vs Output Power (PBTL Mode)**

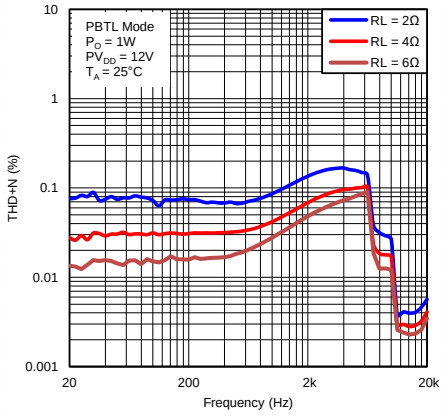



**Figure 36. Total Harmonic Distortion vs Frequency (PBTL Mode)**

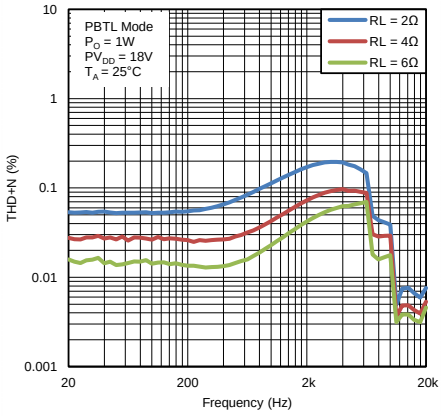



**Figure 37. Total Harmonic Distortion vs Frequency (PBTL Mode)**

## Typical Characteristics, PBTL Configuration (continued)

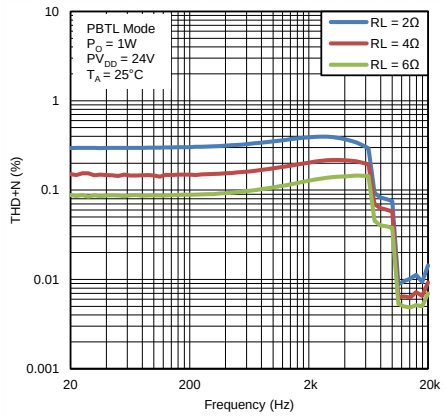



**Figure 38. Total Harmonic Distortion vs Frequency (PBTL Mode)**

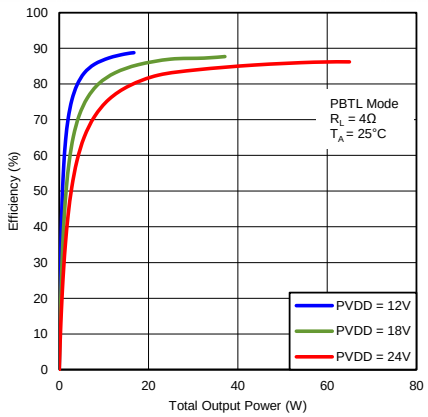



**Figure 39. Efficiency vs Output Power (PBTL Mode)**

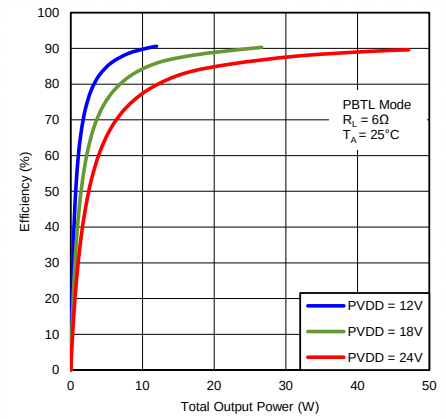



**Figure 40. Efficiency vs Output Power (PBTL Mode)**

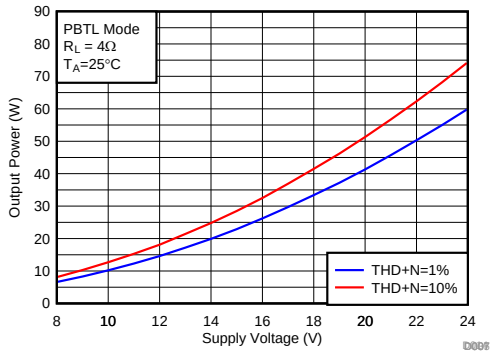



**Figure 41. Power vs Supply Voltage (PBTL Mode)**

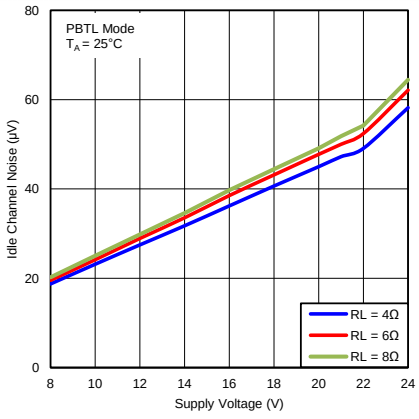



**Figure 42. Idle Channel Noise vs Supply Voltage (PBTL Mode)**

# 8 Parameter Measurement Information

All parameters are measured according to the conditions described in the *Specifications* section.

# 9 Detailed Description

## 9.1 Overview

The TAS5755M an efficient 50-W stereo $I^2S$ input Class-D audio power amplifier. The digital auto processor of the device uses noise shaping and customized correction algorithms to achieve a great power efficiency and high audio performance. Also, the device has up to eight Equalizers per channel and two -band configurable Dynamic Range Control (DRC).

The device needs only a single DVDD supply in addition to the higher-voltage PVDD power supply. An internal voltage regulator provides suitable voltage levels for the gate drive circuit. The wide PVDD power supply range of the device enables its use in a multitude of applications.

The TAS5755M is a slave-only device that is controlled by a bidirectional $I^2C$ interface that supports both 100-kHz and 400-kHz data transfer rates for single- and multiple-byte write and read operations. This control interface is used to program the registers of the device and read the device status.

The PWM of this device operates with a carrier frequency between 384 kHz and 354 kHz, depending the sampling rate. This device allows the use of the same clock signal for both MCLK and BCLK (64xFs) when using a sampling frequency of 44.1 kHz or 48 kHz.

This device can be used in three different modes of operation, Stereo BTL mode, Single filter PBTL mono mode, and 2.1 mode.

## 9.2 Functional Block Diagrams

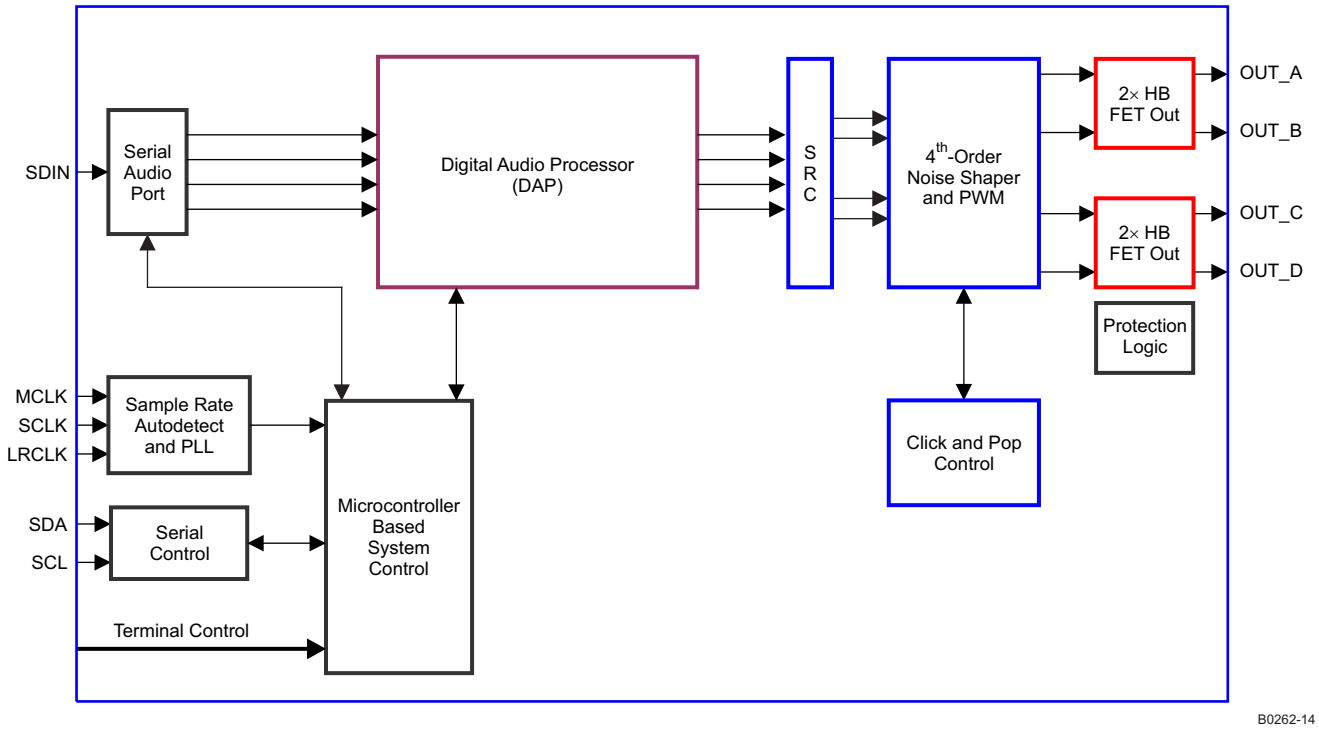



**Figure 43. Functional Block Diagram**

## Functional Block Diagrams (continued)

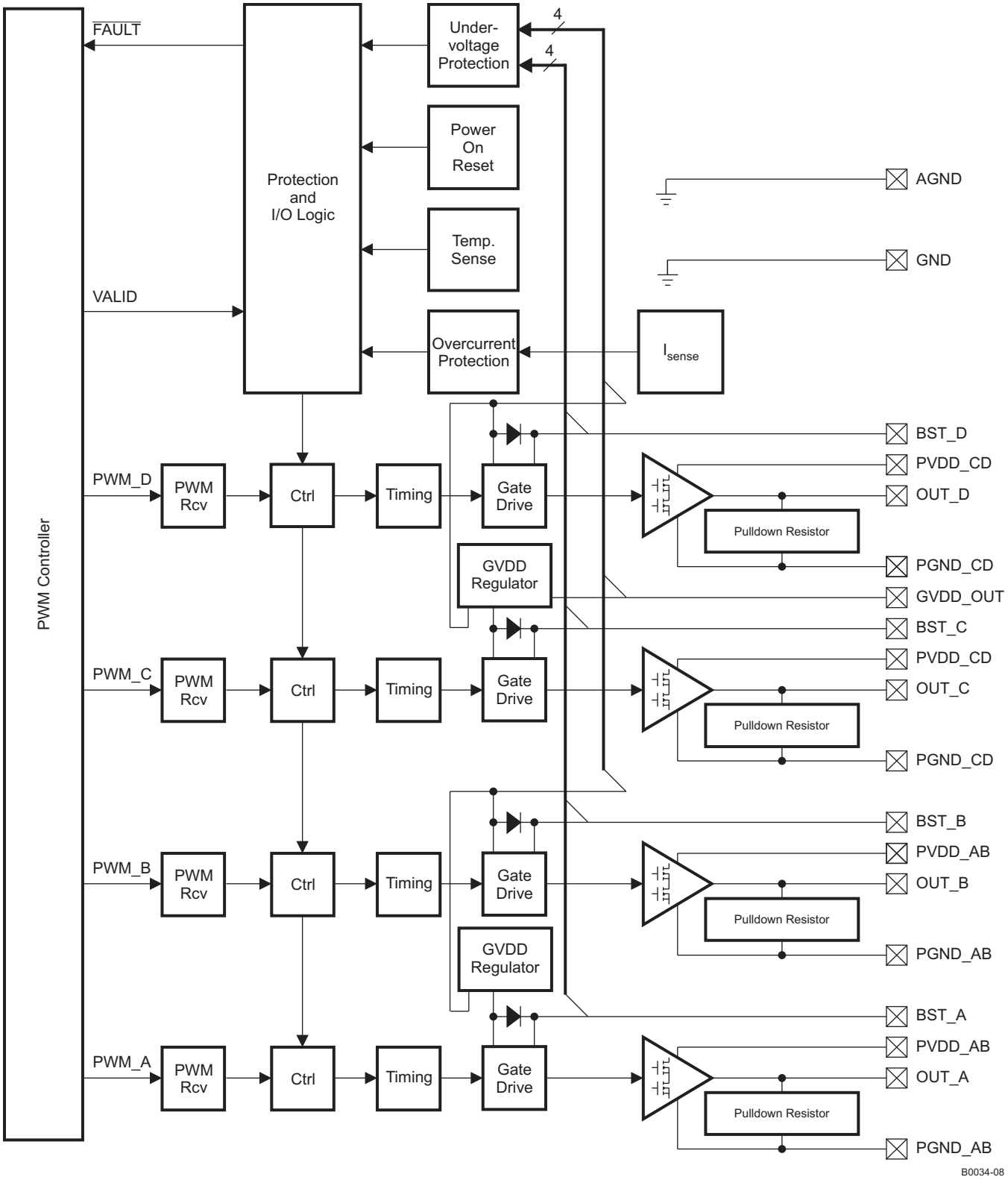



**Figure 44. Power-Stage Functional Block Diagram**

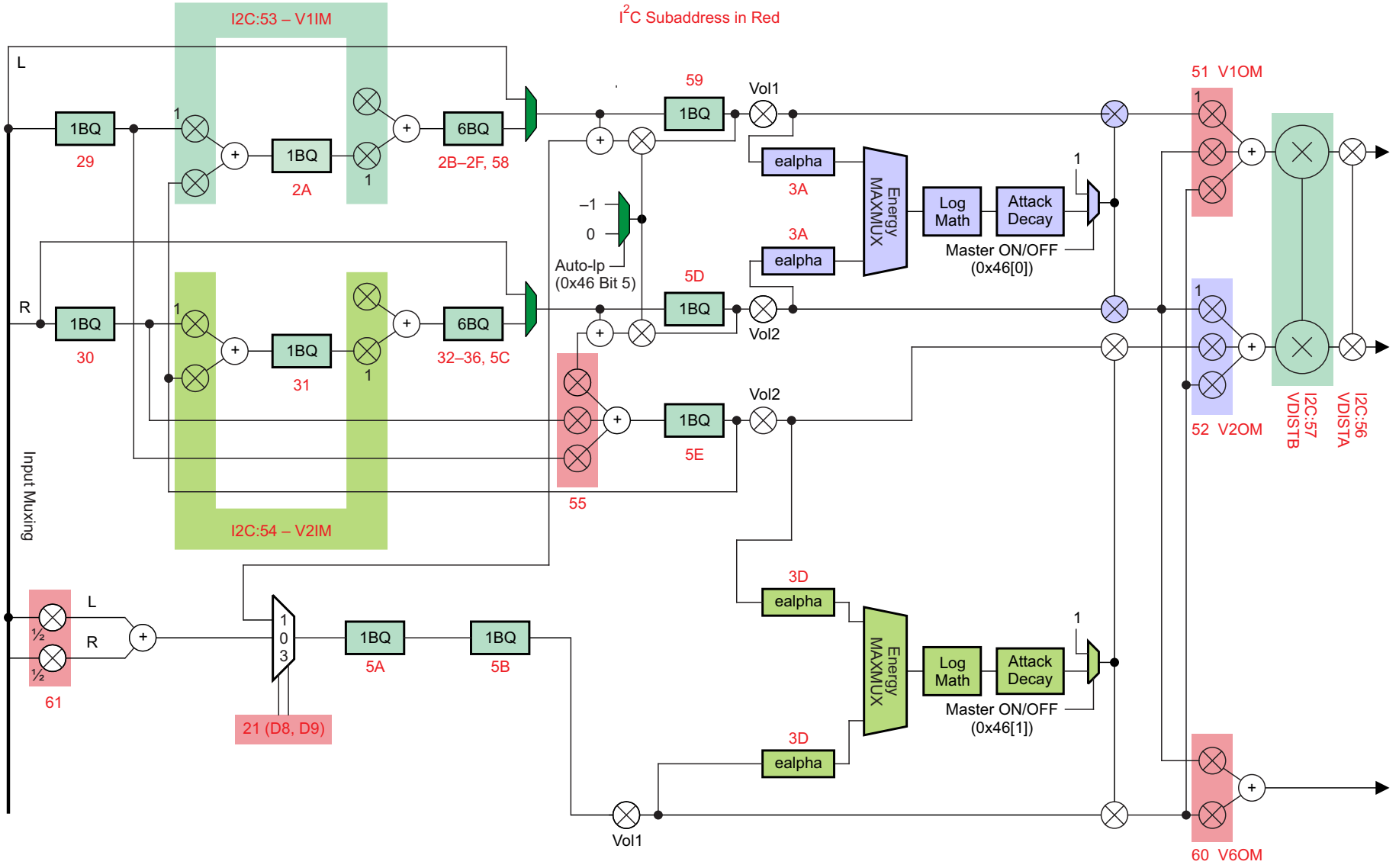



**Figure 45. DAP Process Structure**

## 9.3 Feature Description

### 9.3.1 Power Supply

To facilitate system design, the TAS5755M needs only a 3.3-V supply in addition to the PVDD power-stage supply. An internal voltage regulator provides suitable voltage levels for the gate drive circuitry. Additionally, all circuitry requiring a floating voltage supply, for example, the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors.

In order to provide good electrical and acoustical characteristics, the PWM signal path for the output stage is designed as identical half-bridges with separate bootstrap pins (BST_x). The gate-drive voltage (GVDD_OUT) is derived from the PVDD voltage. Special attention must be paid to placing all decoupling capacitors as close to their associated pins as possible. Inductance between the power-supply pins and decoupling capacitors must be avoided.

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_x) to the power-stage output pin (OUT_x). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive regulator output pin (GVDD_OUT) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 288 kHz to 384 kHz, it is recommended to use 10-nF, X7R ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 10-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power-stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle.

Special attention must be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pins (PVDD_x). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_x pin is decoupled with a 100-nF, X7R ceramic capacitor placed as close as possible to each supply pin.

The TAS5755M is fully protected against erroneous power-stage turnon due to parasitic gate charging.

### 9.3.2 $I^2C$ Address Selection and Fault Output

ADR/$\overline{\text{FAULT}}$ is an input pin during power up. It can be pulled HIGH or LOW through a resistor as shown in the *Typical Applications* sections in order to set the $I^2C$ address. Pulling this pin HIGH through the resistor results in setting the $I^2C$ 7-bit address to 0011011 (0x36), and pulling it LOW through the resistor results in setting the address to 0011010 (0x34).

During power up, the address of the device is latched in, freeing up the ADR/$\overline{\text{FAULT}}$ pin to be used as a fault notification output. When configured as a fault output, the pin will go low when a fault occurs and will return to its default state when register 0x02 is cleared. The behavior of the pin in response to a fault condition is to be pulled low immediately upon an error. The device then waits for a period of time determined by BKND_ERR Register (0x1C) before attempting to resume playback. If the error has been cleared when the device attempts to resume playback, playback will resume, the ADR/$\overline{\text{FAULT}}$ pin will remain high, and normal operation will resume. If the error has not been removed, then the device will immediately re-enter the protected state and wait again for the predetermined period of time to pass. The device will pull the fault pin low for over-current, over-temperature, and under-voltage lock-out.

### 9.3.3 Single-Filter PBTL Mode

The TAS5755M supports parallel BTL (PBTL) mode with OUT_A/OUT_B (and OUT_C/OUT_D) connected before the LC filter. In addition to connecting OUT_A/OUT_B and OUT_C/OUT_D, BST_A/BST_B and BST_C/BST_D must also be connected before the LC filter, as shown in the Figure 71. In order to put the part in PBTL configuration, drive PBTL (pin 8) HIGH. This synchronizes the turnoff of half-bridges A and B (and similarly C/D) if an overcurrent condition is detected in either half-bridge. There is a pulldown resistor on the PBTL pin that configures the part in BTL mode if the pin is left floating.

PWM output multiplexers register (0x25) and PWM Shutdown Group Register (0x19) must be updated to set the device in PBTL mode. Must follow one of below listed configurations for PBTL mode.

- Register (0x25) be written with a value of 0x0110 3245, Register (0x19) be written with a value of 0x35
- Register (0x25) be written with a value of 0x0101 2345, Register (0x19) be written with a value of 0x3A

.

## Feature Description (continued)

### 9.3.4 Device Protection System

#### *9.3.4.1 Overcurrent (OC) Protection With Current Limiting*

The device has independent, fast-reacting current detectors on all high-side and low-side power-stage FETs. The detector outputs are closely monitored by a protection system. If the high-current condition situation persists, that is, the power stage is being overloaded, a protection system triggers a latching shutdown, resulting in the power stage being set in the high-impedance (Hi-Z) state. The device returns to normal operation once the fault condition (that is, a short circuit on the output) is removed. Current-limiting and overcurrent protection are not independent for half-bridges. That is, if the bridge-tied load between half-bridges A and B causes an overcurrent fault, half-bridges A, B, C, and D are shut down.

#### *9.3.4.2 Overtemperature Protection*

The TAS5755M has an overtemperature-protection system. If the device junction temperature exceeds 150°C (nominal), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state. The TAS5755M recovers automatically once the temperature drops approximately 30°C.

#### *9.3.4.3 Undervoltage Protection (UVP) and Power-On Reset (POR)*

The UVP and POR circuits of the TAS5755M fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the PVDD and AVDD supply voltages reach 7.6 V and 2.7 V, respectively. Although PVDD and AVDD are independently monitored, a supply-voltage drop below the UVP threshold on AVDD or either PVDD pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state.

### 9.3.5 SSTIMER Functionality

The SSTIMER pin uses a capacitor connected between this pin and ground to control the output duty cycle when exiting all-channel shutdown. The capacitor on the SSTIMER pin is slowly charged through an internal current source, and the charge time determines the rate at which the output transitions from a near-zero duty cycle to the desired duty cycle. This allows for a smooth transition that minimizes audible pops and clicks. When the part is shut down, the drivers are placed in the high-impedance state and transition slowly down through a 3-kΩ resistor, similarly minimizing pops and clicks. The shutdown transition time is independent of the SSTIMER pin capacitance. Larger capacitors increase the start-up time, while capacitors smaller than 2.2 nF decrease the start-up time. The SSTIMER pin can be left floating for BD modulation.

### 9.3.6 Clock, Autodetection, and PLL

The TAS5755M is an $I^2S$ slave device. It accepts MCLK, SCLK, and LRCLK. The digital audio processor (DAP) supports all the sample rates and MCLK rates that are defined in the *Clock Control Register (0x00)*.

The TAS5755M checks to verify that SCLK is a specific value of 32 $f_S$, 48 $f_S$, or 64 $f_S$. The DAP only supports a 1 × $f_S$ LRCLK. The timing relationship of these clocks to SDIN is shown in subsequent sections. The clock section uses MCLK or the internal oscillator clock (when MCLK is unstable, out of range, or absent) to produce the internal clock (DCLK) running at 512 times the PWM switching frequency.

The DAP can autodetect and set the internal clock control logic to the appropriate settings for all supported clock rates as defined in the clock-control register.

The TAS5755M has robust clock error handling that uses the built-in trimmed oscillator clock to quickly detect changes/errors. Once the system detects a clock change/error, it mutes the audio (through a single-step mute) and then forces PLL to limp using the internal oscillator as a reference clock. Once the clocks are stable, the system autodetects the new rate and reverts to normal operation. During this process, the default volume is restored in a single step (also called hard unmute). The ramp process can be programmed to ramp back slowly (also called soft unmute) as defined in volume register (0x0E).

## Feature Description (continued)

### 9.3.7 PWM Section

The TAS5755M DAP device uses noise-shaping and customized nonlinear correction algorithms to achieve high power efficiency and high-performance digital audio reproduction. The DAP uses a fourth-order noise shaper to increase dynamic range and SNR in the audio band. The PWM section accepts 24-bit PCM data from the DAP and outputs two BTL PWM audio output channels.

The PWM section has individual-channel dc-blocking filters that can be enabled and disabled. The filter cutoff frequency is less than 1 Hz. Individual-channel de-emphasis filters for 44.1 kHz and 48 kHz are included and can be enabled and disabled.

Finally, the PWM section has an adjustable maximum modulation limit of 93.8% to 99.2%.

For a detailed description of using audio processing features like DRC and EQ, see the *TAS5755EVM User's Guide* (SLOU481) and *TAS570X GDE Software Setup* development tool documentation (SLOC124).

### 9.3.8 2.1-Mode Support

The TAS5755M uses a special mid-Z ramp sequence to reduce click and pop in SE-mode and 2.1-mode operation. To enable the mid-Z ramp, register 0x05 bit D7 must be set to 1. To enable 2.1 mode, register 0x05 bit D2 must be set to 1. The SSTIMER pin must be left floating in this mode.

### 9.3.9 $I^2C$ Compatible Serial Control Interface

The TAS5755M DAP has an $I^2C$ serial control slave interface to receive commands from a system controller. The serial control interface supports both normal-speed (100 kHz) and high-speed (400 kHz) operations without wait states. As an added feature, this interface operates even if MCLK is absent. The serial control interface supports both single-byte and multiple-byte read and write operations for status registers and the general control registers associated with the PWM.

### 9.3.10 Audio Serial Interface

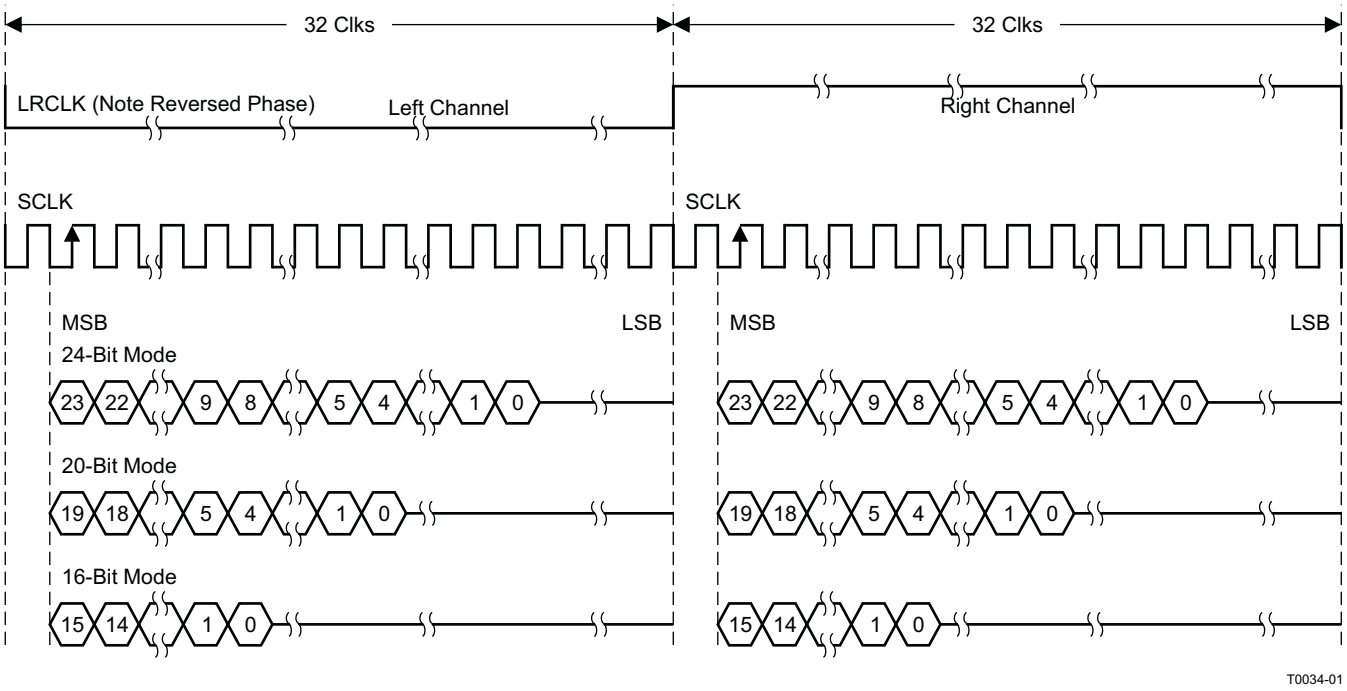
Serial data is input on SDIN. The PWM outputs are derived from SDIN. The TAS5755M DAP accepts serial data in 16-, 20-, or 24-bit left-justified, right-justified, and $I^2S$ serial data formats.

#### *9.3.10.1 $I^2S$ Timing*

$I^2S$ timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is low for the left channel and high for the right channel. A bit clock running at 32, 48, or 64 × $f_S$ is used to clock in the data. There is a delay of one bit clock from the time the LRCLK signal changes state to the first bit of data on the data lines. The data is written MSB-first and is valid on the rising edge of bit clock. The DAP masks unused trailing data bit positions.

## Feature Description (continued)

2-Channel I$^2$S (Philips Format) Stereo Input

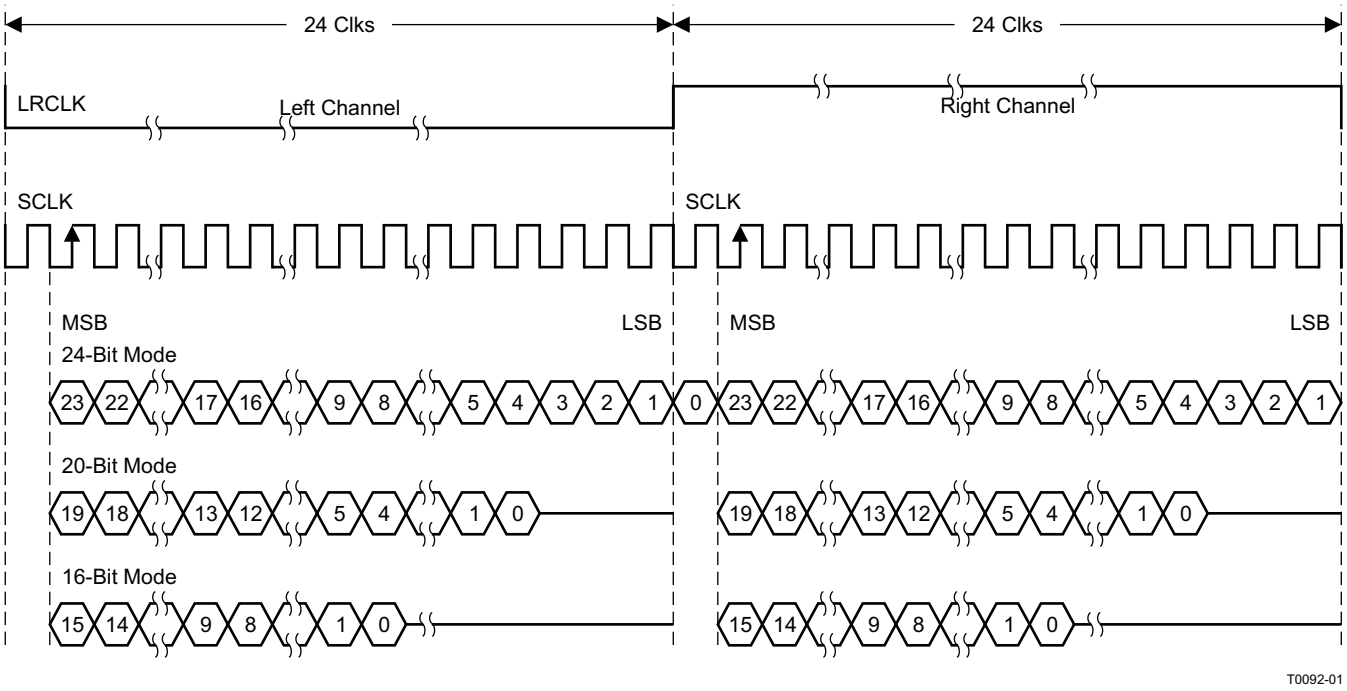



NOTE: All data presented in 2s-complement form with MSB first.

**Figure 46. I$^2$S 64-F$_S$ Format**

## Feature Description (continued)

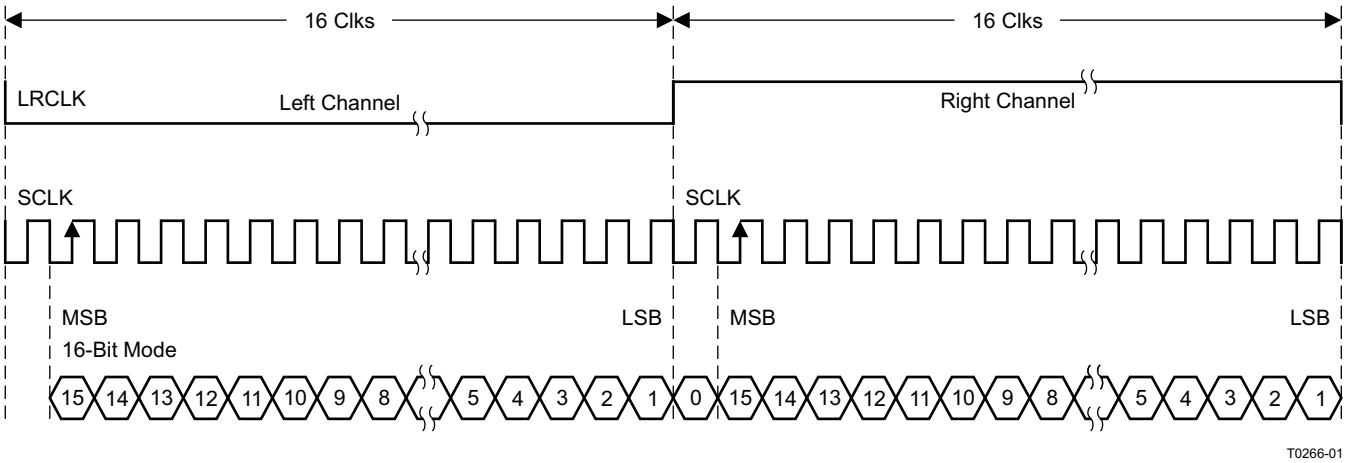
2-Channel I$^2$S (Philips Format) Stereo Input/Output (24-Bit Transfer Word Size)




NOTE: All data presented in 2s-complement form with MSB first.

**Figure 47. I$^2$S 48-$F_S$ Format**

2-Channel I$^2$S (Philips Format) Stereo Input



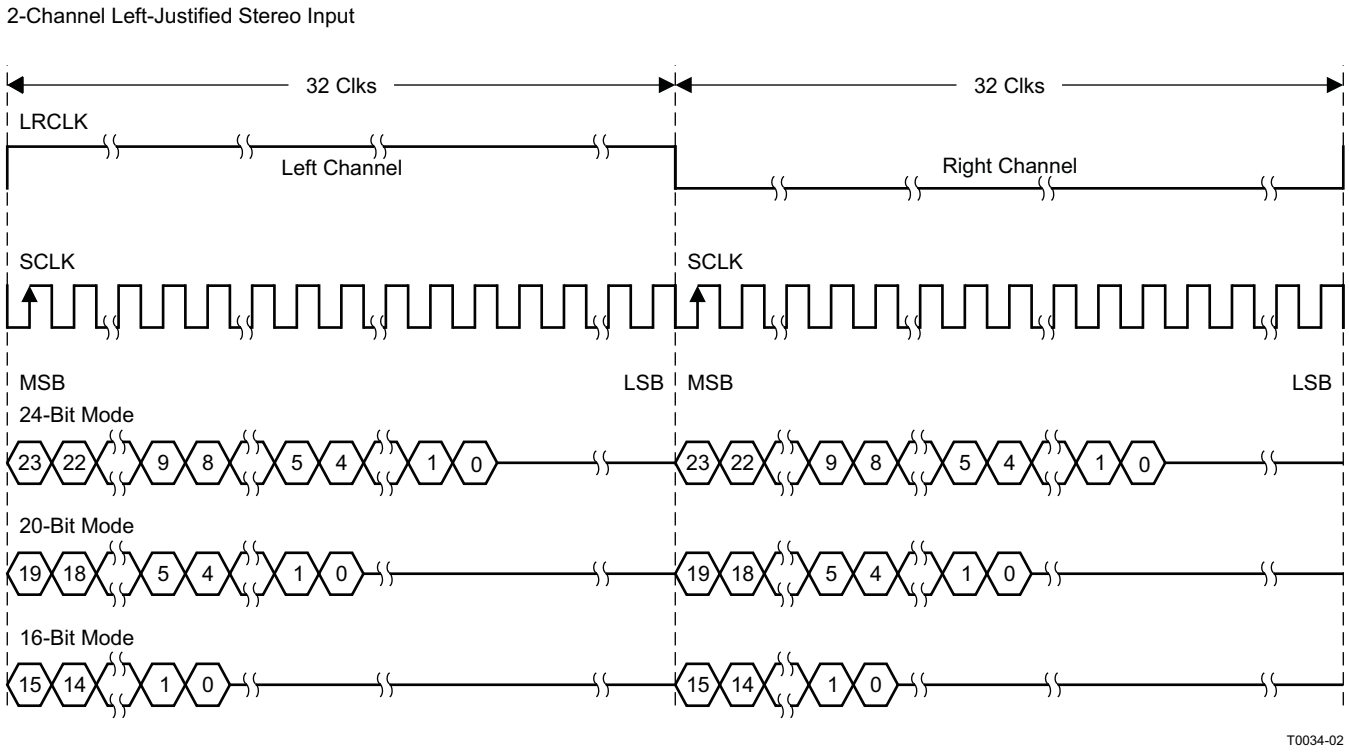

NOTE: All data presented in 2s-complement form with MSB first.

**Figure 48. I$^2$S 32-$F_S$ Format**

## Feature Description (continued)

### 9.3.10.2 Left-Justified

Left-justified (LJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at 32, 48, or 64 × $f_S$ is used to clock in the data. The first bit of data appears on the data lines at the same time LRCLK toggles. The data is written MSB-first and is valid on the rising edge of the bit clock. The DAP masks unused trailing data bit positions.

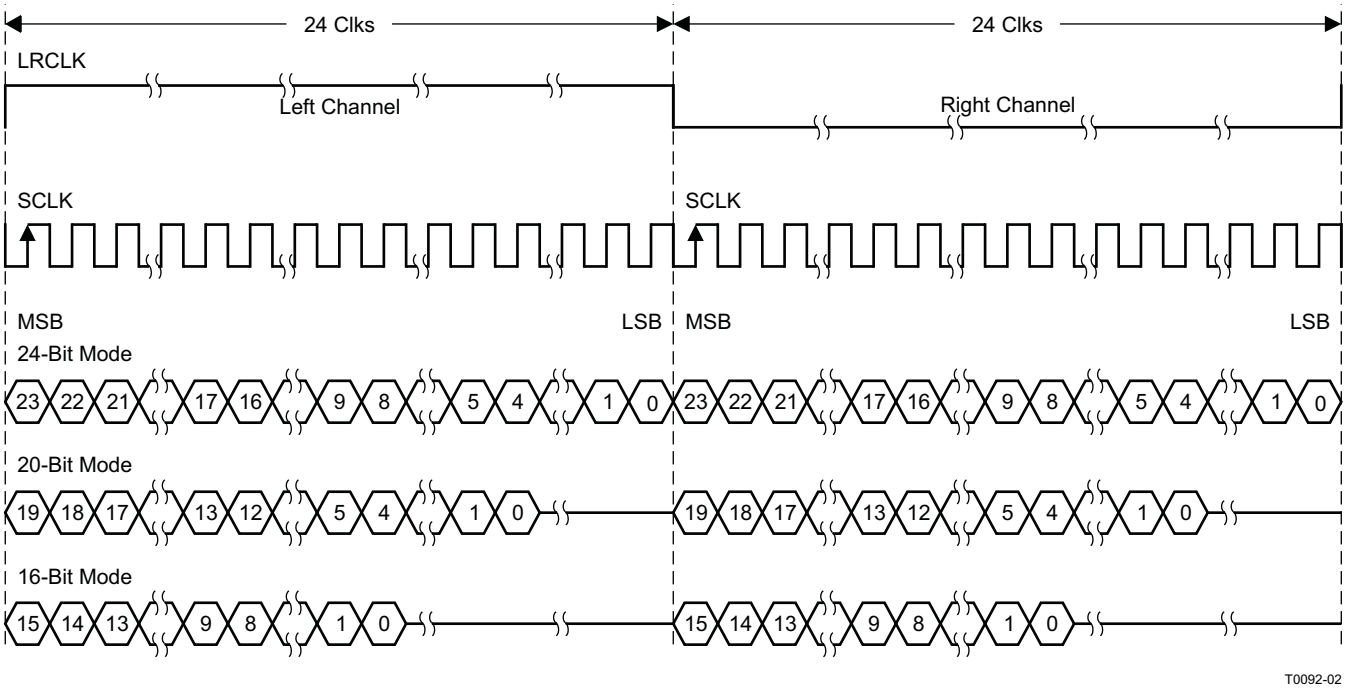



NOTE: All data presented in 2s-complement form with MSB first.

**Figure 49. Left-Justified 64-$F_S$ Format**

## Feature Description (continued)

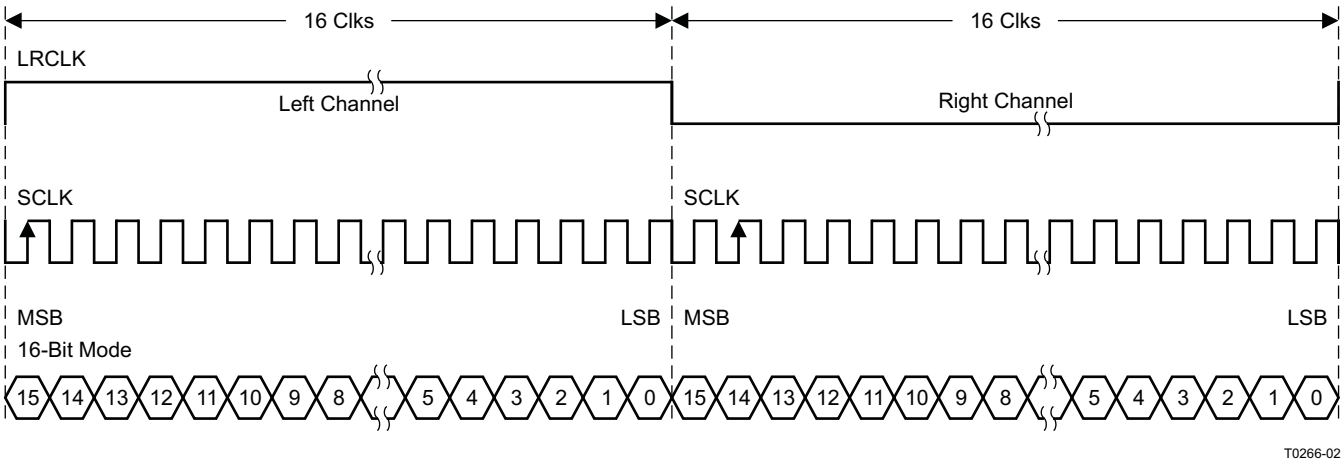
2-Channel Left-Justified Stereo Input (24-Bit Transfer Word Size)




NOTE: All data presented in 2s-complement form with MSB first.

**Figure 50. Left-Justified 48-$F_S$ Format**

2-Channel Left-Justified Stereo Input




NOTE: All data presented in 2s-complement form with MSB first.

**Figure 51. Left-Justified 32-$F_S$ Format**

## Feature Description (continued)

### 9.3.10.3 Right-Justified

Right-justified (RJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at 32, 48, or 64 × $f_S$ is used to clock in the data. The first bit of data appears on the data 8 bit-clock periods (for 24-bit data) after LRCLK toggles. In RJ mode, the LSB of data is always clocked by the last bit clock before LRCLK transitions. The data is written MSB-first and is valid on the rising edge of bit clock. The DAP masks unused leading data bit positions.

2-Channel Right-Justified (Sony Format) Stereo Input

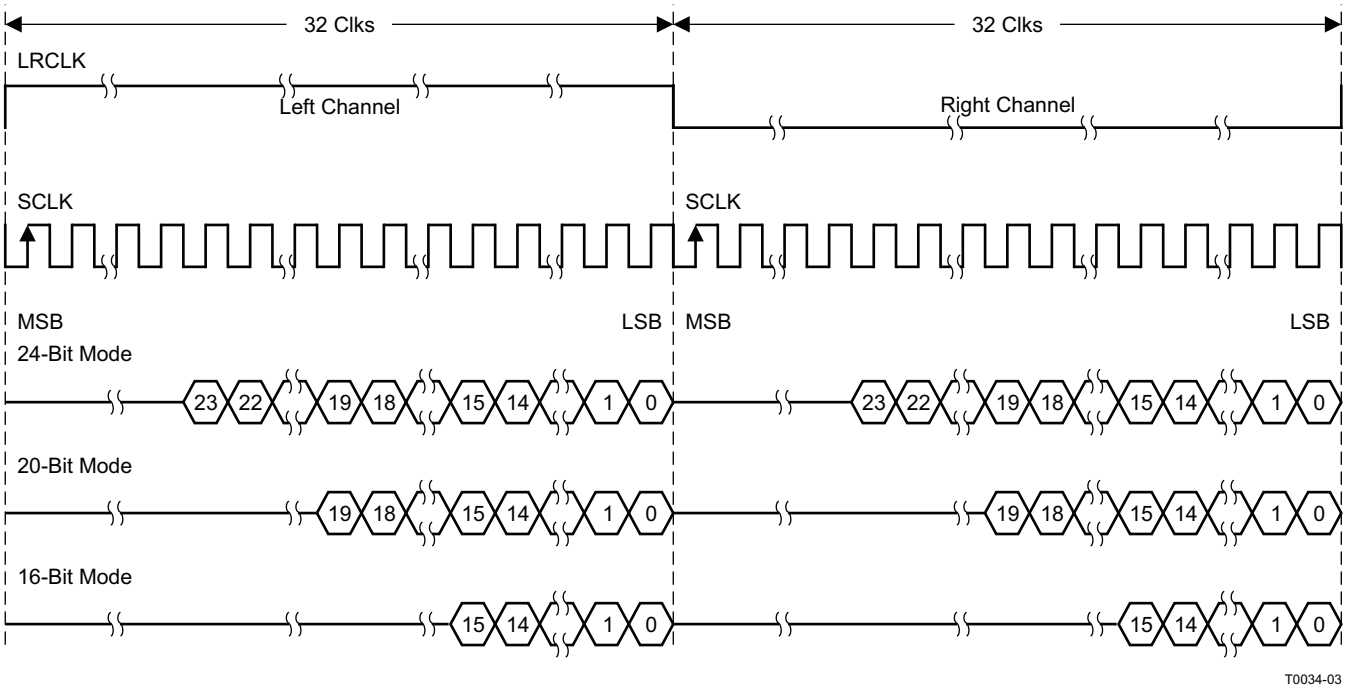



**Figure 52. Right-Justified 64-$F_S$ Format**

## Feature Description (continued)

2-Channel Right-Justified Stereo Input (24-Bit Transfer Word Size)

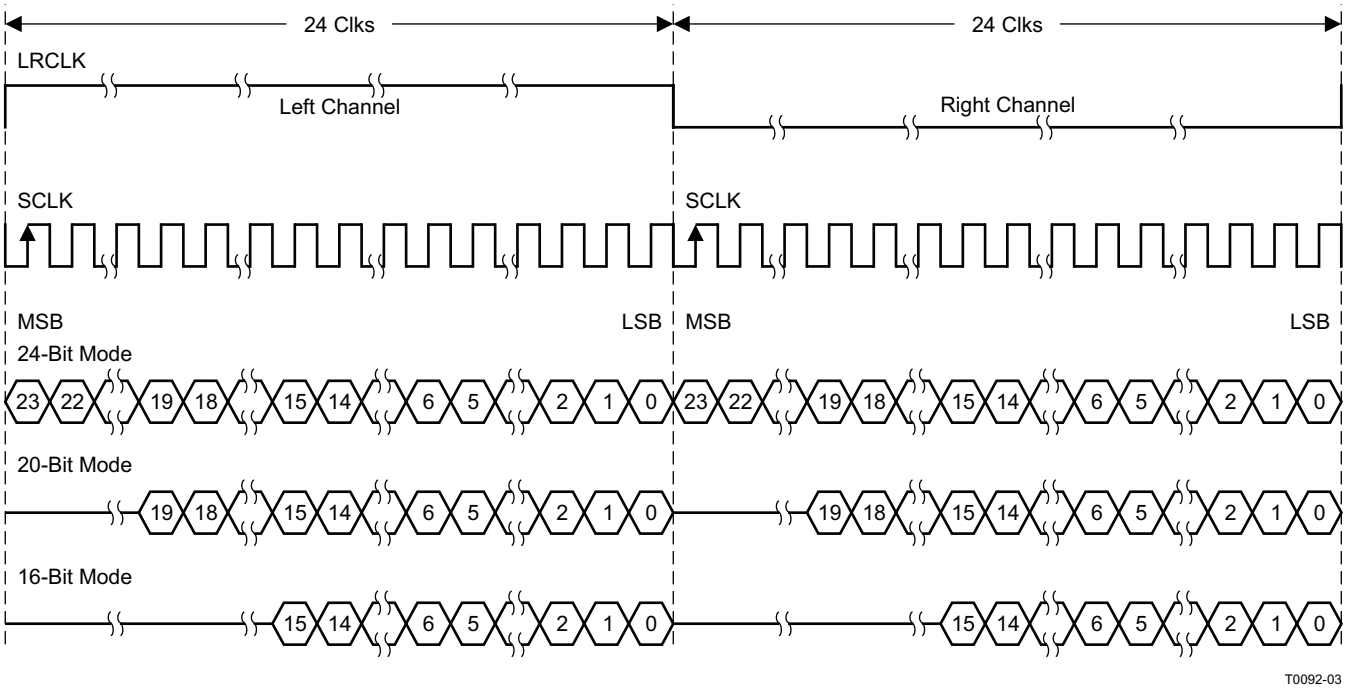



**Figure 53. Right-Justified 48-$F_S$ Format**

2-Channel Right-Justified (Sony Format) Stereo Input

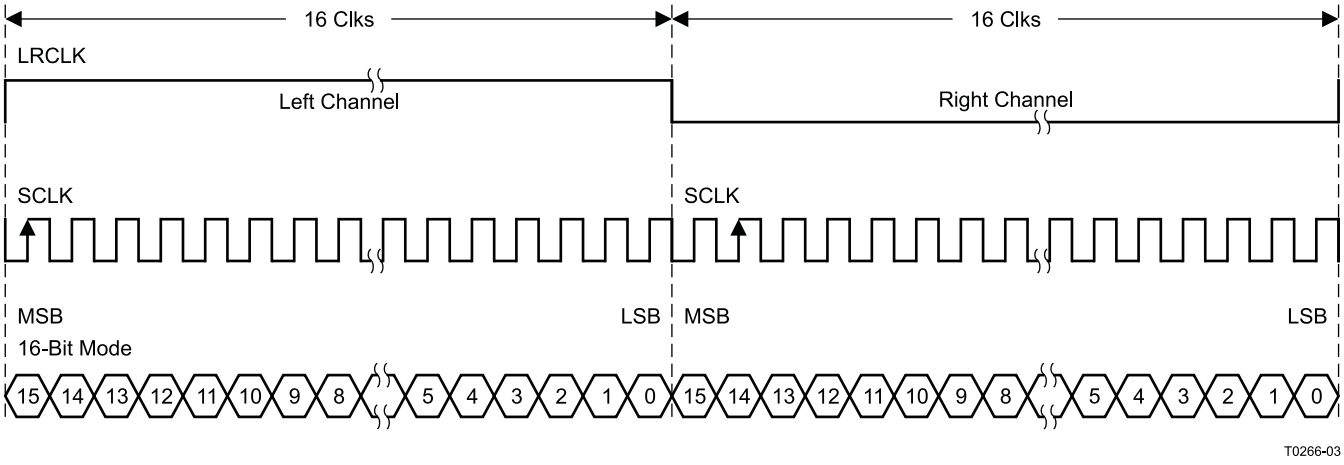


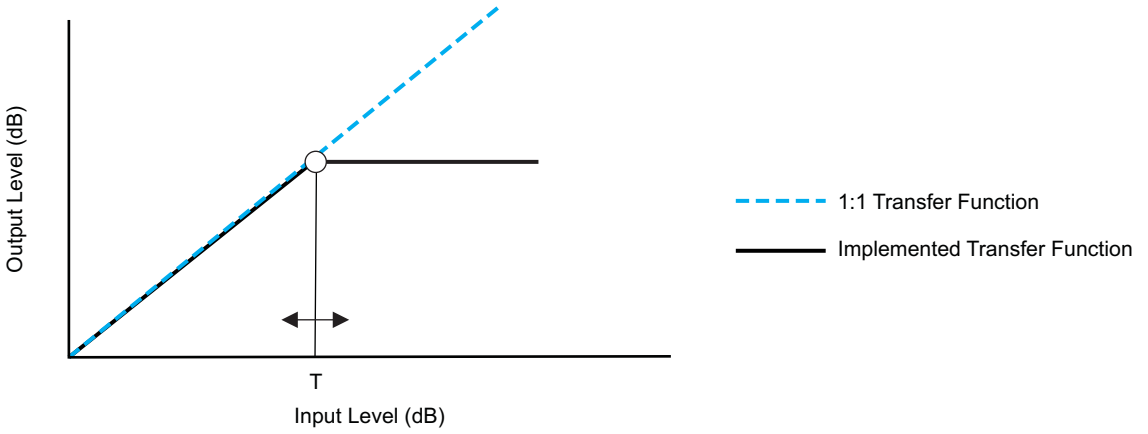

**Figure 54. Right-Justified 32-$F_S$ Format**

## Feature Description (continued)

### 9.3.11 Dynamic Range Control (DRC)

The DRC scheme has two DRC blocks. There is one ganged DRC for the high-band left/right channels and one DRC for the low-band left/right channels.

The DRC input/output diagram is shown in Figure 55.

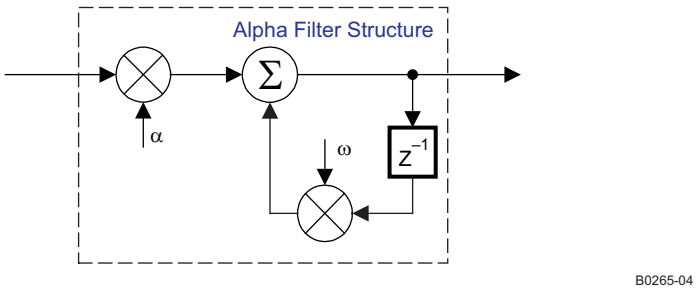



Professional-quality dynamic range compression automatically adjusts volume to flatten volume level.

- Each DRC has adjustable threshold levels.
- Programmable attack and decay time constants
- *Transparent compression*: compressors can attack fast enough to avoid apparent clipping before engaging, and decay times can be set slow enough to avoid pumping.

**Figure 55. Dynamic Range Control**

| | $\alpha$, $\omega$ | T | $\alpha_a$, $\omega_a$ / $\alpha_d$, $\omega_d$ |
|---|---|---|---|
| DRC1 | 0x3C | 0x3B | 0x40 |
| DRC2 | 0x3F | 0x3E | 0x43 |




T = 9.23 format, all other DRC coefficients are 3.23 format

**Figure 56. DRC Structure**

## 9.4 Device Functional Modes

### 9.4.1 Stereo BTL Mode

The classic stereo mode of operation uses the TAS5755M device to amplify two independent signals, which represent the left and right portions of a stereo signal. These amplified left and right audio signals are presented on differential output pairs shown as OUT_A and OUT_B for a channel and OUT_C and OUT_D for the other one. The routing of the audio data which is presented on the OUT_x outputs can be changed according to the PWM Output Mux Register (0x25). By default, the TAS5755M device is configured to output channel 1 to the OUT_A and OUT_B outputs, and channel 2 to the OUT_C and OUT_D outputs. Stereo Mode operation outputs are shown in Figure 57.

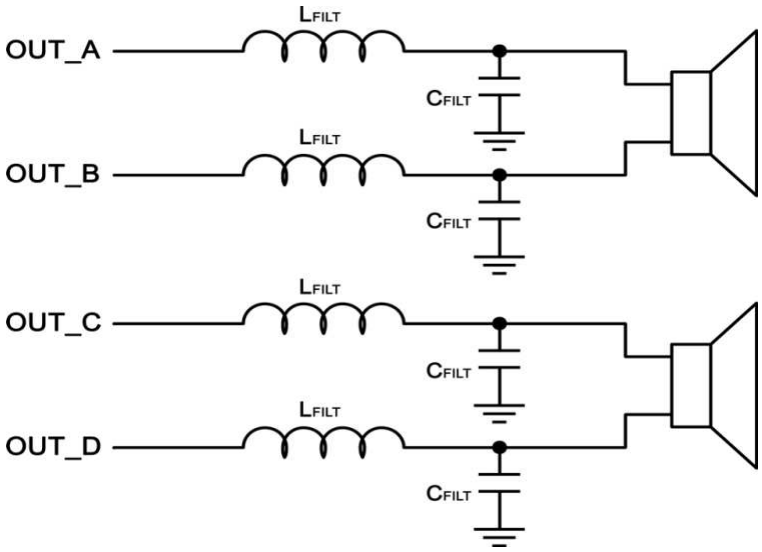



**Figure 57. Stereo BTL Mode**

### 9.4.2 Mono PBTL Mode

When this mode of operation is used, the two stereo outputs of the device are placed in parallel one with another to increase the power sourcing capabilities of the device. The TAS5755M supports parallel BTL (PBTL) mode with OUT_A/OUT_B (and OUT_C/OUT_D) connected before the LC filter.

The merging of the two output channels in this device can be done before the inductor portion of the output filter. This is called Single-Filter PBTL, and this mono operation is shown in Figure 58. More information about this can be found in *Single-Filter PBTL Mode* section.

## Device Functional Modes (continued)

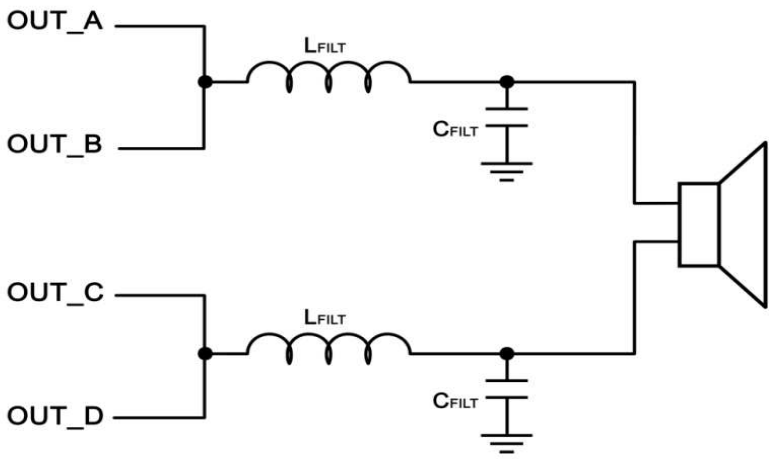



**Figure 58. Pre-Filter PBTL**

On the input side of the TAS5755M device, the input signal to the mono amplifier can be selected from a mix, left or right frame from an $I^2S$, LJ, or RJ signal. The routing of the audio data which is presented on the SPK_OUTx outputs must be configured with the PWM Output Mux Register (0x25) and PWM Shutdown Group Register (0x19).

Refer to the *Mono Parallel Bridge Tied Load Application* section for more details of the correct PBTL output connection of the TAS5755M.

### 9.4.3 2.1 Mode

2.1 Mode is defined as the application of two Single ended channels and one BTL channel used in systems where a third sub channel is required. Generally, both single-ended inputs drive the Left and Right channels, while the BTL channel drives a low-frequency content channel called often Subwoofer. More information about this can be found in the *2.1-Mode Support* section.

## Device Functional Modes (continued)

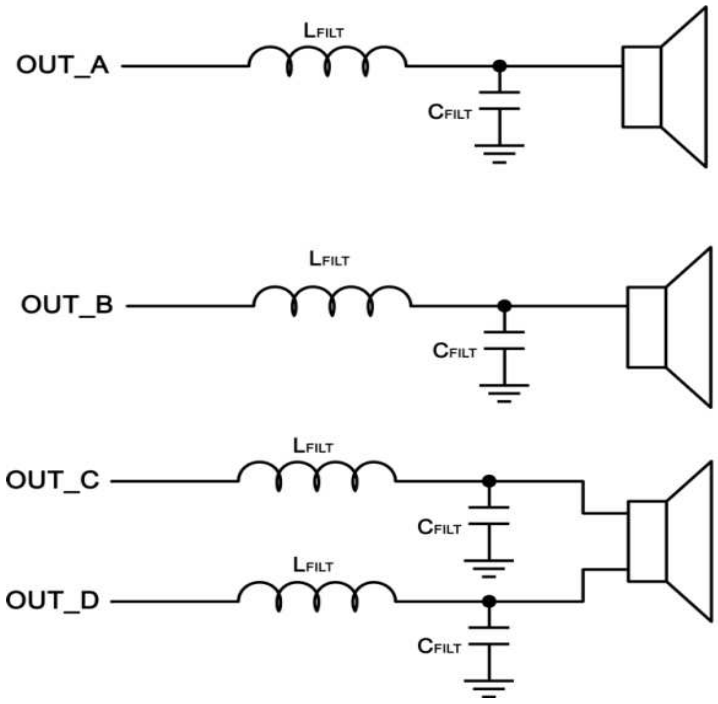



**Figure 59. 2.1 Mode**

Refer to *2.1 Application* section for more details of the correct 2.1 output connection of the TAS5755M.

## 9.5 Programming

### 9.5.1 $I^2C$ Serial Control Interface

The TAS5755M DAP has a bidirectional $I^2C$ interface that is compatible with the Inter IC ($I^2C$) bus protocol and supports both 100-kHz and 400-kHz data transfer rates for single- and multiple-byte write and read operations. This is a slave-only device that does not support a multimaster bus environment or wait-state insertion. The control interface is used to program the registers of the device and to read device status.

The DAP supports the standard-mode $I^2C$ bus operation (100 kHz maximum) and the fast $I^2C$ bus operation (400 kHz maximum). The DAP performs all $I^2C$ operations without $I^2C$ wait cycles.

#### *9.5.1.1 General $I^2C$ Operation*

The $I^2C$ bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially, one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most-significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 60. The master generates the 7-bit slave address and the read/write (R/$\overline{W}$) bit to open communication with another device and then waits for an acknowledge condition. The TAS5755M holds SDA low during the acknowledge clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/$\overline{W}$ bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pullup resistor must be used for the SDA and SCL signals to set the high level for the bus.

## Programming (continued)

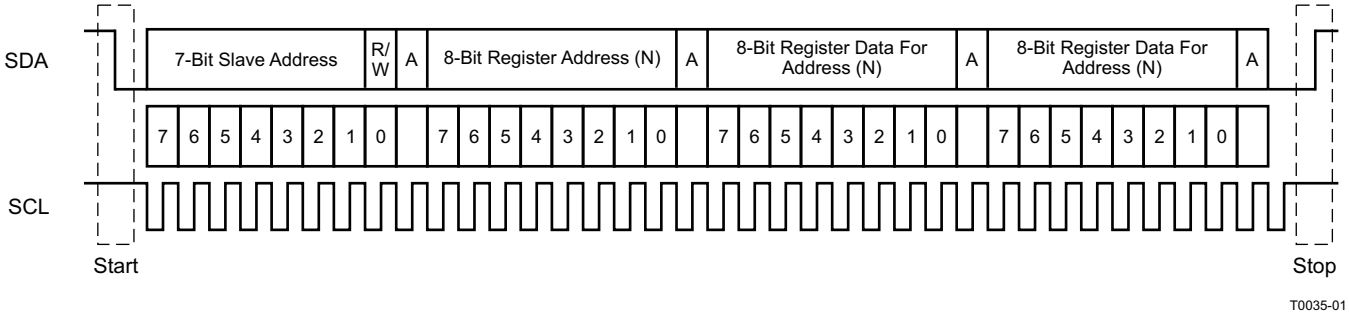



**Figure 60. Typical I²C Sequence**

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 60.

The 7-bit address for TAS5755M is 0011 011 (0x36).

### *9.5.1.2 Single- and Multiple-Byte Transfers*

The serial control interface supports both single-byte and multiple-byte read/write operations for subaddresses 0x00 to 0x1F. However, for the subaddresses 0x20 to 0xFF, the serial control interface supports only multiple-byte read/write operations (in multiples of 4 bytes).

During multiple-byte read operations, the DAP responds with data, a byte at a time, starting at the subaddress assigned, as long as the master device continues to respond with acknowledges. If a particular subaddress does not contain 32 bits, the unused bits are read as logic 0.

During multiple-byte write operations, the DAP compares the number of bytes transmitted to the number of bytes that are required for each specific subaddress. For example, if a write command is received for a biquad subaddress, the DAP must receive five 32-bit words. If fewer than five 32-bit data words have been received when a stop command (or another start command) is received, the received data is discarded.

Supplying a subaddress for each subaddress transaction is referred to as random I²C addressing. The TAS5755M also supports sequential I²C addressing. For write transactions, if a subaddress is issued followed by data for that subaddress and the 15 subaddresses that follow, a sequential I²C write transaction has taken place, and the data for all 16 subaddresses is successfully received by the TAS5755M. For I²C sequential-write transactions, the subaddress then serves as the start address, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many subaddresses are written. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last subaddress, the data for the last subaddress is discarded. However, all other data written is accepted; only the incomplete data is discarded.

### *9.5.1.3 Single-Byte Write*

As shown in Figure 61, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a data-write transfer, the read/write bit is a 0. After receiving the correct I²C device address and the read/write bit, the DAP responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the TAS5755M internal memory address being accessed. After receiving the address byte, the TAS5755M again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5755M again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

## Programming (continued)

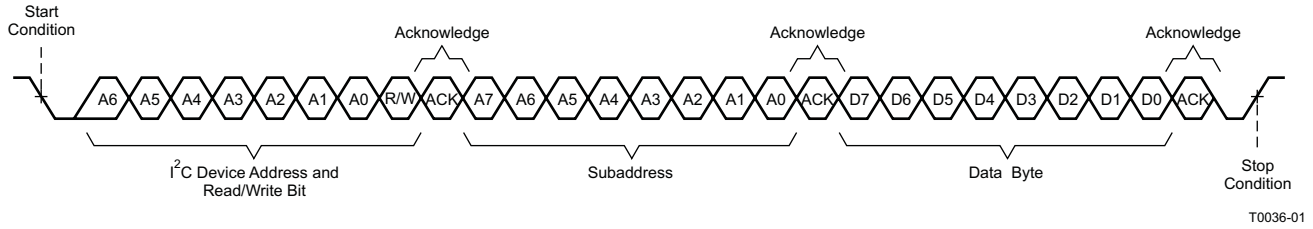



**Figure 61. Single-Byte Write Transfer**

### 9.5.1.4 Multiple-Byte Write

A multiple-byte data-write transfer is identical to a single-byte data-write transfer except that multiple data bytes are transmitted by the master device to the DAP as shown in Figure 62. After receiving each data byte, the TAS5755M responds with an acknowledge bit.

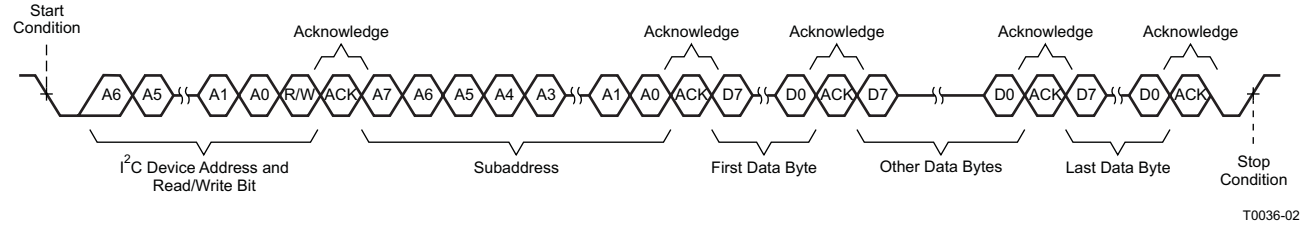



**Figure 62. Multiple-Byte Write Transfer**

### 9.5.1.5 Single-Byte Read

As shown in Figure 63, a single-byte data-read transfer begins with the master device transmitting a start condition, followed by the $I^2C$ device address and the read/write bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the read/write bit becomes a 0. After receiving the TAS5755M address and the read/write bit, TAS5755M responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the TAS5755M address and the read/write bit again. This time, the read/write bit becomes a 1, indicating a read transfer. After receiving the address and the read/write bit, the TAS5755M again responds with an acknowledge bit. Next, the TAS5755M transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

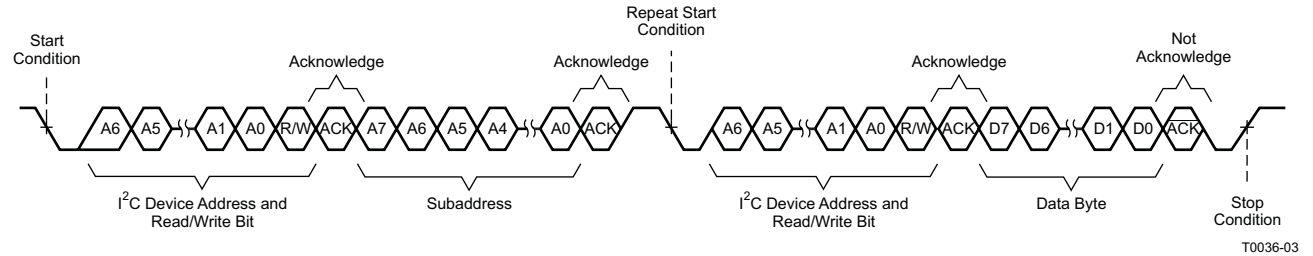



**Figure 63. Single-Byte Read Transfer**

### 9.5.1.6 Multiple-Byte Read

A multiple-byte data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the TAS5755M to the master device as shown in Figure 64. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

## Programming (continued)

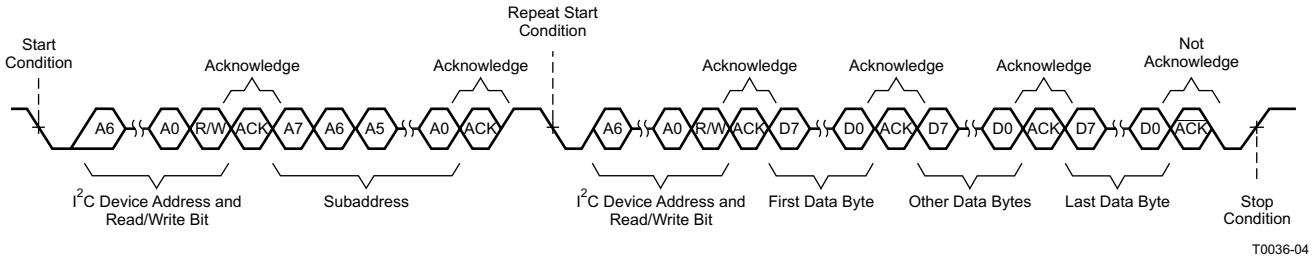



**Figure 64. Multiple-Byte Read Transfer**

### 9.5.2 26-Bit 3.23 Number Format

All mixer gain coefficients are 26-bit coefficients using a 3.23 number format. Numbers formatted as 3.23 numbers means that there are 3 bits to the left of the binary point and 23 bits to the right of the binary point. This is shown in Figure 65.

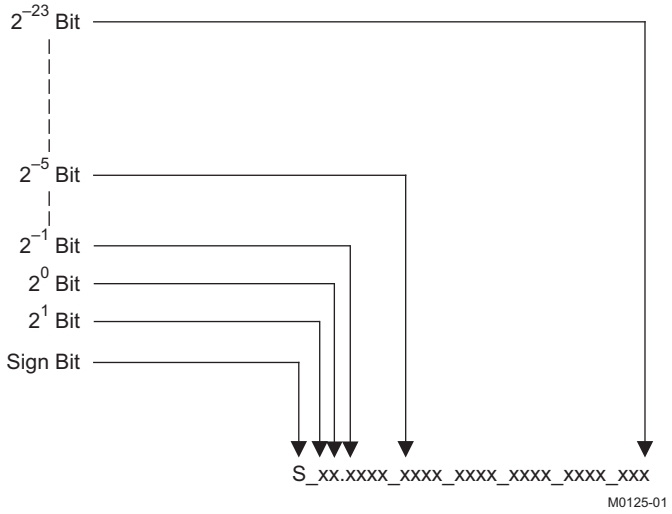



**Figure 65. 3.23 Format**

The decimal value of a 3.23 format number can be found by following the weighting shown in Figure 65. If the most significant bit is logic 0, the number is a positive number, and the weighting shown yields the correct number. If the most significant bit is a logic 1, then the number is a negative number. In this case every bit must be inverted, a 1 added to the result, and then the weighting shown in Figure 66 applied to obtain the magnitude of the negative number.

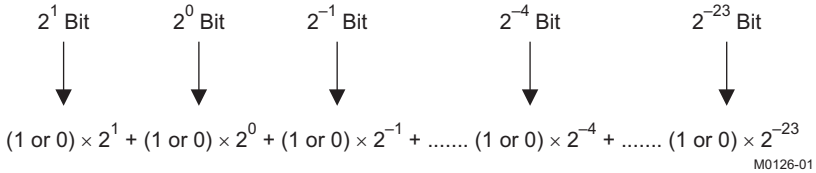
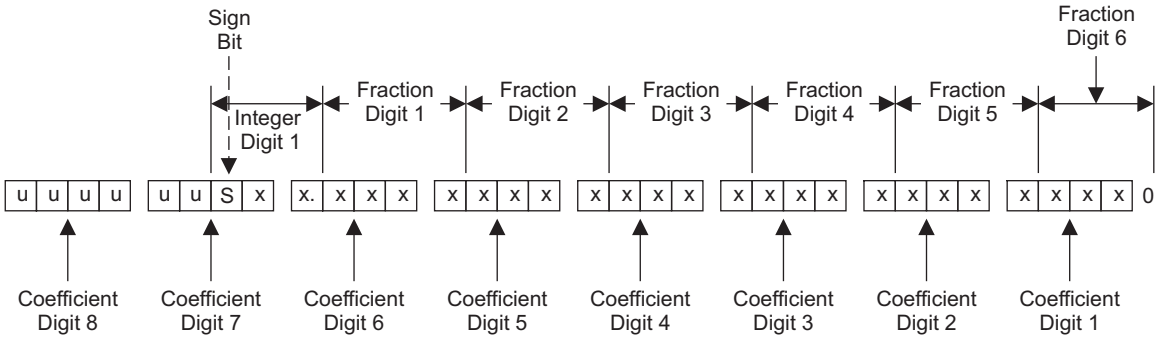



**Figure 66. Conversion Weighting Factors — 3.23 Format To Floating Point**

Gain coefficients, entered via the I²C bus, must be entered as 32-bit binary numbers. The format of the 32-bit number (4-byte or 8-digit hexadecimal number) is shown in Figure 67.

## Programming (continued)




u = unused or don't care bits
Digit = hexadecimal digit

M0127-01

**Figure 67. Alignment of 3.23 Coefficient in 32-Bit I²C Word**

**Table 1. Sample Calculation for 3.23 Format**

| db | LINEAR | DECIMAL | HEX (3.23 Format) |
|---|---|---|---|
| 0 | 1 | 8,388,608 | 80 0000 |
| 5 | 1.77 | 14,917,288 | 00E3 9EA8 |
| –5 | 0.56 | 4,717,260 | 0047 FACC |
| X | $L = 10^{(X/20)}$ | D = 8,388,608 × L | H = dec2hex (D, 8) |

**Table 2. Sample Calculation for 9.17 Format**

| db | LINEAR | DECIMAL | HEX (9.17 Format) |
|---|---|---|---|
| 0 | 1 | 131,072 | 2 0000 |
| 5 | 1.77 | 231,997 | 3 8A3D |
| –5 | 0.56 | 73,400 | 1 1EB8 |
| X | $L = 10^{(X/20)}$ | D = 131,072 × L | H = dec2hex (D, 8) |

## 9.6 Register Maps

### 9.6.1 Register Map Summary

**Table 3. Serial Control Interface Register Summary**

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS(1) | INITIALIZATION VALUE |
|---|---|---|---|---|
| 0x00 | Clock control register | 1 | Description shown in subsequent section | 0x6C |
| 0x01 | Device ID register | 1 | Description shown in subsequent section | 0x00 |
| 0x02 | Error status register | 1 | Description shown in subsequent section | 0x00 |
| 0x03 | System control register 1 | 1 | Description shown in subsequent section | 0xA0 |
| 0x04 | Serial data interface register | 1 | Description shown in subsequent section | 0x05 |
| 0x05 | System control register 2 | 1 | Description shown in subsequent section | 0x40 |
| 0x06 | Soft mute register | 1 | Description shown in subsequent section | 0x00 |
| 0x07 | Master volume | 1 | Description shown in subsequent section | 0xFF (mute) |
| 0x08 | Channel 1 vol | 1 | Description shown in subsequent section | 0x30 (0 dB) |
| 0x09 | Channel 2 vol | 1 | Description shown in subsequent section | 0x30 (0 dB) |
| 0x0A | Channel 3 vol | 1 | Description shown in subsequent section | 0x30 (0 dB) |
| 0x0B–0x0D | | 1 | Reserved(2) | |
| 0x0E | Volume configuration register | 1 | Description shown in subsequent section | 0x91 |
| 0x0F | | 1 | Reserved(2) | |
| 0x10 | Modulation limit register | 1 | Description shown in subsequent section | 0x02 |
| 0x11 | IC delay channel 1 | 1 | Description shown in subsequent section | 0xAC |
| 0x12 | IC delay channel 2 | 1 | Description shown in subsequent section | 0x54 |
| 0x13 | IC delay channel 3 | 1 | Description shown in subsequent section | 0xAC |
| 0x14 | IC delay channel 4 | 1 | Description shown in subsequent section | 0x54 |
| 0x15-0x18 | | 1 | Reserved(2) | |
| 0x19 | PWM channel shutdown group register | 1 | Description shown in subsequent section | 0x30 |
| 0x1A | Start/stop period register | 1 | | 0x0F |
| 0x1B | Oscillator trim register | 1 | | 0x82 |
| 0x1C | BKND_ERR register | 1 | | 0x02 |
| 0x1D–0x1F | | 1 | Reserved(2) | |
| 0x20 | Input MUX register | 4 | Description shown in subsequent section | 0x0001 7772 |
| 0x21 | Ch 4 source select register | 4 | Description shown in subsequent section | 0x0000 4303 |
| 0x22 -0x24 | | 4 | Reserved(2) | |
| 0x25 | PWM MUX register | 4 | Description shown in subsequent section | 0x0102 1345 |
| 0x26-0x28 | | 4 | Reserved(2) | |
| 0x29 | ch1_bq[0] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x2A | ch1_bq[1] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |

(1) A u indicates unused bits.
(2) Reserved registers must not be accessed.

## Register Maps (continued)

**Table 3. Serial Control Interface Register Summary (continued)**

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS(1) | INITIALIZATION VALUE |
|---|---|---|---|---|
| 0x2B | ch1_bq[2] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x2C | ch1_bq[3] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x2D | ch1_bq[4] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x2E | ch1_bq[5] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x2F | ch1_bq[6] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x30 | ch2_bq[0] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x31 | ch2_bq[1] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x32 | ch2_bq[2] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x33 | ch2_bq[3] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |

## Register Maps (continued)

**Table 3. Serial Control Interface Register Summary (continued)**

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS(1) | INITIALIZATION VALUE |
|---|---|---|---|---|
| 0x34 | ch2_bq[4] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x35 | ch2_bq[5] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x36 | ch2_bq[6] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x37 - 0x39 | | 4 | Reserved(2) | |
| 0x3A | DRC1 ae(3) | 8 | u[31:26], ae[25:0] | 0x0080 0000 |
| | DRC1 (1 – ae) | | u[31:26], (1 – ae)[25:0] | 0x0000 0000 |
| 0x3B | DRC1 aa | 8 | u[31:26], aa[25:0] | 0x0080 0000 |
| | DRC1 (1 – aa) | | u[31:26], (1 – aa)[25:0] | 0x0000 0000 |
| 0x3C | DRC1 ad | 8 | u[31:26], ad[25:0] | 0x0080 0000 |
| | DRC1 (1 – ad) | | u[31:26], (1 – ad)[25:0] | 0x0000 0000 |
| 0x3D | DRC2 ae | 8 | u[31:26], ae[25:0] | 0x0080 0000 |
| | DRC 2 (1 – ae) | | u[31:26], (1 – ae)[25:0] | 0x0000 0000 |
| 0x3E | DRC2 aa | 8 | u[31:26], aa[25:0] | 0x0080 0000 |
| | DRC2 (1 – aa) | | u[31:26], (1 – aa)[25:0] | 0x0000 0000 |
| 0x3F | DRC2 ad | 8 | u[31:26], ad[25:0] | 0x0080 0000 |
| | DRC2 (1 – ad) | | u[31:26], (1 – ad)[25:0] | 0x0000 0000 |
| 0x40 | DRC1-T | 4 | T1[31:0] (9.23 format) | 0xFDA2 1490 |
| 0x41 | DRC1-K | 4 | u[31:26], K1[25:0] | 0x0384 2109 |
| 0x42 | DRC1-O | 4 | u[31:26], O1[25:0] | 0x0008 4210 |
| 0x43 | DRC2-T | 4 | T2[31:0] (9.23 format) | 0xFDA2 1490 |
| 0x44 | DRC2-K | 4 | u[31:26], K2[25:0] | 0x0384 2109 |
| 0x45 | DRC2-O | 4 | u[31:26], O2[25:0] | 0x0008 4210 |
| 0x46 | DRC control | 4 | Description shown in subsequent section | 0x0000 0000 |
| 0x47–0x4F | | 4 | Reserved(2) | |
| 0x50 | Bank switch control | 4 | Description shown in subsequent section | 0x0F70 8000 |
| 0x51 | Ch 1 output mixer | 12 | Ch 1 output mix1[2] | 0x0080 0000 |
| | | | Ch 1 output mix1[1] | 0x0000 0000 |
| | | | Ch 1 output mix1[0] | 0x0000 0000 |
| 0x52 | Ch 2 output mixer | 12 | Ch 2 output mix2[2] | 0x0080 0000 |
| | | | Ch 2 output mix2[1] | 0x0000 0000 |
| | | | Ch 2 output mix2[0] | 0x0000 0000 |

(3) "ae" stands for $\propto$ of energy filter, "aa" stands for $\propto$ of attack filter and "ad" stands for $\propto$ of decay filter and 1- $\propto$ = $\omega$.

## Register Maps (continued)

**Table 3. Serial Control Interface Register Summary (continued)**

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS(1) | INITIALIZATION VALUE |
|---|---|---|---|---|
| 0x53 | Ch 1 input mixer | 16 | Ch 1 input mixer[3] | 0x0080 0000 |
| | | | Ch 1 input mixer[2] | 0x0000 0000 |
| | | | Ch 1 input mixer[1] | 0x0000 0000 |
| | | | Ch 1 input mixer[0] | 0x0080 0000 |
| 0x54 | Ch 2 input mixer | 16 | Ch 2 input mixer[3] | 0x0080 0000 |
| | | | Ch 2 input mixer[2] | 0x0000 0000 |
| | | | Ch 2 input mixer[1] | 0x0000 0000 |
| | | | Ch 2 input mixer[0] | 0x0080 0000 |
| 0x55 | Channel 3 input mixer | 12 | Channel 3 input mixer [2] | 0x0080 0000 |
| | | | Channel 3 input mixer [1] | 0x0000 0000 |
| | | | Channel 3 input mixer [0] | 0x0000 0000 |
| 0x56 | Output post-scale | 4 | u[31:26], post[25:0] | 0x0080 0000 |
| 0x57 | Output pre-scale | 4 | u[31:26], pre[25:0] (9.17 format) | 0x0002 0000 |
| 0x58 | ch1 BQ[7] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x59 | ch1 BQ[8] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x5A | Subchannel BQ[0] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x5B | Subchannel BQ[1] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x5C | ch2 BQ[7] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x5D | ch2 BQ[8] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |

## Register Maps (continued)

**Table 3. Serial Control Interface Register Summary (continued)**

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS(1) | INITIALIZATION VALUE |
|---|---|---|---|---|
| 0x5E | pseudo_ch2 BQ[0] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x5F | | 4 | Reserved(2) | |
| 0x60 | Channel 4 (subchannel) output mixer | 8 | Ch 4 output mixer[1] | 0x0000 0000 |
| | | | Ch 4 output mixer[0] | 0x0080 0000 |
| 0x61 | Channel 4 (subchannel) input mixer | 8 | Ch 4 input mixer[1] | 0x0040 0000 |
| | | | Ch 4 input mixer[0] | 0x0040 0000 |
| 0x62 | IDF post scale | 4 | Post-IDF attenuation register | 0x0000 0080 |
| 0x63–0xF7 | | | Reserved(2) | 0x0000 0000 |
| 0xF8 | Device address enable register | 4 | Write F9 A5 A5 A5 in this register to enable write to device address update (0xF9) | 0x0000 0000 |
| 0xF9 | Device address Update Register | 4 | u[31:8], New Dev Id[7:1] , ZERO[0] (New Dev Id (7:1) defines the new device address | 0X0000 0036 |
| 0xFA–0xFF | | 4 | Reserved(2) | 0x0000 0000 |

All DAP coefficients are 3.23 format unless specified otherwise.

### 9.6.2 Register Maps

#### *9.6.2.1 Clock Control Register (0x00)*

The clocks and data rates are automatically determined by the TAS5755M. The clock control register contains the auto-detected clock status. Bits D7–D5 reflect the sample rate. Bits D4–D2 reflect the MCLK frequency. The device accepts a 64 $f_S$ or 32 $f_S$ SCLK rate for all MCLK ratios, but accepts a 48 $f_S$ SCLK rate for MCLK ratios of 192 $f_S$ and 384 $f_S$ only.

**Table 4. Clock Control Register (0x00)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | – | – | – | – | – | $f_S$ = 32-kHz sample rate |
| 0 | 0 | 1 | – | – | – | – | – | Reserved(1) |
| 0 | 1 | 0 | – | – | – | – | – | Reserved(1) |
| **0** | **1** | **1** | **–** | **–** | **–** | – | **–** | **$f_S$ = 44.1/48-kHz sample rate(2)** |
| 1 | 0 | 0 | – | – | – | – | – | $f_S$ = 16-kHz sample rate |
| 1 | 0 | 1 | – | – | – | – | – | $f_S$ = 22.05/24-kHz sample rate |
| 1 | 1 | 0 | – | – | – | – | – | $f_S$ = 8-kHz sample rate |
| 1 | 1 | 1 | – | – | – | – | – | $f_S$ = 11.025/12-kHz sample rate |
| – | – | – | 0 | 0 | 0 | – | – | MCLK frequency = 64 × $f_S$(3) |
| – | – | – | 0 | 0 | 1 | – | – | MCLK frequency = 128 × $f_S$(3) |
| – | – | – | 0 | 1 | 0 | – | – | MCLK frequency = 192 × $f_S$(4) |
| **–** | **–** | **–** | **0** | **1** | **1** | **–** | **–** | **MCLK frequency = 256 × $f_S$** (2)(5) |
| – | – | – | 1 | 0 | 0 | – | – | MCLK frequency = 384 × $f_S$ |
| – | – | – | 1 | 0 | 1 | – | – | MCLK frequency = 512 × $f_S$ |
| – | – | – | 1 | 1 | 0 | – | – | Reserved(1) |
| – | – | – | 1 | 1 | 1 | – | – | Reserved(1) |
| – | – | – | – | – | – | **0** | – | **Reserved(1)** (2) |
| **–** | **–** | **–** | – | **–** | **–** | **–** | **0** | **Reserved**(1) (2) |

(1) Reserved registers must not be accessed.
(2) Default values are in **bold**.
(3) Only available for 44.1-kHz and 48-kHz rates
(4) Rate only available for 32/44.1/48-kHz sample rates
(5) Not available at 8 kHz

#### *9.6.2.2 Device ID Register (0x01)*

The device ID register contains the ID code for the firmware revision.

**Table 5. General Status Register (0x01)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Identification code** |

#### 9.6.2.3 Error Status Register (0x02)

The error bits are sticky and are not cleared by the hardware. This means that the software must clear the register (write zeroes) and then read them to determine if they are persistent errors.

Error Definitions:

- MCLK Error : MCLK frequency is changing. The number of MCLKs per LRCLK is changing.
- SCLK Error: The number of SCLKs per LRCLK is changing.
- LRCLK Error: LRCLK frequency is changing.
- Frame Slip: LRCLK phase is drifting with respect to internal Frame Sync.

**Table 6. Error Status Register (0x02)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 1 | - | – | – | – | – | – | – | MCLK error |
| – | 1 | – | – | – | – | – | – | PLL autolock error |
| – | – | 1 | – | – | – | – | – | SCLK error |
| – | – | – | 1 | – | – | – | – | LRCLK error |
| – | – | – | – | 1 | – | – | – | Frame slip |
| – | – | – | – | – | 1 | – | – | Clip indicator |
| – | – | – | – | – | – | 1 | – | Overcurrent, overtemperature, or undervoltage errors |
| – | – | – | – | – | – | – | **0** | **Reserved** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | – | **No errors**(1) |

(1) Default values are in **bold**.

#### 9.6.2.4 System Control Register 1 (0x03)

The system control register 1 has several functions:

Bit D7: If 0, the dc-blocking filter for each channel is disabled.
If 1, the dc-blocking filter (–3 dB cutoff <1 Hz) for each channel is enabled (default).

Bit D5: If 0, use soft unmute on recovery from clock error. This is a slow recovery. Unmute takes the same time as the volume ramp defined in register 0x0E.
If 1, use hard unmute on recovery from clock error (default). This is a fast recovery, a single step volume ramp

Bits D1–D0: Select de-emphasis

**Table 7. System Control Register 1 (0x03)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 0 | – | – | – | – | – | – | – | PWM high-pass (dc blocking) disabled |
| **1** | – | – | – | – | – | – | – | **PWM high-pass (dc blocking) enabled**(1) |
| – | **0** | – | – | – | – | – | – | **Reserved**(1) |
| – | – | 0 | – | – | – | – | – | Soft unmute on recovery from clock error |
| – | – | **1** | – | – | – | – | – | **Hard unmute on recovery from clock error**(1) |
| – | – | – | **0** | – | – | – | – | **Reserved**(1) |
| – | – | – | – | **0** | – | – | – | **Reserved**(1) |
| – | – | – | – | – | **0** | – | – | **Reserved**(1) |
| – | – | – | – | – | – | **0** | **0** | **No de-emphasis**(1) |
| – | – | – | – | – | – | 0 | 1 | De-emphasis for $f_S$ = 32 kHz |
| – | – | – | – | – | – | 1 | 0 | De-emphasis for $f_S$ = 44.1 kHz |
| – | – | – | – | – | – | 1 | 1 | De-emphasis for $f_S$ = 48 kHz |

(1) Default values are in **bold**.

#### 9.6.2.5 Serial Data Interface Register (0x04)

As shown in Table 8, the TAS5755M supports 9 serial data modes. The default is 24-bit, $I^2S$ mode,

**Table 8. Serial Data Interface Control Register (0x04)**

| RECEIVE SERIAL DATA INTERFACE FORMAT | WORD LENGTH | D7–D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|
| Right-justified | 16 | 0000 | 0 | 0 | 0 | 0 |
| Right-justified | 20 | 0000 | 0 | 0 | 0 | 1 |
| Right-justified | 24 | 0000 | 0 | 0 | 1 | 0 |
| $I^2S$ | 16 | 000 | 0 | 0 | 1 | 1 |
| $I^2S$ | 20 | 0000 | 0 | 1 | 0 | 0 |
| **$I^2S$** (1) | **24** | **0000** | **0** | **1** | **0** | **1** |
| Left-justified | 16 | 0000 | 0 | 1 | 1 | 0 |
| Left-justified | 20 | 0000 | 0 | 1 | 1 | 1 |
| Left-justified | 24 | 0000 | 1 | 0 | 0 | 0 |
| Reserved | | 0000 | 1 | 0 | 0 | 1 |
| Reserved | | 0000 | 1 | 0 | 1 | 0 |
| Reserved | | 0000 | 1 | 0 | 1 | 1 |
| Reserved | | 0000 | 1 | 1 | 0 | 0 |
| Reserved | | 0000 | 1 | 1 | 0 | 1 |
| Reserved | | 0000 | 1 | 1 | 1 | 0 |
| Reserved | | 0000 | 1 | 1 | 1 | 1 |

(1) Default values are in **bold**.

#### 9.6.2.6 System Control Register 2 (0x05)

When bit D6 is set low, the system exits all channel shutdown and starts playing audio; otherwise, the outputs are shut down (hard mute).

**Table 9. System Control Register 2 (0x05)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | – | – | – | – | – | – | – | **Mid-Z ramp disabled**(1) |
| 1 | – | – | – | – | – | – | – | Mid-Z ramp enabled |
| – | 0 | – | – | – | – | – | – | Exit all-channel shutdown (normal operation) |
| – | **1** | – | – | – | – | – | – | **Enter all-channel shutdown (hard mute)**(1) |
| | | | | **0** | | | | **Sub-channel in AD Mode** |
| | | | | 1 | | | | Sub-channel in BD Mode |
| – | – | – | – | – | **0** | – | – | **2.0 mode [2.0 BTL]**(1) |
| – | – | – | – | – | 1 | – | – | 2.1 mode [2 SE + 1 BTL] |
| – | – | – | – | – | – | **0** | – | **ADR/$\overline{\text{FAULT}}$ pin is configured as to serve as an address input only**(1) |
| – | – | – | – | – | – | 1 | – | ADR/$\overline{\text{FAULT}}$ pin is configured as fault output |
| – | – | **0** | **0** | **-** | **–** | **–** | **0** | **Reserved**(1) |

(1) Default values are in **bold**.

### 9.6.2.7 Soft Mute Register (0x06)

Writing a 1 to any of the following bits sets the output of the respective channel to 50% duty cycle (soft mute).

**Table 10. Soft Mute Register (0x06)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **0** | **0** | – | – | – | **Reserved**(1) |
| – | – | – | – | – | **0** | – | – | **Soft unmute channel 3**(1) |
| – | – | – | – | – | 1 | – | – | Soft mute channel 3 |
| – | – | – | – | – | – | **0** | – | **Soft unmute channel 2**(1) |
| – | – | – | – | – | – | 1 | – | Soft mute channel 2 |
| – | – | – | – | – | – | – | **0** | **Soft unmute channel 1**(1) |
| – | – | – | – | – | – | – | 1 | Soft mute channel 1 |

(1) Default values are in **bold**.

### 9.6.2.8 Volume Registers (0x07, 0x08, 0x09, 0x0A)

Step size is 0.5 dB.

Master volume – 0x07 (default is mute)
Channel-1 volume – 0x08 (default is 0 dB)
Channel-2 volume – 0x09 (default is 0 dB)
Channel-3 volume – 0x0A (default is 0 dB)

**Table 11. Volume Registers (0x07, 0x08, 0x09, 0x0A)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 24 dB |
| **0** | **0** | **1** | **1** | **0** | **0** | **0** | **0** | **0 dB (default for individual channel volume)**(1) |
| | | | | | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | –103 dB |
| **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **Soft mute (default for master volume)** (1) |

(1) Default values are in **bold**.

#### 9.6.2.9 Volume Configuration Register (0x0E)

Bits D2–D0: Volume slew rate (Used to control volume change and MUTE ramp rates). These bits control the number of steps in a volume ramp. Volume steps occur at a rate that depends on the sample rate of the $I^2S$ data as follows

| Sample Rate (KHz) | Approximate Ramp Rate |
|---|---|
| 8/16/32 | 125 µs/step |
| 11.025/22.05/44.1 | 90.7 µs/step |
| 12/24/48 | 83.3 µs/step |

**Table 12. Volume Control Register (0x0E)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **1** | **–** | **–** | **1** | **0** | – | – | – | **Reserved**(1) |
| – | **0** | – | – | – | – | – | – | **Subchannel (ch4) volume = ch1 volume** (2) (1) |
| – | 1 | – | – | – | – | – | – | Subchannel volume = register 0x0A(2) |
| – | – | **0** | – | – | – | – | – | **Ch3 volume = ch2 volume**(1) |
| – | – | 1 | – | – | – | – | – | Ch3 volume = register 0x0A |
| – | – | – | – | – | 0 | 0 | 0 | Volume slew 512 steps (43-ms volume ramp time at 48 kHz) |
| – | – | – | – | – | **0** | **0** | **1** | **Volume slew 1024 steps (85-ms volume ramp time at 48 kHz)**(1) |
| – | – | – | – | – | 0 | 1 | 0 | Volume slew 2048 steps (171- ms volume ramp time at 48 kHz) |
| – | – | – | – | – | 0 | 1 | 1 | Volume slew 256 steps (21-ms volume ramp time at 48 kHz) |
| – | – | – | – | – | 1 | X | X | Reserved |

(1) Default values are in **bold**.
(2) Bits 6:5 can be changed only when volume is in MUTE [master volume = MUTE (register 0x07 = 0xFF)].

#### 9.6.2.10 Modulation Limit Register (0x10)

The modulation limit is the maximum duty cycle of the PWM output waveform.

**Table 13. Modulation Limit Register (0x10)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | MODULATION LIMIT |
|---|---|---|---|---|---|---|---|---|
| – | – | – | – | – | 0 | 0 | 0 | 99.2% |
| – | – | – | – | – | 0 | 0 | 1 | 98.4% |
| – | – | – | – | – | **0** | **1** | **0** | **97.7%**(1) |
| – | – | – | – | – | 0 | 1 | 1 | 96.9% |
| – | – | – | – | – | 1 | 0 | 0 | 96.1% |
| – | – | – | – | – | 1 | 0 | 1 | 95.3% |
| – | – | – | – | – | 1 | 1 | 0 | 94.5% |
| – | – | – | – | – | 1 | 1 | 1 | 93.8% |
| 0 | 0 | 0 | 0 | 0 | – | – | – | Reserved |

(1) Default values are in **bold**.

### 9.6.2.11 Interchannel Delay Registers (0x11, 0x12, 0x13, and 0x14)

Internal PWM Channels 1, 2, $\overline{1}$, and $\overline{2}$ are mapped into registers 0x11, 0x12, 0x13, and 0x14.

**Table 14. Channel Interchannel Delay Registers (0x11, 0x12, 0x13, and 0x14)**

| BITS DEFINITION | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | 0 | 0 | – | – | Minimum absolute delay, 0 DCLK cycles |
| | 0 | 1 | 1 | 1 | 1 | 1 | – | – | Maximum positive delay, 31 × 4 DCLK cycles |
| | 1 | 0 | 0 | 0 | 0 | 0 | – | – | Maximum negative delay, –32 × 4 DCLK cycles |
| | | | | | | | 0 | 0 | Reserved |
| **SUBADDRESS** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **DELAY = (VALUE) × 4 DCLKs** |
| **0x11** | **1** | **0** | **1** | **0** | **1** | **1** | – | – | **Default value for channel 1** (1) |
| **0x12** | **0** | **1** | **0** | **1** | **0** | **1** | – | – | **Default value for channel 2** (1) |
| **0x13** | **1** | **0** | **1** | **0** | **1** | **1** | – | – | **Default value for $\overline{\text{channel 1}}$** (1) |
| **0x14** | **0** | **1** | **0** | **1** | **0** | **1** | – | – | **Default value for $\overline{\text{channel 2}}$** (1) |

(1) Default values are in **bold**.

ICD settings have high impact on audio performance (e.g., dynamic range, THD, crosstalk etc.). Therefore, appropriate ICD settings must be used. By default, the device has ICD settings for AD mode. If used in BD mode, then update these registers before coming out of all-channel shutdown.

| REGISTER | AD MODE | BD MODE |
|---|---|---|
| 0x11 | AC | B8 |
| 0x12 | 54 | 60 |
| 0x13 | AC | A0 |
| 0x14 | 54 | 48 |

### 9.6.2.12 PWM Shutdown Group Register (0x19)

Settings of this register determine which PWM channels are active. The value must be 0x30 for BTL mode and 0x3A for PBTL mode. The default value of this register is 0x30. The functionality of this register is tied to the state of bit D5 in the system control register.

This register defines which channels belong to the shutdown group (SDG). If a 1 is set in the shutdown group register, that particular channel is **not** started following an exit *out of all-channel shutdown* command (if bit D5 is set to 0 in system control register 2, 0x05).

**Table 15. Shutdown Group Register (0x19)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | – | – | – | – | – | – | – | **Reserved** (1) |
| – | **0** | – | – | – | – | – | – | **Reserved** (1) |
| – | – | **1** | – | – | – | – | – | **Reserved** (1) |
| – | – | – | **1** | – | – | – | – | **Reserved** (1) |
| – | – | – | – | **0** | – | – | – | **PWM channel 4 does not belong to shutdown group.** (1) |
| – | – | – | – | 1 | – | – | – | PWM channel 4 belongs to shutdown group. |
| – | – | – | – | – | **0** | – | – | **PWM channel 3 does not belong to shutdown group.** (1) |
| – | – | – | – | – | 1 | – | – | PWM channel 3 belongs to shutdown group. |
| – | – | – | – | – | – | **0** | – | **PWM channel 2 does not belong to shutdown group.** (1) |
| – | – | – | – | – | – | 1 | – | PWM channel 2 belongs to shutdown group. |
| – | – | – | – | – | – | – | **0** | **PWM channel 1 does not belong to shutdown group.** (1) |
| – | – | – | – | – | – | – | 1 | PWM channel 1 belongs to shutdown group. |

(1) Default values are in **bold**.

### 9.6.2.13 Start/Stop Period Register (0x1A)

This register is used to control the soft-start and soft-stop period following an enter/exit all channel shut down command or change in the $\overline{\text{PDN}}$ state. This helps reduce pops and clicks at start-up and shutdown. The times are only approximate and vary depending on device activity level and $I^2S$ clock stability.

**Table 16. Start/Stop Period Register (0x1A)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **–** | **–** | – | – | – | – | – | **SSTIMER enabled**(1) |
| 1 | – | – | – | – | – | – | – | SSTIMER disabled |
| – | **0** | **0** | – | – | – | – | – | **Reserved**(1) |
| – | – | – | 0 | 0 | – | – | – | No 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 0 | 0 | 0 | 16.5-ms 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 0 | 0 | 1 | 23.9-ms 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 0 | 1 | 0 | 31.4-ms 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 0 | 1 | 1 | 40.4-ms 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 1 | 0 | 0 | 53.9-ms 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 1 | 0 | 1 | 70.3-ms 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 1 | 1 | 0 | 94.2-ms 50% duty cycle start/stop period |
| – | – | – | **0** | **1** | **1** | **1** | **1** | **125.7-ms 50% duty cycle start/stop period**(1) |
| – | – | – | 1 | 0 | 0 | 0 | 0 | 164.6-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 0 | 0 | 1 | 239.4-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 0 | 1 | 0 | 314.2-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 0 | 1 | 1 | 403.9-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 1 | 0 | 0 | 538.6-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 1 | 0 | 1 | 703.1-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 1 | 1 | 0 | 942.5-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 1 | 1 | 1 | 1256.6-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 0 | 0 | 0 | 1728.1-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 0 | 0 | 1 | 2513.6-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 0 | 1 | 0 | 3299.1-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 0 | 1 | 1 | 4241.7-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 1 | 0 | 0 | 5655.6-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 1 | 0 | 1 | 7383.7-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 1 | 1 | 0 | 9897.3-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 1 | 1 | 1 | 13,196.4-ms 50% duty cycle start/stop period |

(1) Default values are in **bold**.

### 9.6.2.14 Oscillator Trim Register (0x1B)

The TAS5755M PWM processor contains an internal oscillator to support autodetect of $I^2S$ clock rates. This reduces system cost because an external reference is not required. Currently, TI recommends a reference resistor value of 18.2 kΩ (1%). This must be connected between OSC_RES and DVSSO.

Writing 0x00 to register 0x1B enables the trim that was programmed at the factory.

**NOTE**

Trim must always be run following reset of the device.

**Table 17. Oscillator Trim Register (0x1B)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | – | – | – | – | – | – | – | **Reserved**(1) |
| – | **0** | – | – | – | – | – | – | **Oscillator trim not done (read-only)**(1) |
| – | 1 | – | – | – | – | – | – | Oscillator trim done (read only) |
| – | – | **0** | **0** | **0** | **0** | – | – | **Reserved**(1) |
| – | – | – | – | – | – | 0 | – | Select factory trim (Write a 0 to select factory trim; default is 1.) |
| – | – | – | – | – | – | **1** | – | **Factory trim disabled**(1) |
| – | – | – | – | – | – | – | **0** | **Reserved**(1) |

(1) Default values are in **bold**.

### 9.6.2.15 BKND_ERR Register (0x1C)

When a back-end error signal is received from the internal power stage, the power stage is reset stopping all PWM activity. Subsequently, the modulator waits approximately for the time listed in Table 18 before attempting to re-start the power stage.

**Table 18. BKND_ERR Register (0x1C)(1)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | Reserved |
| – | – | – | – | **0** | **0** | **1** | **0** | **Set back-end reset period to 299 ms**(2) |
| – | – | – | – | 0 | 0 | 1 | 1 | Set back-end reset period to 449 ms |
| – | – | – | – | 0 | 1 | 0 | 0 | Set back-end reset period to 598 ms |
| – | – | – | – | 0 | 1 | 0 | 1 | Set back-end reset period to 748 ms |
| – | – | – | – | 0 | 1 | 1 | 0 | Set back-end reset period to 898 ms |
| – | – | – | – | 0 | 1 | 1 | 1 | Set back-end reset period to 1047 ms |
| – | – | – | – | 1 | 0 | 0 | 0 | Set back-end reset period to 1197 ms |
| – | – | – | – | 1 | 0 | 0 | 1 | Set back-end reset period to 1346 ms |
| – | – | – | – | 1 | 0 | 1 | X | Set back-end reset period to 1496 ms |
| – | – | – | – | 1 | 1 | X | X | Set back-end reset period to 1496 ms |

(1) This register can be written only with a "non-Reserved" value. Also this register can be written once after the reset.
(2) Default values are in **bold**.

### 9.6.2.16 Input Multiplexer Register (0x20)

This register controls the modulation scheme (AD or BD mode) as well as the routing of $I^2S$ audio to the internal channels.

**Table 19. Input Multiplexer Register (0x20)**

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Reserved**(1) |
| **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** | **FUNCTION** |
| **0** | – | – | – | – | – | – | – | **Channel-1 AD mode**(1) |
| 1 | – | – | – | – | – | – | – | Channel-1 BD mode |
| – | **0** | **0** | **0** | – | – | – | – | **SDIN-L to channel 1**(1) |
| – | 0 | 0 | 1 | – | – | – | – | SDIN-R to channel 1 |
| – | 0 | 1 | 0 | – | – | – | – | Reserved |
| – | 0 | 1 | 1 | – | – | – | – | Reserved |
| – | 1 | 0 | 0 | – | – | – | – | Reserved |
| – | 1 | 0 | 1 | – | – | – | – | Reserved |
| – | 1 | 1 | 0 | – | – | – | – | Ground (0) to channel 1 |
| – | 1 | 1 | 1 | – | – | – | – | Reserved |
| – | – | – | – | **0** | – | – | – | **Channel 2 AD mode**(1) |
| – | – | – | – | 1 | – | – | – | Channel 2 BD mode |
| – | – | – | – | – | 0 | 0 | 0 | SDIN-L to channel 2 |
| – | – | – | – | – | **0** | **0** | **1** | **SDIN-R to channel 2**(1) |
| – | – | – | – | – | 0 | 1 | 0 | Reserved |
| – | – | – | – | – | 0 | 1 | 1 | Reserved |
| – | – | – | – | – | 1 | 0 | 0 | Reserved |
| – | – | – | – | – | 1 | 0 | 1 | Reserved |
| – | – | – | – | – | 1 | 1 | 0 | Ground (0) to channel 2 |
| – | – | – | – | – | 1 | 1 | 1 | Reserved |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **FUNCTION** |
| **0** | **1** | **1** | **1** | **0** | **1** | **1** | **1** | **Reserved**(1) |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **FUNCTION** |
| **0** | **1** | **1** | **1** | **0** | **0** | **1** | **0** | **Reserved**(1) |

(1) Default values are in **bold**.

### 9.6.2.17 Channel 4 Source Select Register (0x21)

This register selects the channel 4 source.

**Table 20. Subchannel Control Register (0x21)**

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Reserved**(1) |
| **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** | **FUNCTION** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Reserved**(1) |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **FUNCTION** |
| **0** | **1** | **0** | **0** | **0** | **0** | **1** | 1 | **Select SDIN path (third path), not available in TAS5755M**(1) |
| – | – | – | – | – | – | **–** | 0 | (L + R)/2 |
| – | – | – | – | – | – | 0 | **1** | **Left-channel post-BQ**(1) |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **FUNCTION** |
| **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **Reserved**(1) |

(1) Default values are in **bold**.

### 9.6.2.18 PWM Output Mux Register (0x25)

This DAP output mux selects which internal PWM channel is output to the external pins. Any channel can be output to any external output pin.

Bits D21–D20: Selects which PWM channel is output to OUT_A
Bits D17–D16: Selects which PWM channel is output to OUT_B
Bits D13–D12: Selects which PWM channel is output to OUT_C
Bits D09–D08: Selects which PWM channel is output to OUT_D

**NOTE**
Channels are encoded so that channel 1 = 0x00, channel 2 = 0x01, …, channel 4 = 0x03.

**Table 21. PWM Output Mux Register (0x25)**

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **Reserved**(1) |
| **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** | **FUNCTION** |
| **0** | **0** | – | – | – | – | – | – | **Reserved**(1) |
| **–** | **–** | **0** | **0** | – | – | – | – | **Multiplex PWM 1 to OUT_A**(1) |
| – | – | 0 | 1 | – | – | – | – | Multiplex PWM 2 to OUT_A |
| – | – | 1 | 0 | – | – | – | – | Multiplex PWM 3 to OUT_A |
| – | – | 1 | 1 | – | – | – | – | Multiplex PWM 4 to OUT_A |
| – | – | – | – | **0** | **0** | – | – | **Reserved**(1) |
| – | – | – | – | – | – | 0 | 0 | Multiplex PWM 1 to OUT_B |
| – | – | – | – | – | – | 0 | 1 | Multiplex PWM 2 to OUT_B |
| – | – | – | – | – | – | **1** | **0** | **Multiplex PWM 3 to OUT_B**(1) |
| – | – | – | – | – | – | 1 | 1 | Multiplex PWM 4 to OUT_B |

(1) Default values are in **bold**.

**Table 21. PWM Output Mux Register (0x25) (continued)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | – | – | – | – | – | – | **Reserved**(1) |
| – | – | 0 | 0 | – | – | – | – | Multiplex PWM 1 to OUT_C |
| – | – | **0** | **1** | – | – | – | – | **Multiplex PWM 2 to OUT_C**(1) |
| – | – | 1 | 0 | – | – | – | – | Multiplex PWM 3 to OUT_C |
| – | – | 1 | 1 | – | – | – | – | Multiplex PWM 4 to OUT_C |
| – | – | – | – | **0** | **0** | – | – | **Reserved**(1) |
| – | – | – | – | – | – | 0 | 0 | Multiplex PWM 1 to OUT_D |
| – | – | – | – | – | – | 0 | 1 | Multiplex PWM 2 to OUT_D |
| – | – | – | – | – | – | 1 | 0 | Multiplex PWM 3 to OUT_D |
| – | – | – | – | – | – | **1** | **1** | **Multiplex PWM 4 to OUT_D**(1) |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **FUNCTION** |
| **0** | **1** | **0** | **0** | **0** | **1** | **0** | **1** | **Reserved**(1) |

### *9.6.2.19 DRC Control Register (0x46)*

Each DRC can be enabled independently using the DRC control register. The DRCs are disabled by default.

**Table 22. DRC Control Register (0x46)**

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Reserved**(1) |
| **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** | **FUNCTION** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Reserved** (1) |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **FUNCTION** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Reserved**(1) |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **FUNCTION** |
| **0** | **0** | **–** | **–** | – | – | – | – | **Reserved**(1) |
| – | – | 0 | – | – | – | – | – | Disable complementary (1 - H) low-pass filter generation |
| – | – | 1 | – | – | – | – | – | Enable complementary (1 - H) low-pass filter generation |
| – | – | – | **0** | – | – | – | – | |
| – | – | – | 1 | – | – | – | – | |
| | | | | **0** | **0** | | | **Reserved**(1) |
| – | – | – | – | – | – | **0** | – | **DRC2 turned OFF**(1) |
| – | – | – | – | – | – | 1 | – | DRC2 turned ON |
| – | – | – | – | – | – | – | **0** | **DRC1 turned OFF**(1) |
| – | – | – | – | – | – | – | 1 | DRC1 turned ON |

(1) Default values are in **bold**.

### 9.6.2.20 Bank Switch and EQ Control Register (0x50)

**Table 23. Bank Switching Command Register (0x50)**

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | – | – | – | – | – | – | – | **32 kHz, does not use bank 3**(1) |
| 1 | – | – | – | – | – | – | – | 32 kHz, uses bank 3 |
| – | **0** | – | – | – | – | – | – | **Reserved**(1) |
| – | – | **0** | – | – | – | – | – | **Reserved**(1) |
| – | – | – | **0** | – | – | – | – | **44.1/48 kHz, does not use bank 3**(1) |
| – | – | – | 1 | – | – | – | – | 44.1/48 kHz, uses bank 3 |
| – | – | – | – | 0 | – | – | – | 16 kHz, does not use bank 3 |
| – | – | – | – | **1** | – | – | – | **16 kHz, uses bank 3**(1) |
| – | – | – | – | – | 0 | – | – | 22.025/24 kHz, does not use bank 3 |
| – | – | – | – | – | **1** | – | – | **22.025/24 kHz, uses bank 3**(1) |
| – | – | – | – | – | – | 0 | – | 8 kHz, does not use bank 3 |
| – | – | – | – | – | – | **1** | – | **8 kHz, uses bank 3**(1) |
| – | – | – | – | – | – | – | 0 | 11.025 kHz/12, does not use bank 3 |
| – | – | – | – | – | – | – | **1** | **11.025/12 kHz, uses bank 3**(1) |
| **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** | **FUNCTION** |
| **0** | – | – | – | – | – | – | – | **32 kHz, does not use bank 2**(1) |
| 1 | – | – | – | – | – | – | – | 32 kHz, uses bank 2 |
| – | **1** | – | – | – | – | – | – | **Reserved**(1) |
| – | – | **1** | – | – | – | – | – | **Reserved**(1) |
| – | – | – | 0 | – | – | – | – | 44.1/48 kHz, does not use bank 2 |
| – | – | – | **1** | – | – | – | – | **44.1/48 kHz, uses bank 2**(1) |
| – | – | – | – | **0** | – | – | – | **16 kHz, does not use bank 2**(1) |
| – | – | – | – | 1 | – | – | – | 16 kHz, uses bank 2 |
| – | – | – | – | – | **0** | – | – | **22.025/24 kHz, does not use bank 2**(1) |
| – | – | – | – | – | 1 | – | – | 22.025/24 kHz, uses bank 2 |
| – | – | – | – | – | – | **0** | – | **8 kHz, does not use bank 2**(1) |
| – | – | – | – | – | – | 1 | – | 8 kHz, uses bank 2 |
| – | – | – | – | – | – | – | **0** | **11.025/12 kHz, does not use bank 2**(1) |
| – | – | – | – | – | – | – | 1 | 11.025/12 kHz, uses bank 2 |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **FUNCTION** |
| 0 | – | – | – | – | – | – | – | 32 kHz, does not use bank 1 |
| **1** | – | – | – | – | – | – | – | **32 kHz, uses bank 1**(1) |
| – | **0** | – | – | – | – | – | – | **Reserved**(1) |
| – | – | **0** | – | – | – | – | – | **Reserved**(1) |
| – | – | – | **0** | – | – | – | – | **44.1/48 kHz, does not use bank 1**(1) |
| – | – | – | 1 | – | – | – | – | 44.1/48 kHz, uses bank 1 |
| – | – | – | – | **0** | – | – | – | **16 kHz, does not use bank 1**(1) |
| – | – | – | – | 1 | – | – | – | 16 kHz, uses bank 1 |
| – | – | – | – | – | **0** | – | – | **22.025/24 kHz, does not use bank 1**(1) |
| – | – | – | – | – | 1 | – | – | 22.025/24 kHz, uses bank 1 |
| – | – | – | – | – | – | **0** | – | **8 kHz, does not use bank 1**(1) |
| – | – | – | – | – | – | 1 | – | 8 kHz, uses bank 1 |
| – | – | – | – | – | – | – | **0** | **11.025/12 kHz, does not use bank 1**(1) |
| – | – | – | – | – | – | – | 1 | 11.025/12 kHz, uses bank 1 |

(1) Default values are in **bold**.

**Table 23. Bank Switching Command Register (0x50) (continued)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | | | | | | | | **EQ ON** |
| 1 | – | – | – | – | – | – | – | EQ OFF (bypass BQ 0-7 of channels 1 and 2) |
| – | **0** | – | – | – | – | – | – | **Reserved**(1) |
| – | – | **0** | – | – | – | – | – | **Ignore bank-mapping in bits D31–D8.Use default mapping.**(1) |
| | | 1 | | | | | | Use bank-mapping in bits D31–D8. |
| – | – | – | **0** | – | – | – | – | **L and R can be written independently.**(1) |
| – | – | – | 1 | – | – | – | – | L and R are ganged for EQ biquads; a write to left-channel BQ is also written to right-channel BQ. (0x29–0x2F is ganged to 0x30–0x36.Also 0x58–0x59 is ganged to 0x5C–0x5D) |
| – | – | **–** | **–** | **0** | – | – | – | **Reserved**(1) |
| – | – | – | – | – | **0** | **0** | **0** | **No bank switching. All updates to DAP**(1) |
| – | – | – | – | – | 0 | 0 | 1 | Configure bank 1 (32 kHz by default) |
| – | – | – | – | – | 0 | 1 | 0 | Configure bank 2 (44.1/48 kHz by default) |
| – | – | – | – | – | 0 | 1 | 1 | Configure bank 3 (other sample rates by default) |
| – | – | – | – | – | 1 | 0 | 0 | Automatic bank selection |
| – | – | – | – | – | 1 | 0 | 1 | Reserved |
| – | – | – | – | – | 1 | 1 | X | Reserved |

# 10 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

Figure 68, Figure 71, and Figure 72 highlight the required external components and system level connections for proper operation of the device in several popular use cases.

Each of these configurations can be realized using the Evaluation Modules (EVMs) for the device. These flexible modules allow full evaluation of the device in the most common modes of operation. Any design variation can be supported by TI through schematic and layout reviews. Visit http://e2e.ti.com for design assistance and join the audio amplifier discussion forum for additional information.

## 10.2 Typical Applications

### 10.2.1 Stereo Bridge Tied Load Application

A stereo system generally refers to a system in which there are two full range speakers without a separate amplifier path for the speakers that reproduce the low-frequency content. In this system, two channels are presented to the amplifier via the digital input signal. These two channels are amplified and then sent to two separate speakers.

Most commonly, the two channels are a pair of signals called a stereo pair, with one channel containing the audio for the left channel and the other channel containing the audio for the right channel.

The Stereo BTL Configuration with Headphone and Line Driver Amplifier application is shown in Figure 68.

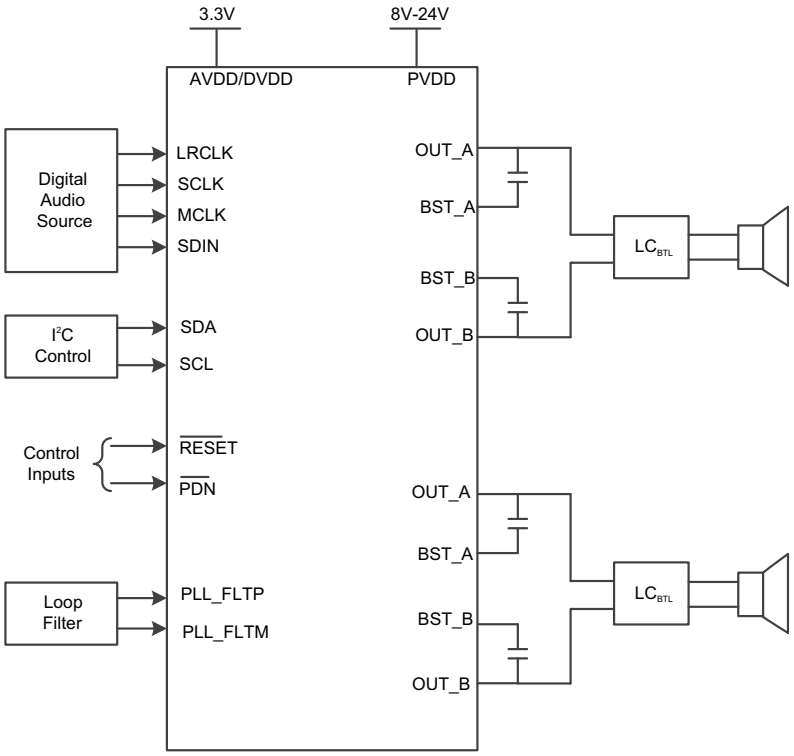





**Figure 68. Stereo Bridge Tied Load Application**

## Typical Applications (continued)

### *10.2.1.1 Design Requirements*

**Table 24. Design Requirements**

| PARAMETER | EXAMPLE |
|---|---|
| Low Power Supply | 3.3 V |
| High Power Supply | 8 V to 24 V |
| Host Processor | $I^2S$ Compliant Master |
| | $I^2C$ Compliant Master |
| | GPIO Control |
| Output Filters | Inductor-Capacitor Low Pass Filter |
| Speaker | 4 Ω minimum |

### *10.2.1.2 Detailed Design Procedure*

#### 10.2.1.2.1 Component Selection and Hardware Connections

The typical connections required for proper operation of the device can be found in the *TAS5755EVM User's Guide* (SLOU481A). The device was tested with this list of components; deviation from this list of typical application components, unless recommended by this document, may produce unwanted results, which could range from degradation of audio performance to destructive failure of the device.

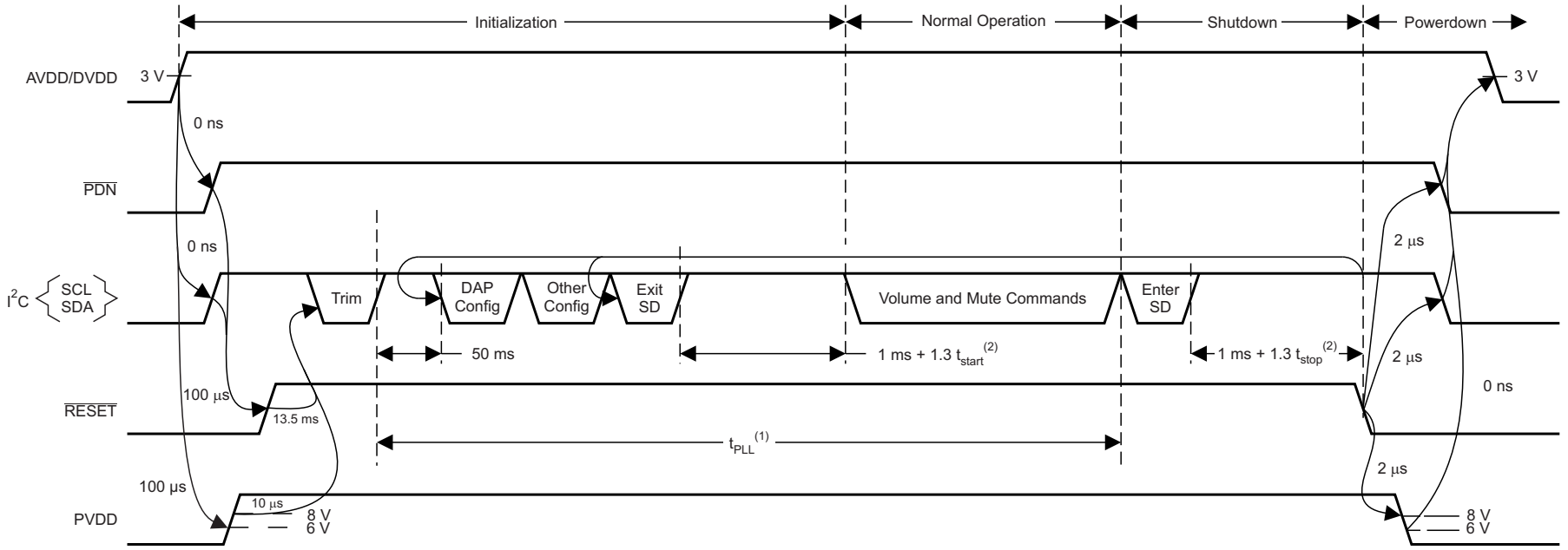
#### 10.2.1.2.2 $I^2C$ Pullup Resistors

Customary pullup resistors are required on the SCL and SDA signal lines. They are not shown in the Typical Application Circuits, because they are shared by all of the devices on the $I^2C$ bus and are considered to be part of the associated passive components for the System Processor. These resistor values must be chosen per the guidance provided in the $I^2C$ Specification.

#### 10.2.1.2.3 Digital I/O Connectivity

The digital I/O lines of the TAS5755M are described in previous sections. As discussed, whenever a static digital pin (that is a pin that is hardwired to be HIGH or LOW) is required to be pulled HIGH, it must be connected to DVDD through a pullup resistor to control the slew rate of the voltage presented to the digital I/O pins. It is not, however, necessary to have a separate pullup resistor for each static digital I/O line. Instead, a single resistor can be used to tie all static I/O lines HIGH to reduce BOM count.

#### 10.2.1.2.4 Recommended Start-Up and Shutdown Procedures




(1) $t_{PLL}$ has to be greater than 240 ms + 1.3 $t_{start}$.
This constraint only applies to the first trim command following AVDD/DVDD power-up.
It does not apply to trim commands following subsequent resets.
(2) $t_{start}$/$t_{stop}$ = PWM start/stop time as defined in register 0X1A

T0419-06

**Figure 69. Recommended Command Sequence**

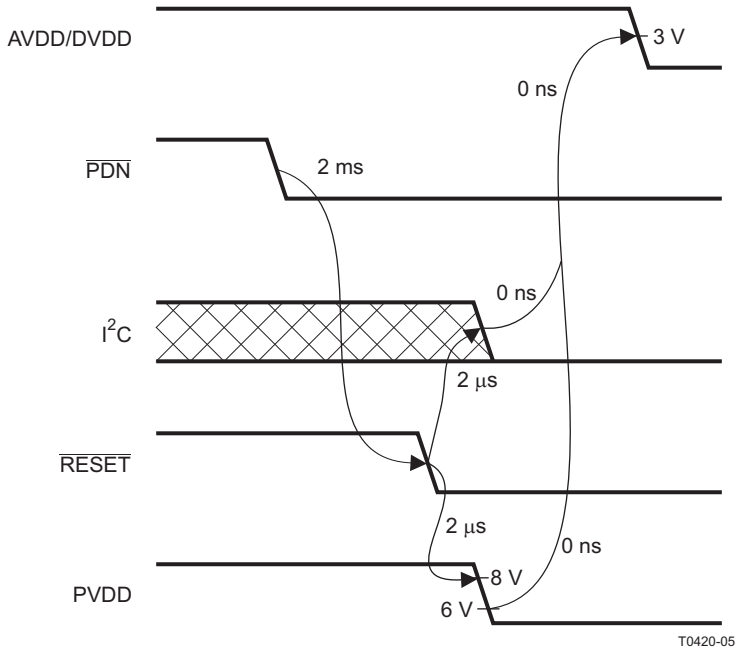



**Figure 70. Power-Loss Sequence**

#### *10.2.1.2.4.1 Initialization Sequence*

Use the following sequence to power up and initialize the device:

1. Hold all digital inputs low and ramp up AVDD/DVDD to at least 3 V.
2. Initialize digital inputs and PVDD supply as follows:
   - Drive $\overline{\text{RESET}}$ = 0, $\overline{\text{PDN}}$ = 1, and other digital inputs to their desired state while ensuring that all are never more than 2.5 V above AVDD/DVDD. Wait at least 100 µs, drive $\overline{\text{RESET}}$ = 1, and wait at least another 13.5 ms.
   - Ramp up PVDD to at least 8 V while ensuring that it remains below 6 V for at least 100 µs after AVDD/DVDD reaches 3 V. Then wait at least another 10 µs.
3. Trim oscillator (write 0x00 to register 0x1B) and wait at least 50 ms.
4. Configure the DAP via $I^2C$, see *TAS5755EVM Evaluation Module User's Guide* (SLOU481A) for typical values.
5. Configure remaining registers.
6. Exit shutdown (sequence defined in *Shutdown Sequence*).

#### *10.2.1.2.4.2 Normal Operation*

The following are the only events supported during normal operation:

1. Writes to master/channel volume registers
2. Writes to soft-mute register
3. Enter and exit shutdown (sequence defined in *Shutdown Sequence*)

**NOTE**

Event 3 is not supported for 240 ms + 1.3 × $t_{start}$ after trim following AVDD/DVDD power-up ramp (where $t_{start}$ is specified by register 0x1A).

#### 10.2.1.2.4.3 Shutdown Sequence

Enter:

1. Write 0x40 to register 0x05.
2. Wait at least 1 ms + 1.3 × $t_{stop}$ (where $t_{stop}$ is specified by register 0x1A).
3. If desired, reconfigure by returning to step 4 of initialization sequence.

Exit:

1. Write 0x00 to register 0x05 (exit shutdown command may not be serviced for as much as 240 ms after trim following AVDD/DVDD power-up ramp).
2. Wait at least 1 ms + 1.3 × $t_{start}$ (where $t_{start}$ is specified by register 0x1A).
3. Proceed with normal operation.

#### 10.2.1.2.4.4 Power-Down Sequence

Use the following sequence to power down the device and its supplies:

1. If time permits, enter shutdown (sequence defined in *Shutdown Sequence*); else, in case of sudden power loss, assert $\overline{PDN}$ = 0 and wait at least 2 ms.
2. Assert $\overline{RESET}$ = 0.
3. Drive digital inputs low and ramp down PVDD supply as follows:
   - Drive all digital inputs low after $\overline{RESET}$ has been low for at least 2 µs.
   - Ramp down PVDD while ensuring that it remains above 8 V until $\overline{RESET}$ has been low for at least 2 µs.
4. Ramp down AVDD/DVDD while ensuring that it remains above 3 V until PVDD is below 6 V and that it is never more than 2.5 V below the digital inputs.

### 10.2.1.3 Application Curves

**Table 25. Relevant Performance Curves**

| CURVE TITLE | FIGURE |
|---|---|
| Output Power vs Supply Voltage (2.0 BTL Mode)<br>With 4Ω Load on Typical 2 Layer PCB Device May Be Thermally Limited Above 20 V | Figure 18 |
| Total Harmonic Distortion + Noise vs Output Power (2.0 BTL Mode) | Figure 19 |
| Total Harmonic Distortion + Noise vs Output Power (2.0 BTL Mode) | Figure 20 |
| Total Harmonic Distortion + Noise vs Output Power (2.0 BTL Mode) | Figure 21 |
| Total Harmonic Distortion vs Frequency (2.0 BTL Mode) | Figure 22 |
| Total Harmonic Distortion vs Frequency (2.0 BTL Mode) | Figure 23 |
| Total Harmonic Distortion vs Frequency (2.0 BTL Mode) | Figure 24 |
| Efficiency vs Output Power (2.0 BTL Mode) | Figure 25 |
| Crosstalk vs Frequency (2.0 BTL Mode) | Figure 26 |
| Crosstalk vs Frequency (2.0 BTL Mode) | Figure 27 |
| Crosstalk vs Frequency (2.0 BTL Mode) | Figure 28 |
| Crosstalk vs Frequency (2.0 BTL Mode) | Figure 29 |
| Power vs Supply Voltage (2.0 BTL Mode) | Figure 30 |
| Idle Channel Noise vs Supply Voltage (2.0 BTL Mode) | Figure 31 |

### 10.2.2 Mono Parallel Bridge Tied Load Application

A mono system refers to a system in which the amplifier is used to drive a single loudspeaker. Parallel Bridge Tied Load (PBTL) indicates that the two full-bridge channels of the device are placed in parallel and drive the loudspeaker simultaneously using an identical audio signal. The primary benefit of operating the TAS5755M device in PBTL operation is to reduce the power dissipation and increase the current sourcing capabilities of the amplifier output. In this mode of operation, the current limit of the audio amplifier is approximately doubled while the on-resistance is approximately halved.

The loudspeaker can be a full-range transducer or one that only reproduces the low-frequency content of an audio signal, as in the case of a powered subwoofer. Often in this use case, two stereo signals are mixed together and sent through a low-pass filter in order to create a single audio signal which contains the low frequency information of the two channels.

The Mono Parallel Bridge Tied Load application is shown in Figure 71.

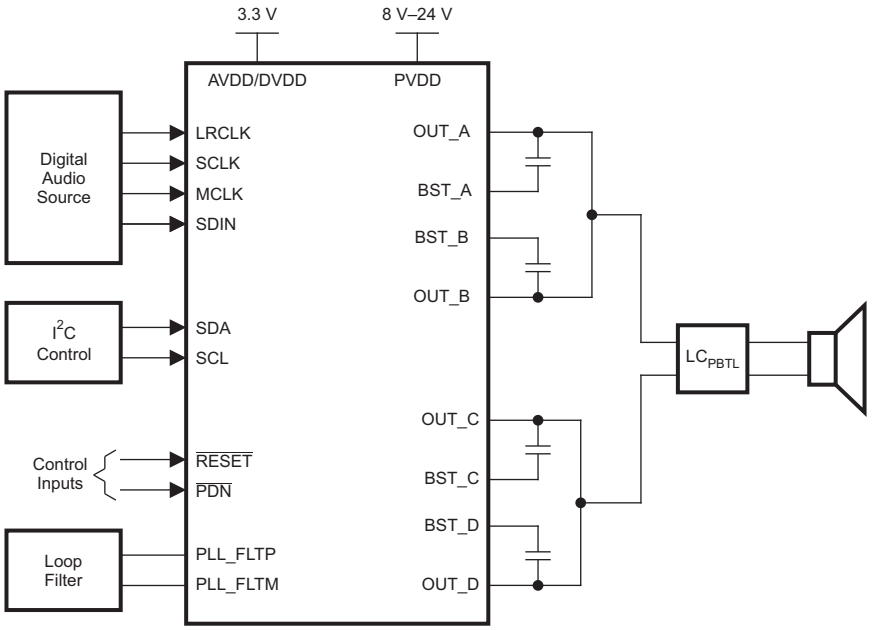





**Figure 71. Mono Parallel Bridge Tied Load Application**

#### 10.2.2.1 Design Requirements

**Table 26. Design Requirements**

| PARAMETER | EXAMPLE |
|---|---|
| Low Power Supply | 3.3 V |
| High Power Supply | 8 V to 24 V |
| Host Processor | $I^2S$ Compliant Master |
| | $I^2C$ Compliant Master |
| | GPIO Control |
| Output Filters | Inductor-Capacitor Low Pass Filter |
| Speaker | 4 Ω minimum |

#### 10.2.2.2 Detailed Design Procedure

Refer to *Detailed Design Procedure* for information.

#### 10.2.2.3 Application Curves

**Table 27. Relevant Performance Curves**

| CURVE TITLE | FIGURE |
|---|---|
| Output Power vs Supply Voltage (PBTL Mode)<br>With 2Ω Load on Typical 2 Layer PCB, Device May Be Thermally Limited Above 20 V | Figure 32 |
| Total Harmonic Distortion + Noise vs Output Power (PBTL Mode) | Figure 33 |
| Total Harmonic Distortion + Noise vs Output Power (PBTL Mode) | Figure 34 |
| Total Harmonic Distortion + Noise vs Output Power (PBTL Mode) | Figure 35 |
| Total Harmonic Distortion vs Frequency (PBTL Mode) | Figure 36 |
| Total Harmonic Distortion vs Frequency (PBTL Mode) | Figure 37 |
| Total Harmonic Distortion vs Frequency (PBTL Mode) | Figure 38 |
| Efficiency vs Output Power (PBTL Mode) | Figure 39 |
| Efficiency vs Output Power (PBTL Mode) | Figure 40 |
| Power vs Supply Voltage (PBTL Mode) | Figure 41 |
| Idle Channel Noise vs Supply Voltage (PBTL Mode) | Figure 42 |

### 10.2.3 2.1 Application

A 2.1 system generally refers to a system in which there are two full range speakers with a separate amplifier path for the speakers which reproduce the low-frequency content. In this system, two channels are presented to the amplifier via the digital input signal, these are driven into two single-ended speakers and are mixed into a third channel, conditioned to stream low-frequency content into a differentially connected speaker.

The 2.1 application is shown in Figure 72.

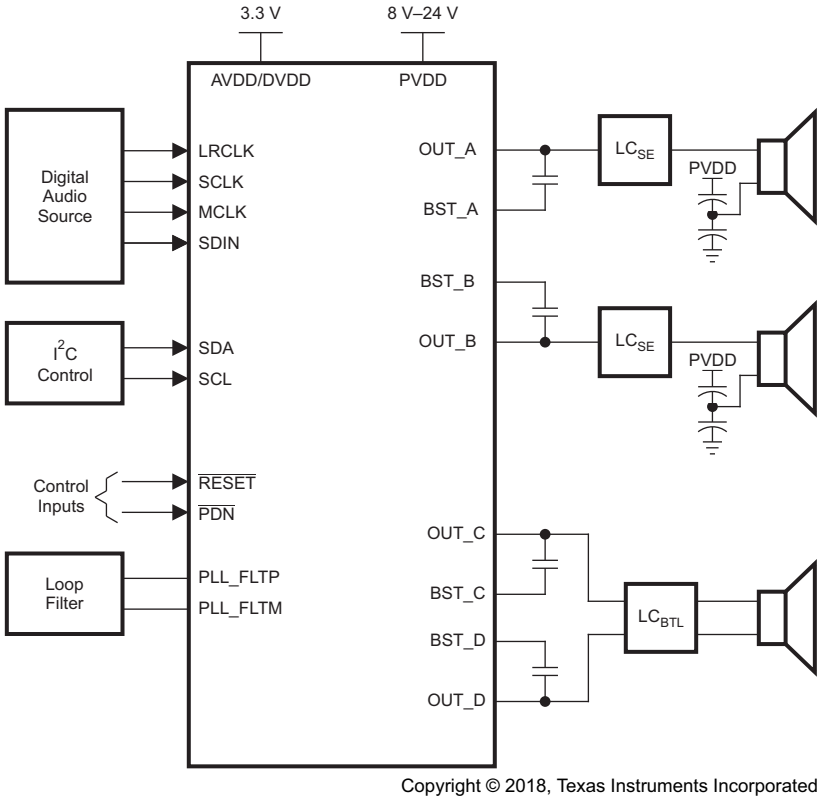



**Figure 72. Simplified 2.1 Application Diagram**

#### *10.2.3.1 Design Requirements*

**Table 28. Design Requirements**

| PARAMETER | EXAMPLE |
|---|---|
| Low Power Supply | 3.3 V |
| High Power Supply | 8 V to 24 V |
| Host Processor | $I^2S$ Compliant Master |
| | $I^2C$ Compliant Master |
| | GPIO Control |
| Output Filters | Inductor-Capacitor Low Pass Filter |
| Speaker | 4 Ω (BTL), 2 Ω (SE) minimum |

#### 10.2.3.2 Detailed Design Procedure

Refer to *Detailed Design Procedure* for information.

#### 10.2.3.3 Application Curves

**Table 29. Relevant Performance Curves**

| CURVE TITLE | FIGURE |
|---|---|
| Output Power vs Supply Voltage (2.1 SE Mode)<br>With 2 × 4Ω + 4Ω Load on Typical 2 Layer PCB Device May Be Thermally Limited Above 20 V | Figure 5 |
| Total Harmonic Distortion + Noise vs Output Power (2.1 SE Mode) | Figure 6 |
| Total Harmonic Distortion + Noise vs Output Power (2.1 SE Mode) | Figure 7 |
| Total Harmonic Distortion + Noise vs Output Power (2.1 SE Mode) | Figure 8 |
| Total Harmonic Distortion + Noise vs Frequency (2.1 SE Mode) | Figure 9 |
| Total Harmonic Distortion + Noise vs Frequency (2.1 SE Mode) | Figure 10 |
| Total Harmonic Distortion + Noise vs Frequency (2.1 SE Mode) | Figure 11 |
| Efficiency vs Total Output Power (2.1 SE Mode) | Figure 12 |
| Efficiency vs Total Output Power (2.1 SE Mode) | Figure 13 |
| Crosstalk vs Frequency (2.1 SE Mode) | Figure 14 |
| Crosstalk vs Frequency (2.1 SE Mode) | Figure 15 |
| Crosstalk vs Frequency (2.1 SE Mode) | Figure 16 |
| Crosstalk vs Frequency (2.1 SE Mode) | Figure 17 |

# 11 Power Supply Recommendations

The TAS5755M requires two power supplies; a low voltage 3.3 V nominal for the pins DVDD, AVDD, and DRVDD and a high power supply, 8 V to 24 V for the pin PVDD. There is no requirement for power up sequencing of low and high power supplies, however is recommended to put the PDN pin to low before removing the low voltage power supplies in order to protect the outputs.

## 11.1 DVDD and AVDD Supplies

The AVDD Supply is used to power the analog internal circuit of the device, and needs a well regulated and filtered 3.3-V supply voltage. The DVDD Supply is used to power the digital circuitry. DVDD needs a well regulated and filtered 3.3-V supply voltage.

## 11.2 PVDD Power Supply

The TAS5755M class-D audio amplifier requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) and noise is as low as possible. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 µF, placed as close as possible to the device PVDD leads works best. For filtering lower frequency noise signals, a 10 µF or greater capacitor placed near the audio power amplifier is recommended.

# 12 Layout

## 12.1 Layout Guidelines

Class-D switching edges are fast and switched currents are high so it is necessary to take care when planning the layout of the printed circuit board. The following suggestions will help to meet audio, thermal and EMC requirements.

- Decoupling capacitors: the high-frequency decoupling capacitors must be placed as close to the supply pins as possible; on the TAS5755M a 1-µF high-quality ceramic capacitor is used. Large (10 µF or greater) bulk power supply decoupling capacitors must be placed near the TAS5755M on the PVDD supplies.
- Keep the current loop from each of the outputs through the output inductor and the small filter cap and back to GND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Grounding: A big common GND plane is recommended. The PVDD decoupling capacitors must connect to GND. The TAS5755M PowerPAD must be connected to GND.
- Output filter: remember to select inductors that can handle the high short circuit current of the device. The LC filter must be placed close to the outputs.

The EVM product folder (TAS5755EVM) and User's Guide (SLOU481A) available on www.ti.com show schematic, bill of material, gerber files, and more detailed layout plots.

## 12.2 Layout Examples

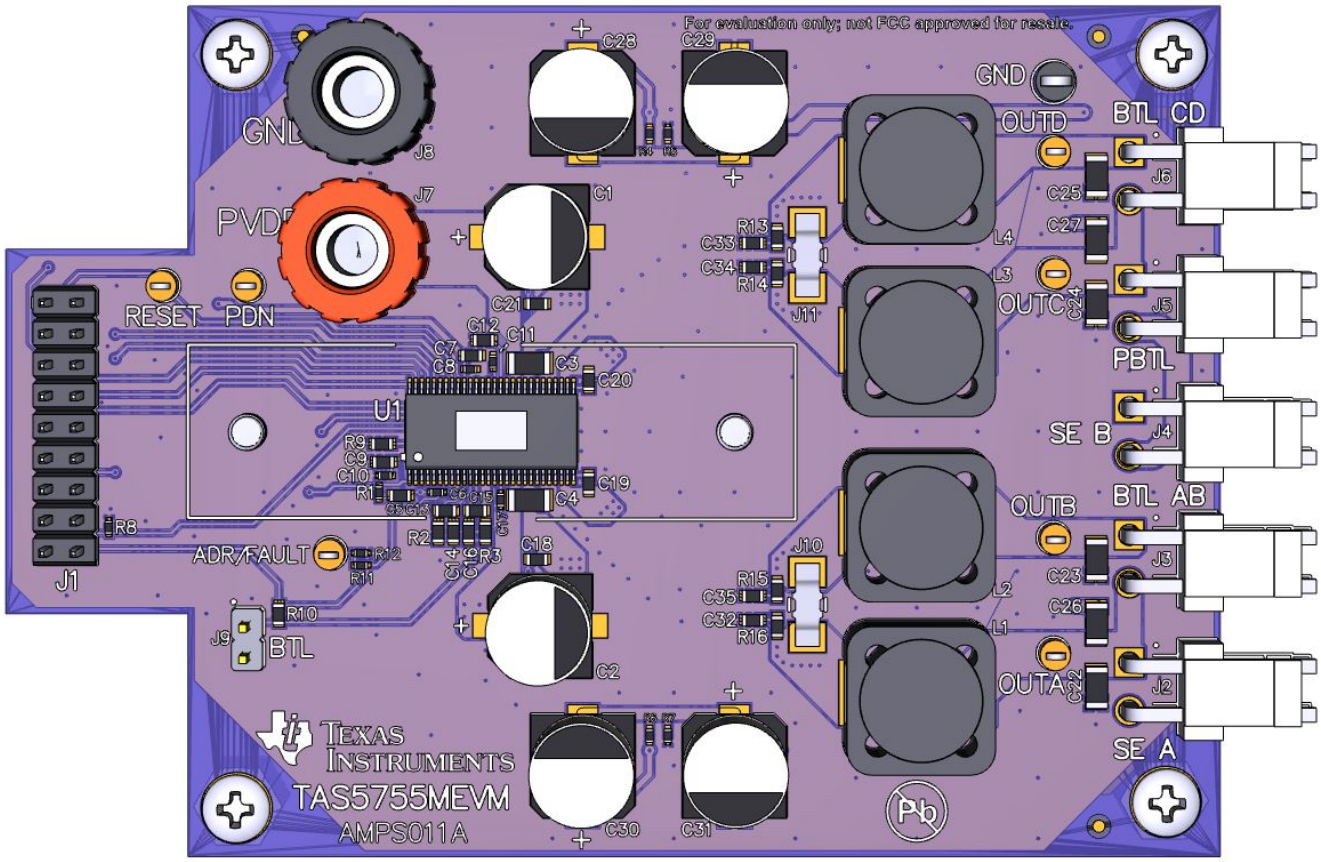



**Figure 73. Top Layer Layout with Stereo BTL Mode**

## Layout Examples (continued)

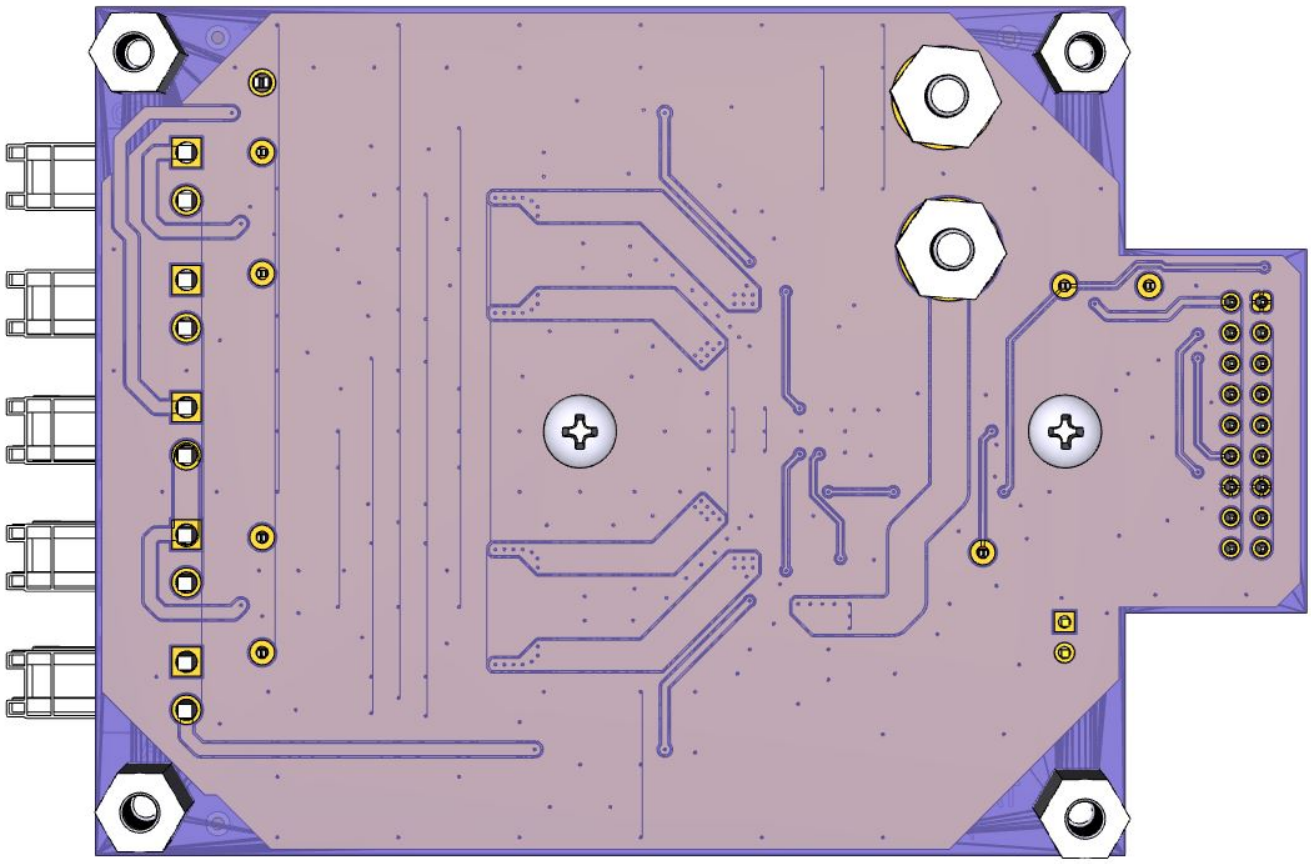


**Figure 74. Bottom Layer Layout with Stereo BTL Mode**

# 13 Device and Documentation Support

## 13.1 Device Support

### 13.1.1 Development Support

TAS570X GDE Software Setup development tool documentation (SLOC124)

## 13.2 Documentation Support

EVM product folder (TAS5755MEVM)

### 13.2.1 Related Documentation

TAS5755MEVM User's Guide (SLOU481A)

## 13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 13.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.

## 13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TAS5755MDFD | ACTIVE | HTSSOP | DFD | 56 | 35 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-4-260C-72 HR | 0 to 125 | 5755M | Samples |
| TAS5755MDFDR | ACTIVE | HTSSOP | DFD | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-4-260C-72 HR | 0 to 125 | 5755M | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

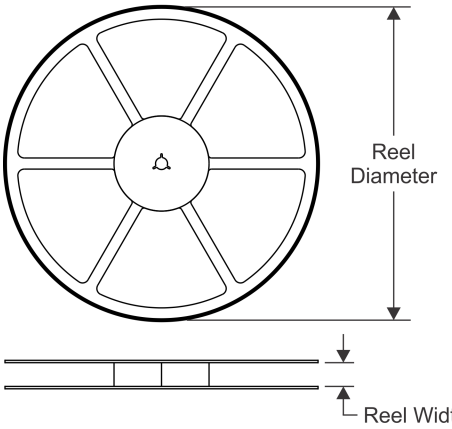
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

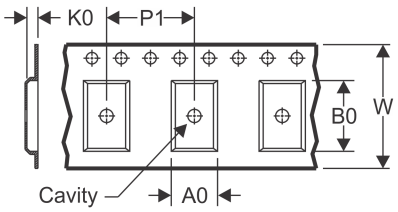
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

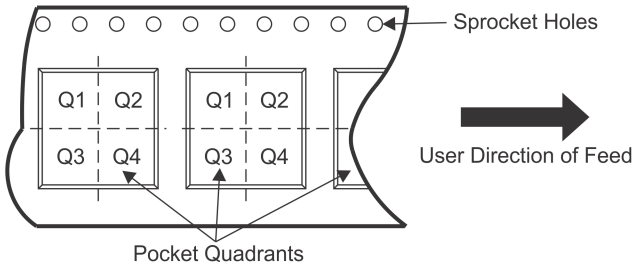



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

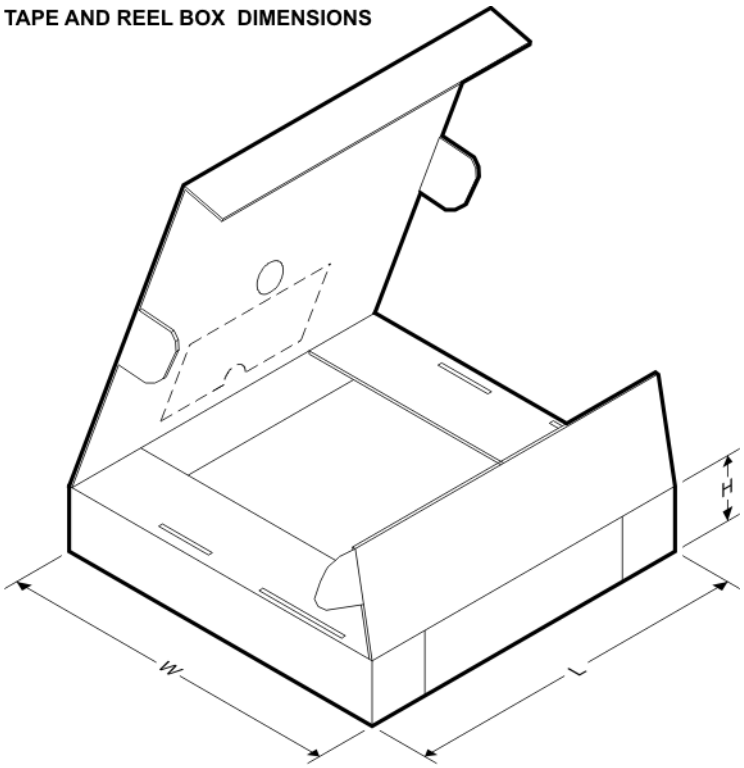
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TAS5755MDFDR | HTSSOP | DFD | 56 | 2000 | 330.0 | 24.4 | 8.6 | 15.6 | 1.8 | 12.0 | 24.0 | Q1 |

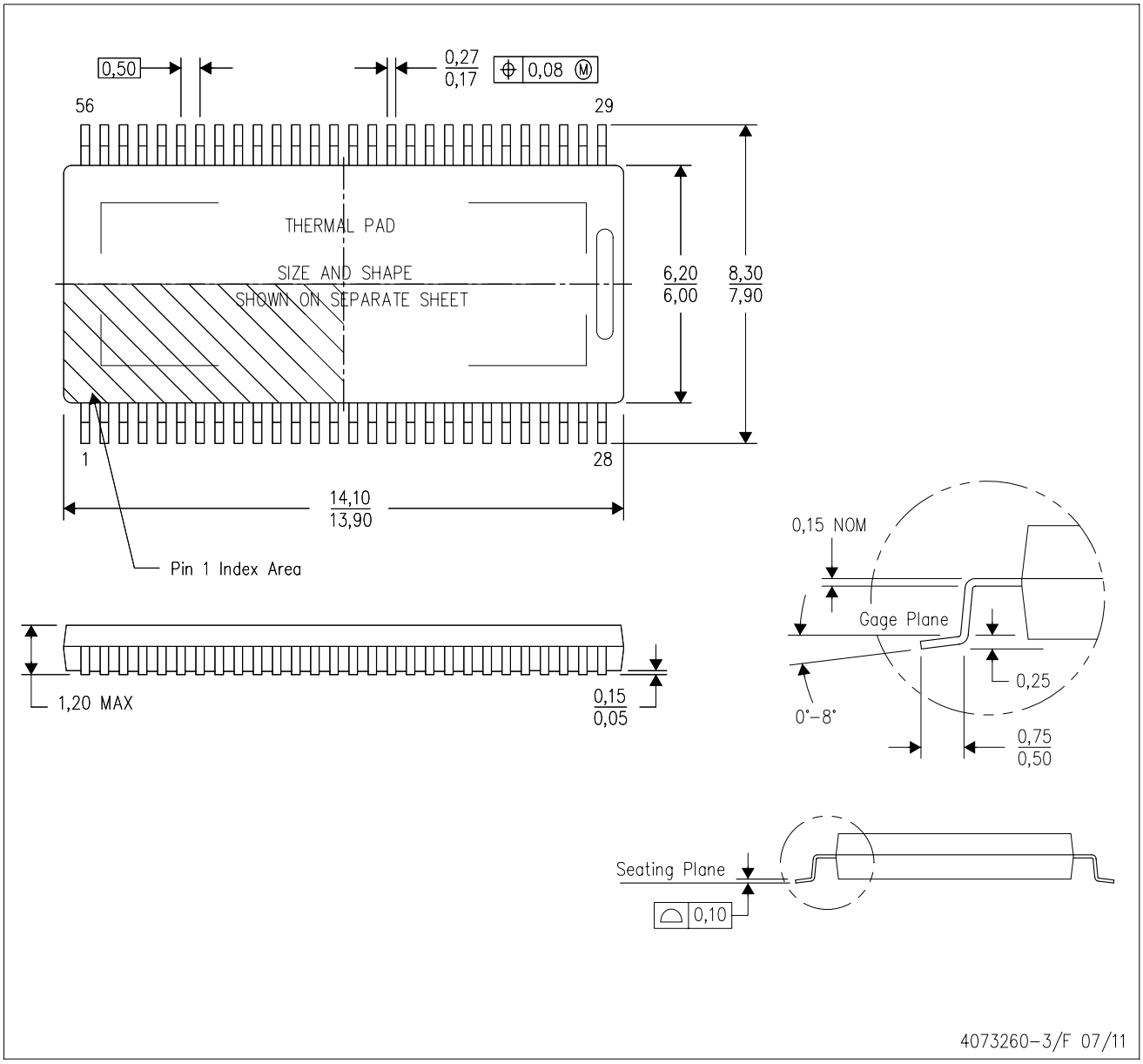
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TAS5755MDFDR | HTSSOP | DFD | 56 | 2000 | 367.0 | 367.0 | 45.0 |

DFD (R–PDSO–G56) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

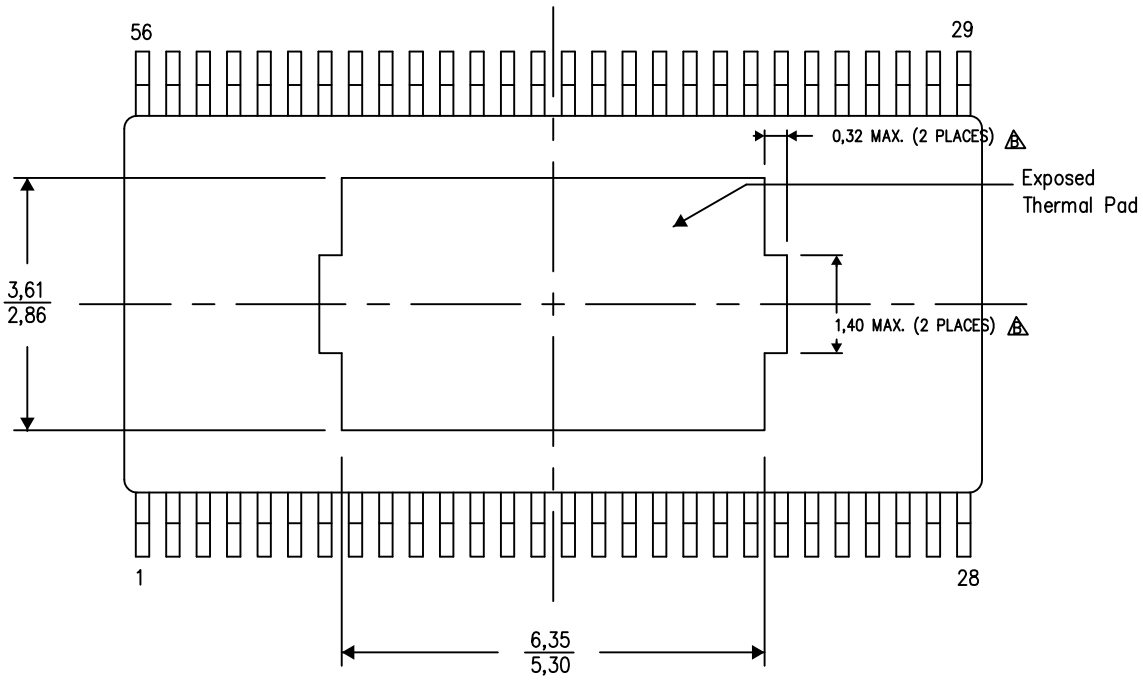
DFD (R–PDSO–G56) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

Exposed Thermal Pad Dimensions

4210501–4/G 07/12

NOTES: A. All linear dimensions are in millimeters

B Keep–out features are identified to prevent board routing interference.
These exposed metal features may vary within the identified area or completely absent on some devices.

PowerPAD is a trademark of Texas Instruments

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