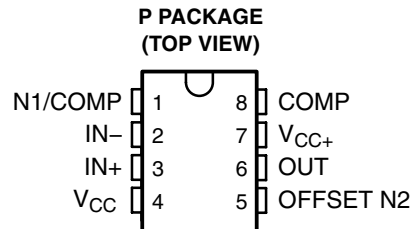


- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion . . . 0.003% Typ
- High Input Impedance . . . JFET Input Stage
- External Frequency Compensation
- Common-Mode Input Voltage Range Includes  $V_{CC+}$
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/ $\mu$ s Typ



## description

The TL080 JFET-input operational amplifier incorporates well-matched, high-voltage JFET and bipolar transistors in an integrated circuit. This device features high slew rates, low input bias and offset currents, and a low offset-voltage temperature coefficient. Offset adjustment and external-compensation options are available.

The TL080C is characterized for operation from 0°C to 70°C.

### AVAILABLE OPTIONS

T <sub>A</sub>	V <sub>IO</sub> max AT 25°C	PACKAGE
		PLASTIC DIP (P)
0°C to 70°C	10 mV	TL080CP



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

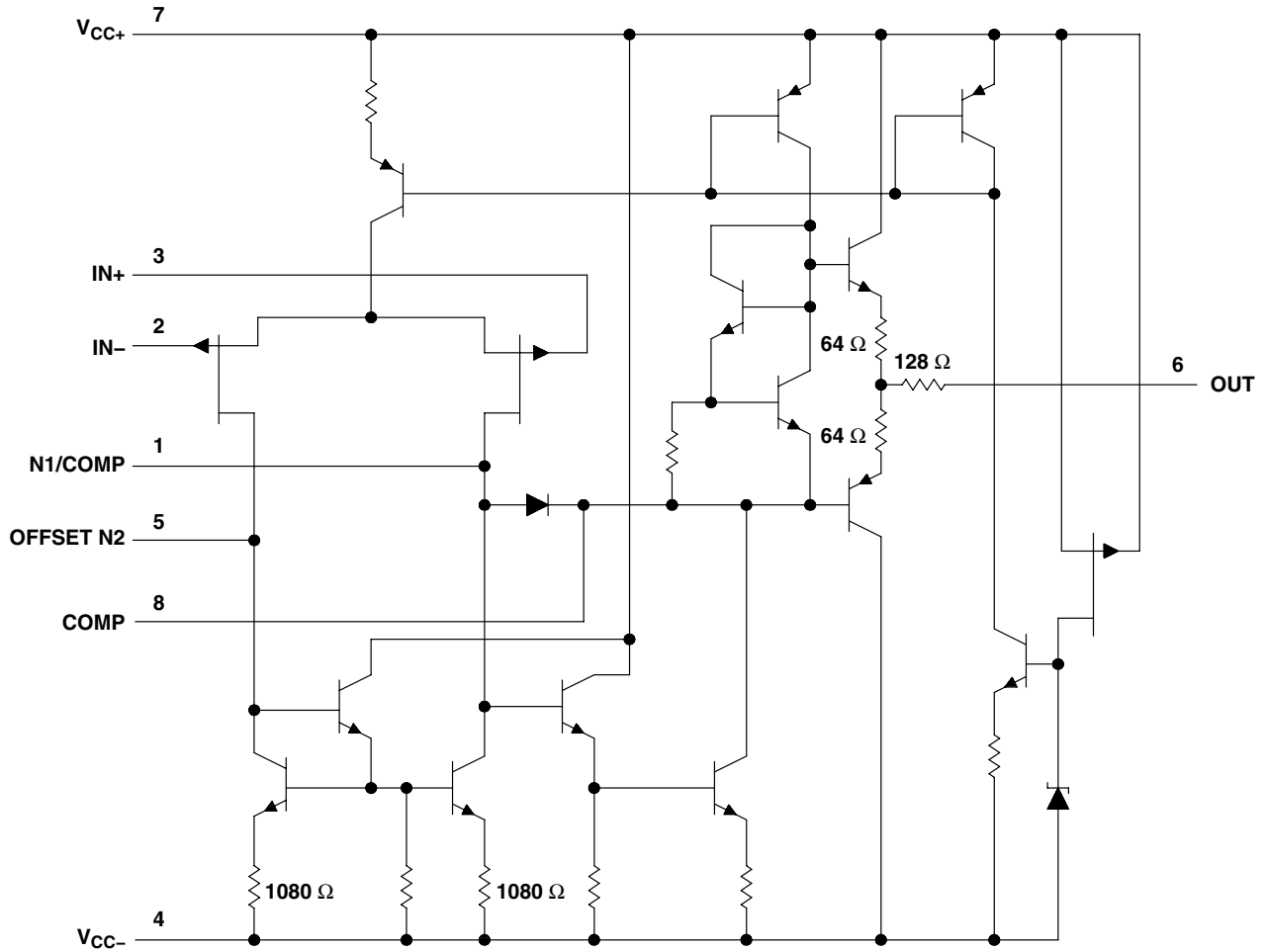
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# TL080 JFET-INPUT OPERATIONAL AMPLIFIER

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## schematic



All component values shown are nominal.



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage (see Note 1): $V_{CC+}$ .....	18 V
$V_{CC-}$ .....	–18 V
Differential input voltage, $V_{ID}$ (see Note 2) .....	±30 V
Input voltage, $V_I$ (see Notes 1 and 3) .....	±15 V
Duration of short-circuit current (see Note 4) .....	Unlimited
Package thermal impedance, $\theta_{JA}$ (see Notes 5 and 6) .....	85°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .....	260°C
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .
  2. Differential voltages are at  $IN+$  with respect to  $IN-$ .
  3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
  4. The output can be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
  5. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can impact reliability.
  6. The package thermal impedance is calculated in accordance with JESD 51-7.

**electrical characteristics,  $V_{CC\pm} = \pm 15$  V (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	$T_A$ †	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$V_O = 0, R_S = 50 \Omega$	25°C		3	15	mV
			Full range			20	
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage	$V_O = 0, R_S = 50 \Omega$	Full range		18		$\mu V/^\circ C$
$I_{IO}$	Input offset current‡	$V_O = 0$	25°C		5	200	pA
			Full range			2	nA
$I_{IB}$	Input bias current‡	$V_O = 0$	25°C		30	400	pA
			Full range			10	nA
$V_{ICR}$	Common-mode input voltage range		25°C	±11	–12 to 15		V
$V_{OM}$	Maximum peak output voltage swing	$R_L = 10 k\Omega$	25°C	±12	±13.5		V
		$R_L \geq 10 k\Omega$	Full range	±12			
		$R_L \geq 2 k\Omega$		±10		±12	
$A_{VD}$	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 2 k\Omega$	25°C		25	200	V/mV
			Full range		15		
$B_1$	Unity-gain bandwidth		25°C		3		MHz
$r_i$	Input resistance		25°C		$10^{12}$		$\Omega$
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, V_O = 0, R_S = 50 \Omega$	25°C		70	86	dB
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC} = \pm 15$ V to $\pm 9$ V, $V_O = 0, R_S = 50 \Omega$	25°C		70	86	dB
$I_{CC}$	Supply current	$V_O = 0,$ No load	25°C		1.4	2.8	mA
$V_{O1}/V_{O2}$	Crosstalk attenuation	$A_{VD} = 100$	25°C		120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for  $T_A$  is –40°C to 85°C.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 5. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.



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operating characteristics,  $V_{CC\pm} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
SR Slew rate at unity gain	$V_I = 10\text{ V}$ ,	$R_L = 2\text{ k}\Omega$ ,	$C_L = 100\text{ pF}$ , See Figure 1	8	13		$\text{V}/\mu\text{s}$
$t_r$ Rise-time overshoot factor	$V_I = 20\text{ mV}$ ,	$R_L = 2\text{ k}\Omega$ ,	$C_L = 100\text{ pF}$ , See Figure 1		0.05 20%		$\mu\text{s}$
$V_n$ Equivalent input noise voltage	$R_S = 100\ \Omega$	$f = 1\text{ kHz}$			18		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ Hz to } 10\text{ kHz}$			4		$\mu\text{V}$
$I_n$ Equivalent input noise current	$R_S = 100\ \Omega$ ,	$f = 1\text{ kHz}$			0.01		$\text{pA}/\sqrt{\text{Hz}}$
THD Total harmonic distortion	$V_{O(\text{rms})} = 10\text{ V}$ ,	$R_S \leq 1\text{ k}\Omega$ ,	$R_L \geq 2\text{ k}\Omega$ , $f = 1\text{ kHz}$		0.003%		

## APPLICATION INFORMATION

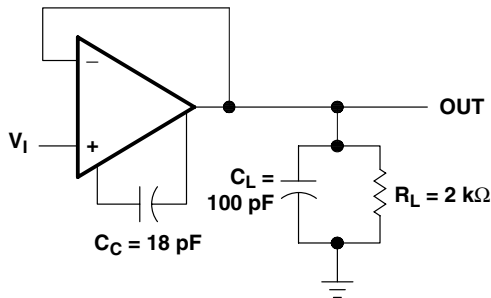


Figure 1. Unity-Gain Amplifier

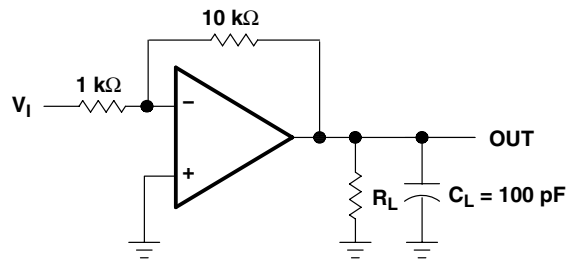


Figure 2. Gain-of-10 Inverting Amplifier

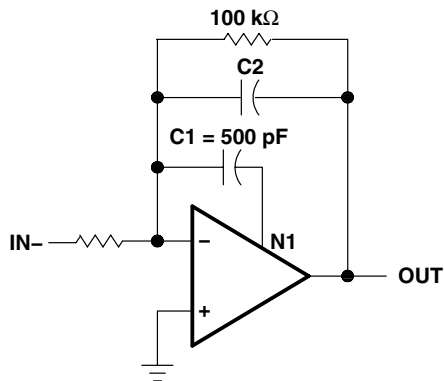


Figure 3. Feed-Forward Compensation

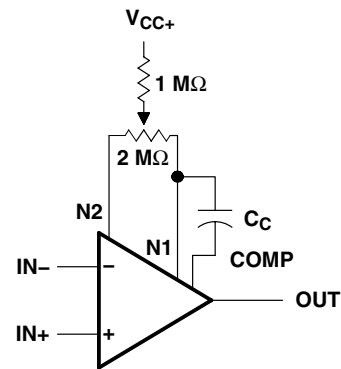


Figure 4. Input Offset Voltage Null Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE	
$V_{OM}$	Maximum peak output voltage	vs Frequency	5, 6, 7
		vs Free-air temperature	8
		vs Load resistance	9
		vs Supply voltage	10
$A_{VD}$	Large-signal differential voltage amplification	vs Free-air temperature	11
		vs Frequency	12
	Differential voltage amplification	vs Frequency	13
$P_D$	Total power dissipation	vs Free-air temperature	14
$I_{CC}$	Supply current	vs Free-air temperature	14
		vs Supply voltage	15
$I_{IB}$	Input bias current	vs Free-air temperature	16
	Large-signal pulse response	vs Time	17
$V_O$	Output voltage	vs Elapsed time	18
CMRR	Common-mode rejection ratio	vs Free-air temperature	19
$V_n$	Equivalent input noise voltage	vs Frequency	20
THD	Total harmonic distortion	vs Frequency	21

MAXIMUM PEAK OUTPUT VOLTAGE  
vs  
FREQUENCY

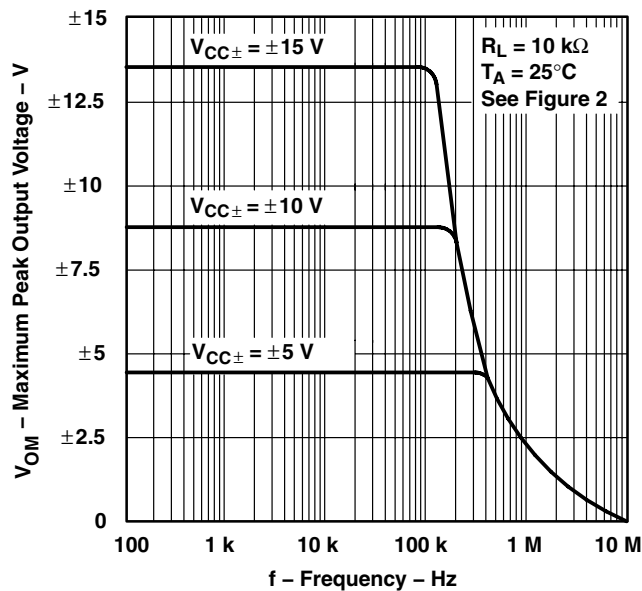


Figure 5

MAXIMUM PEAK OUTPUT VOLTAGE  
vs  
FREQUENCY

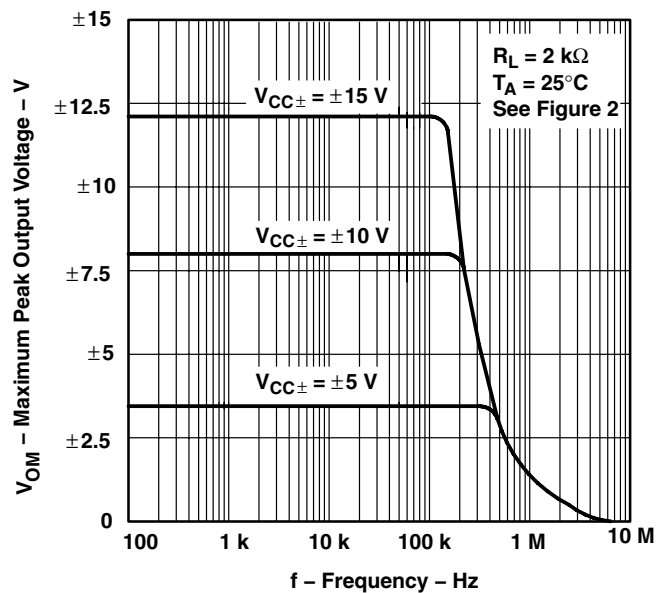


Figure 6

# TL080 JFET-INPUT OPERATIONAL AMPLIFIER

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## TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE  
vs  
FREQUENCY

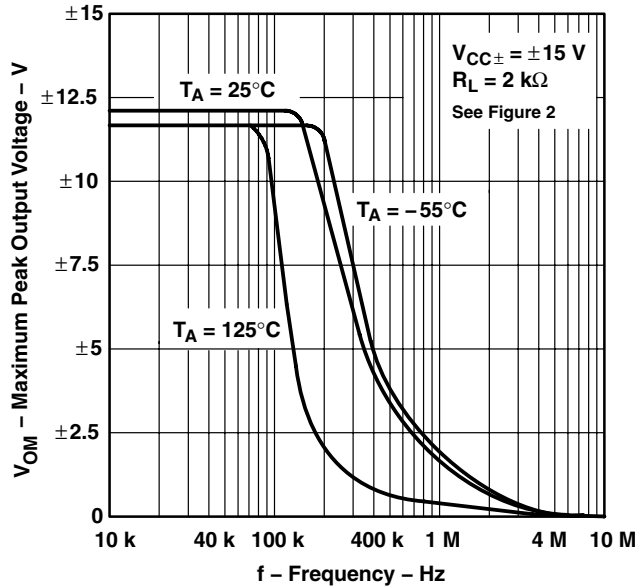


Figure 7

MAXIMUM PEAK OUTPUT VOLTAGE  
vs  
FREE-AIR TEMPERATURE

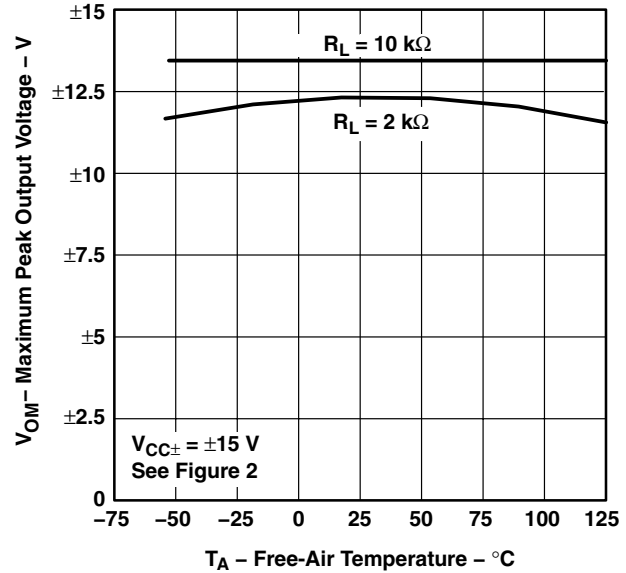


Figure 8

MAXIMUM PEAK OUTPUT VOLTAGE  
vs  
LOAD RESISTANCE

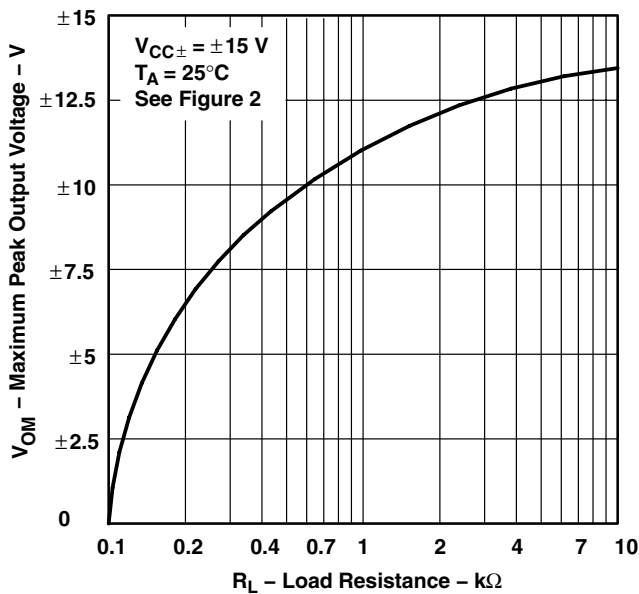


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE  
vs  
SUPPLY VOLTAGE

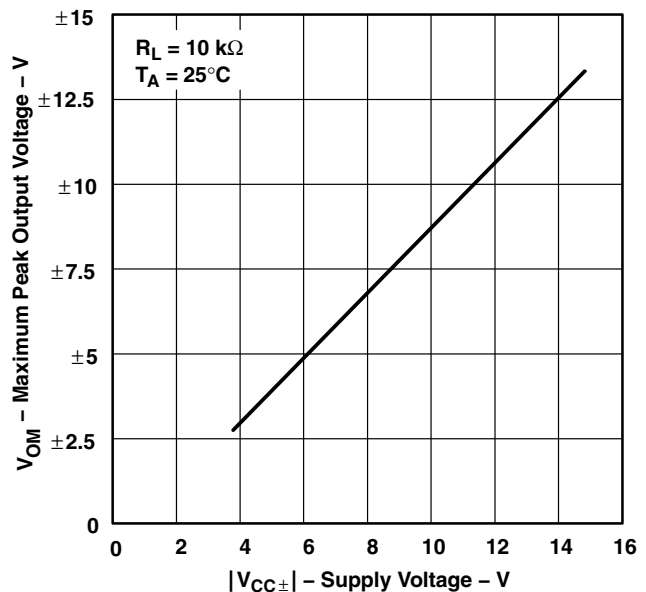
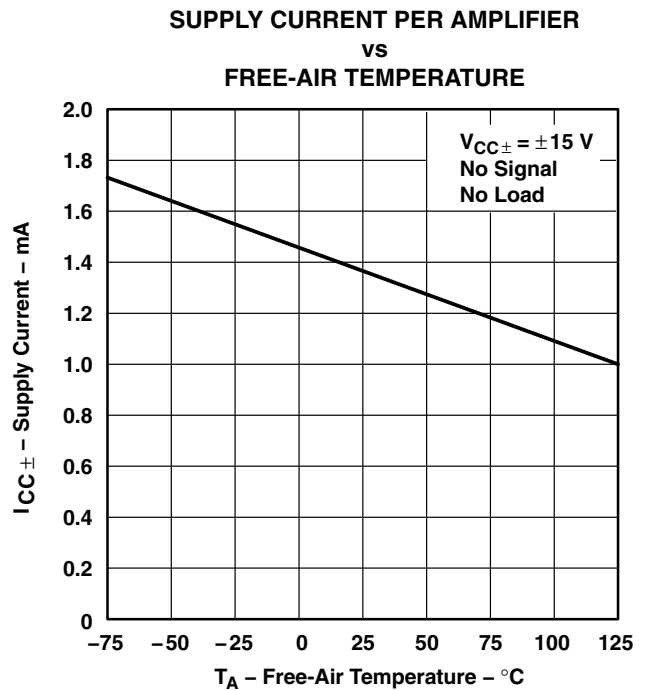
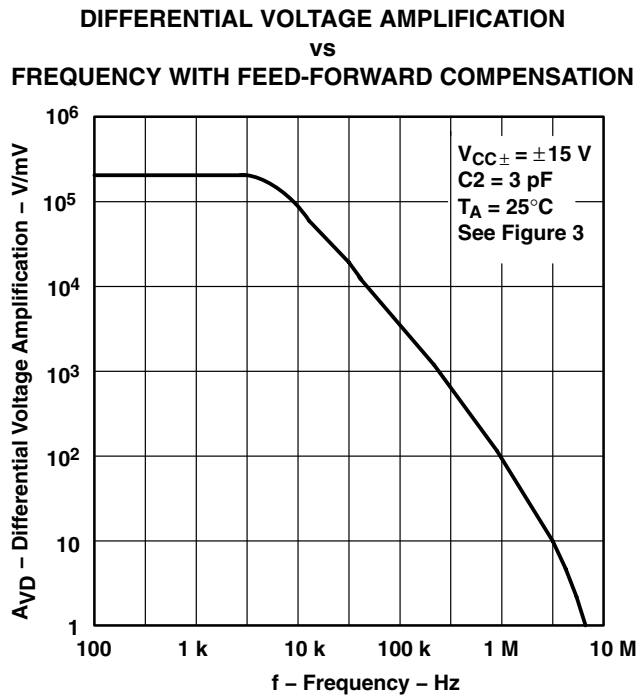
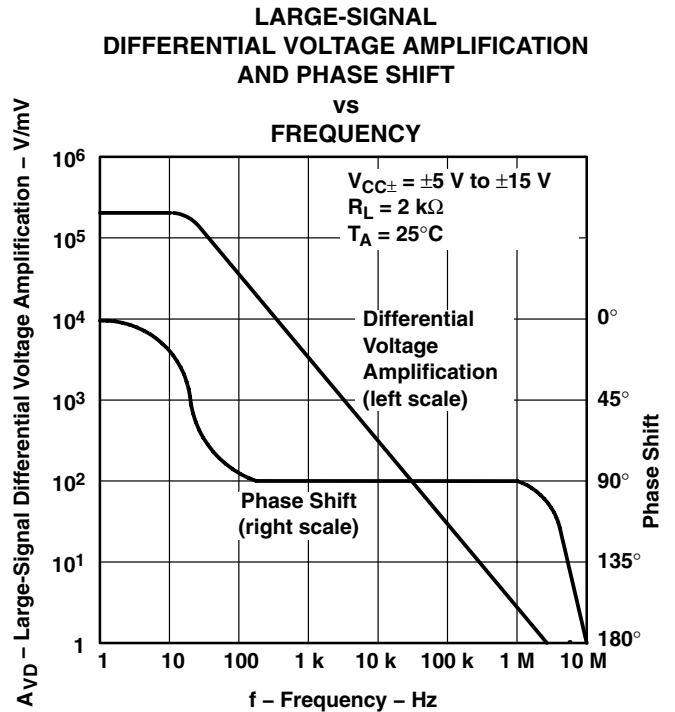
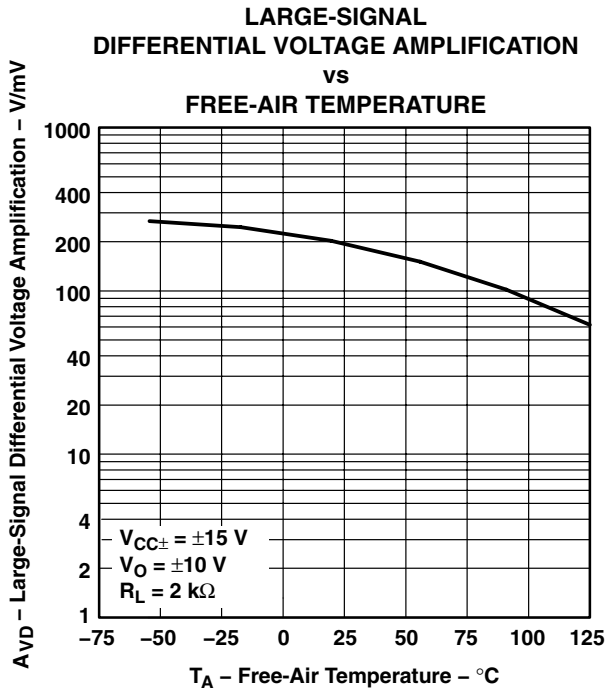


Figure 10



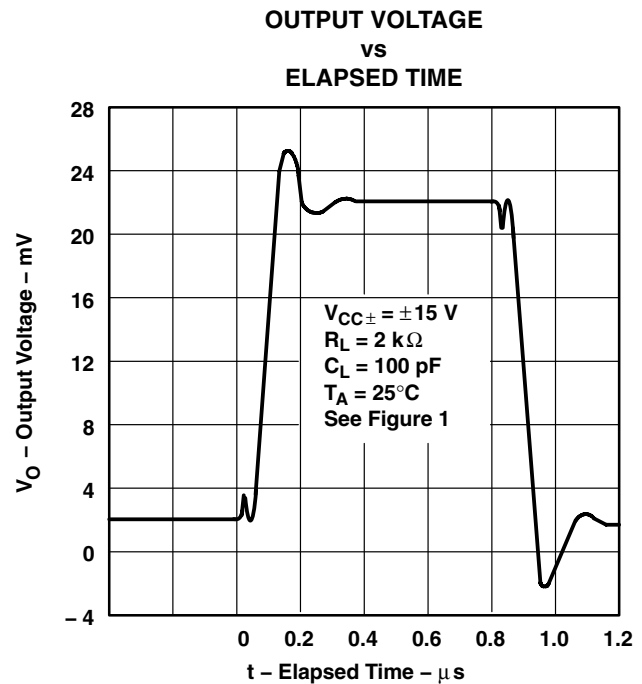
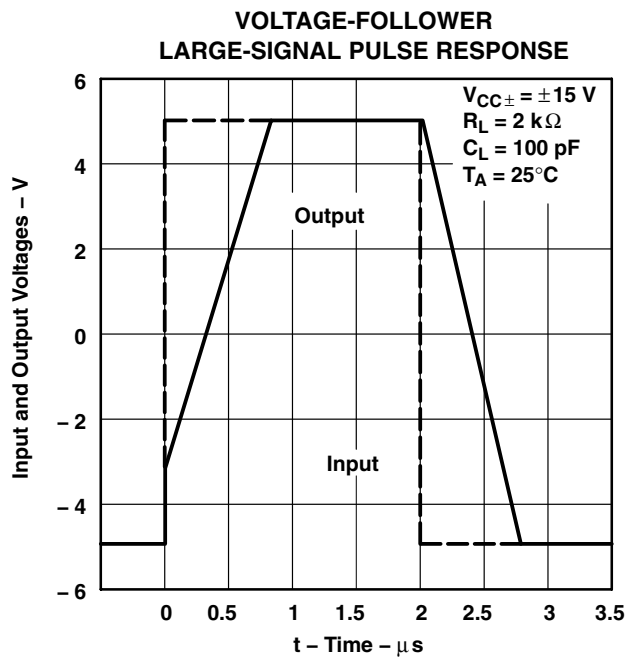
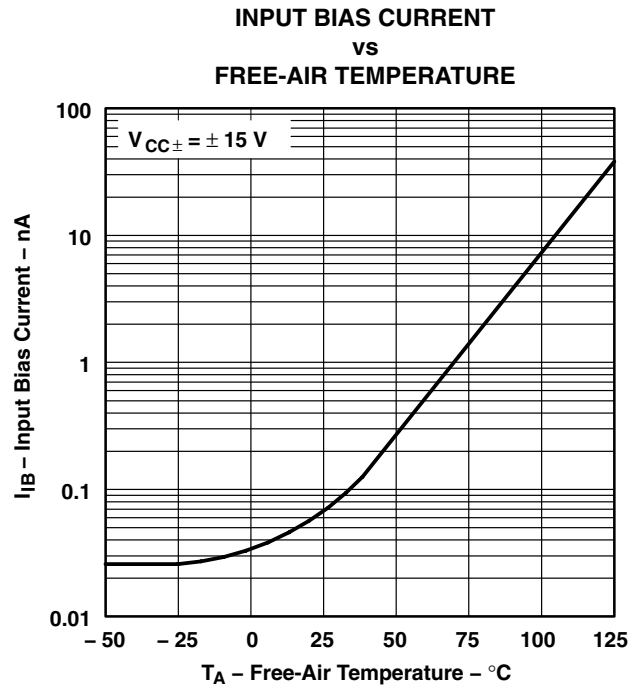
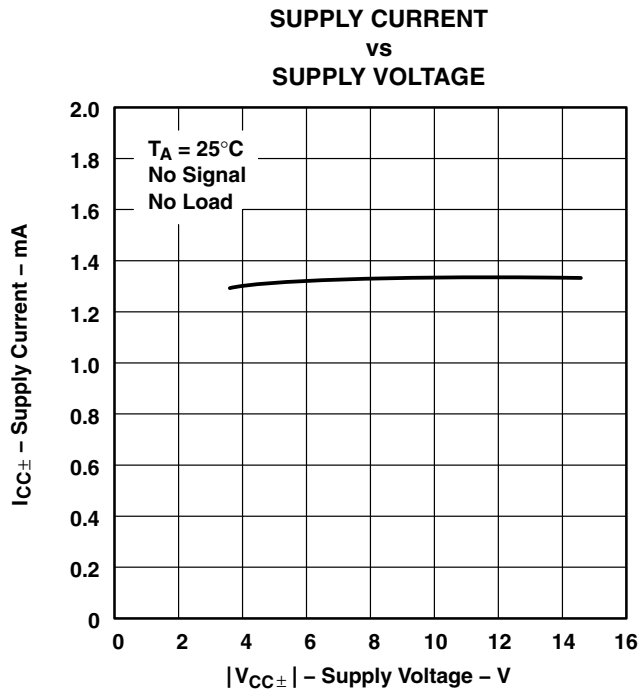
TYPICAL CHARACTERISTICS



# TL080 JFET-INPUT OPERATIONAL AMPLIFIER

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## TYPICAL CHARACTERISTICS





TYPICAL CHARACTERISTICS

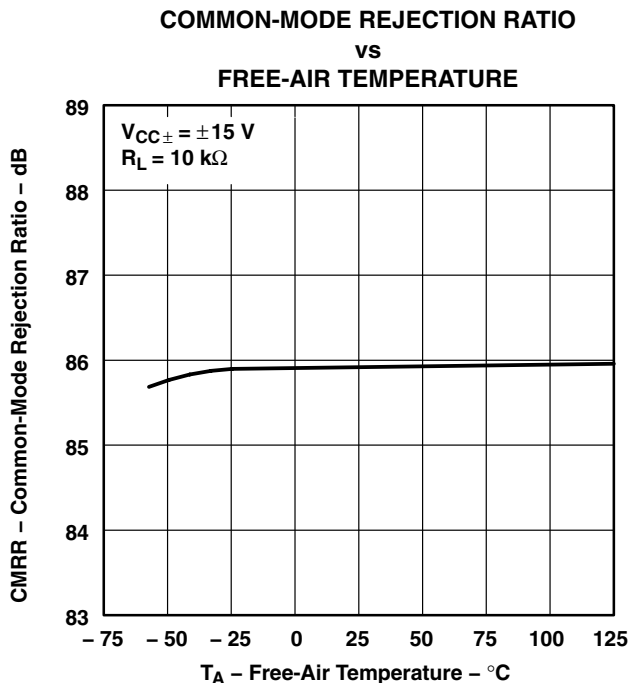


Figure 19

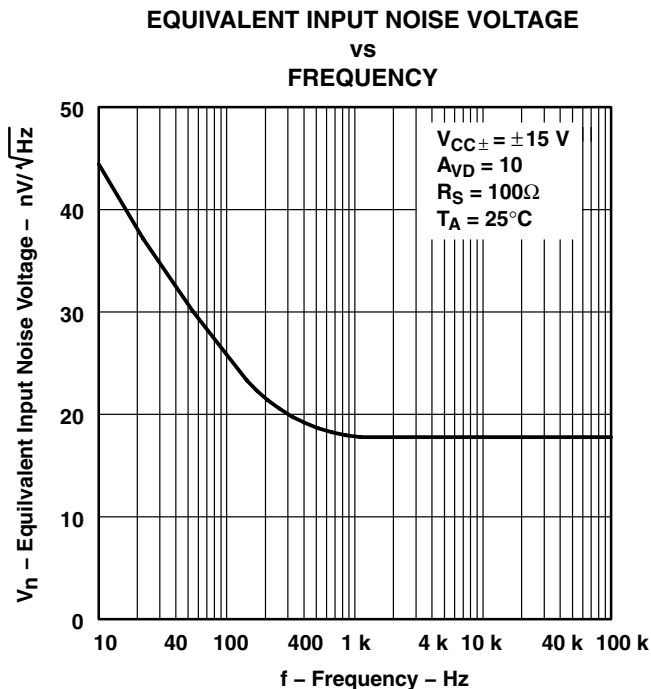


Figure 20

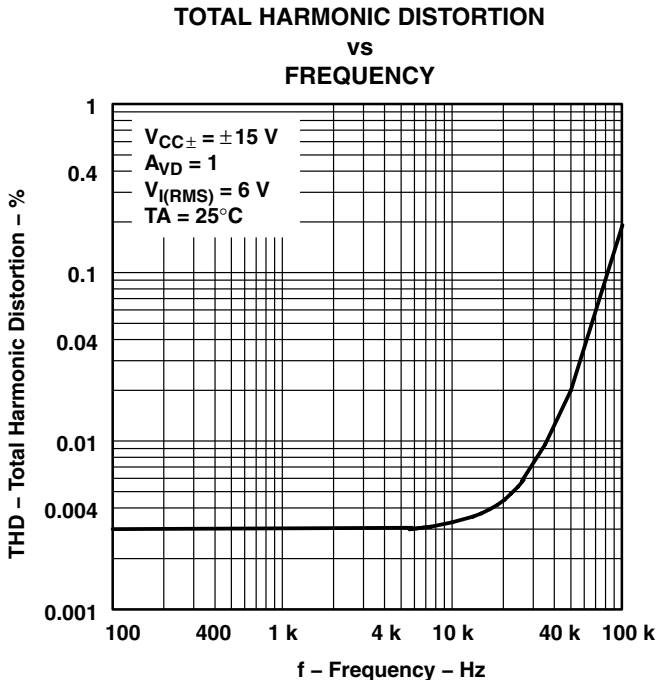


Figure 21

# TL080 JFET-INPUT OPERATIONAL AMPLIFIER

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## APPLICATION INFORMATION

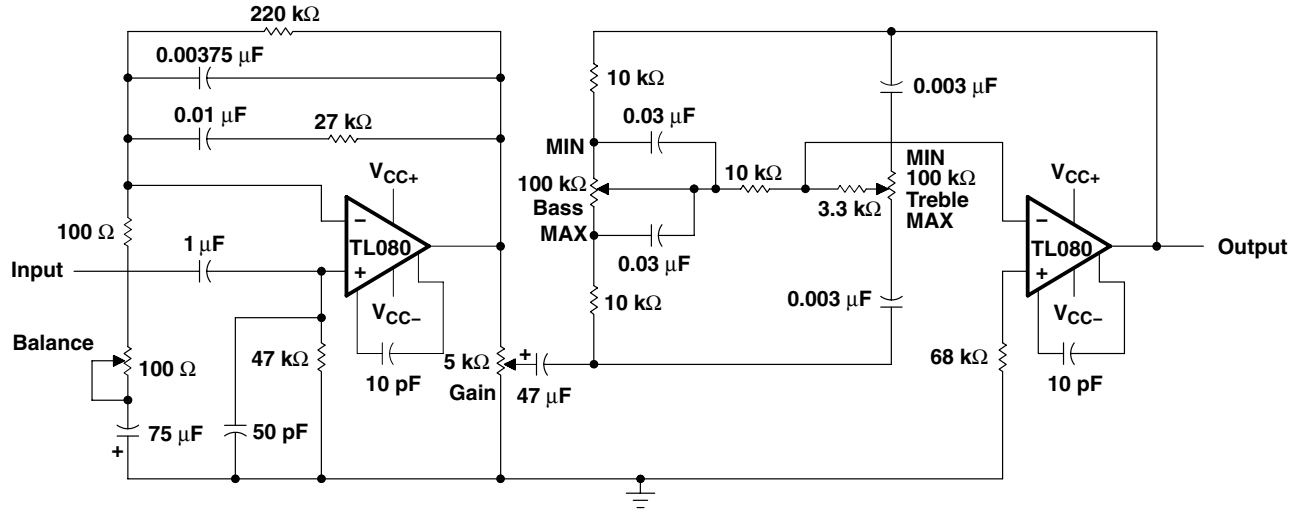


Figure 22. IC Preamplifier

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TL080CP	NRND	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL080CPE4	NRND	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL080IP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

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DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>	Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
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Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Energy	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
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RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>	Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless-apps">www.ti.com/wireless-apps</a>