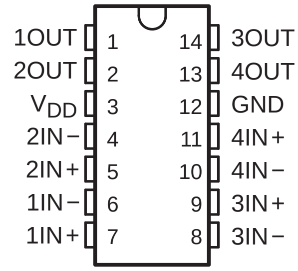
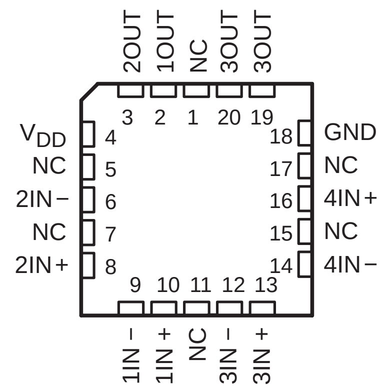
- **Very Low Power . . . 200 μW Typ at 5 V**
- **Fast Response Time . . . 2.5 μs Typ With 5-mV Overdrive**
- **Single Supply Operation:**
  - **TLC139M . . . 4 V to 16 V**
  - **TLC339M . . . 4 V to 16 V**
  - **TLC339C . . . 3 V to 16 V**
  - **TLC339I . . . 3 V to 16 V**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Input Offset Voltage Change at Worst Case Input at Condition Typically 0.23 μV/Month Including the First 30 Days**
- **On-Chip ESD Protection**

D, J, N, OR PW PACKAGE (TOP VIEW)



FK PACKAGE (TOP VIEW)



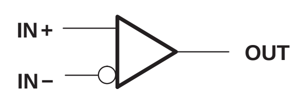
NC − No internal connection

description

The TLC139/TLC339 consists of four independent differential-voltage comparators designed to operate from a single supply. It is functionally similar to the LM139/LM339 family but uses 1/20th the power for similar response times. The open-drain MOS output stage interfaces to a variety of leads and supplies, as well as wired logic functions. For a similar device with a push-pull output configuration, see the TLC3704 data sheet.

The Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS™ process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

symbol (each comparator)



AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE				
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (P)	TSSOP (PW)
0°C to 70°C	5 mV	TLC339CD	—	—	TLC339CN	TLC339CPW
−40°C to 85°C	5 mV	TLC339ID	—	—	TLC339IN	TLC339IPW
−40°C to 125°C	5 mV	TLC339QD	—	—	TLC339QN	—
−55°C to 125°C	5 mV	TLC339MD	TLC139MFK	TLC139MJ	TLC339MN	—

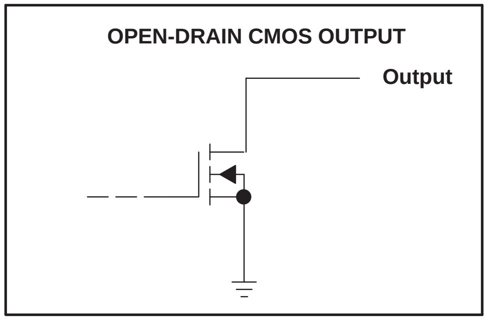
The D and PW packages are available taped and reeled. Add the suffix R to the device type (e.g., TLC339CDR or TLC339CPWR).

LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

The TLC139M and TLC339M are characterized for operation over the full military temperature range of −55°C to 125°C. The TLC339C is characterized for operation over the commercial temperature range of 0°C to 70°C. The TLC339I is characterized for operation over the industrial temperature range of −40°C to 85°C. The TLC339Q is characterized for operation over the extended industrial temperature range of −40°C to 125°C.

output schematic



OPEN-DRAIN CMOS OUTPUT

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) . . . . . −0.3 V to 18 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±18 V
Input voltage range, V_I . . . . . −0.3 V to V_{DD}
Output voltage range, V_O . . . . . −0.3 V to V_{DD}
Input current, I_I . . . . . ±5 mA
Output current, I_O (each output) . . . . . 20 mA
Total supply current into V_{DD} . . . . . 40 mA
Total current out of GND . . . . . 60 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: TLC139M . . . . . −55°C to 125°C
TLC339C . . . . . 0°C to 70°C
TLC339I . . . . . −40°C to 85°C
TLC339M . . . . . −55°C to 125°C
TLC339Q . . . . . −40°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN −.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW
PW	700 mW	5.6 mW/°C	448 mW	364 mW	140 mW

recommended operating conditions

	TLC139M, TLC339M MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	0		$V_{DD}-1.5$	V
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	−55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A	TLC139M, TLC339M MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, See Note 3	V_{DD} = 5 V to 10 V,	25°C		1.4	5	mV
				−55°C to 125°C			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V		25°C		1		pA
				125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V		25°C		5		pA
				125°C			30	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1$			V
				−55°C to 125°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min		25°C		84		dB
				125°C		84		
				−55°C		84		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V		25°C		85		dB
				125°C		84		
				−55°C		84		
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 6 mA	25°C		300	400	mV
				125°C			800	
I_{OH}	High-level output current	V_{ID} = −1 V,	V_O = 5 V	25°C		0.8	40	nA
				125°C			1	µA
I_{DD}	Supply current (four comparators)	Outputs low,	No load	25°C		44	80	µA
				−55°C to 125°C			175	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to V_{DD}.

recommended operating conditions

	TLC339C			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	−0.2		$V_{DD}-1.5$	V
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A	TLC339C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, See Note 3	V_{DD} = 5 V to 10 V,	25°C		1.4	5	mV
				0°C to 70°C			6.5	
I_{IO}	Input offset current	V_{IC} = 2.5 V		25°C		1		pA
				70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V		25°C		5		pA
				70°C			0.6	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1$			V
				0°C to 70°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min		25°C		84		dB
				70°C		84		
				0°C		84		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V		25°C		85		dB
				70°C		85		
				0°C		85		
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 6 mA	25°C		300	400	mV
				70°C			650	
I_{OH}	High-level output current	V_{ID} = −1 V,	V_O = 5 V	25°C		0.8	40	nA
				70°C			1	µA
I_{DD}	Supply current (four comparators)	Outputs low,	No load	25°C		44	80	µA
				0°C to 70°C			100	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to V_{DD}.

recommended operating conditions

	TLC339I			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	−0.2		$V_{DD}-1.5$	V
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	TLC339I			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 3	25°C		1.4	5	mV
			−40°C to 85°C			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			85°C			2	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to $V_{DD}-1$			V
			−40°C to 85°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			85°C		84		
			−40°C		84		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			85°C		85		
			−40°C		84		
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 6 mA	25°C		300	400	mV
			85°C			700	
I_{OH}	High-level output current	V_{ID} = −1 V, V_O = 5 V	25°C		0.8	40	nA
			85°C			1	µA
I_{DD}	Supply current (four comparators)	Outputs low, No load	25°C		44	80	µA
			−40°C to 85°C			125	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to V_{DD}.

recommended operating conditions

	TLC339Q			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	0		$V_{DD} - 1.5$	V
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	− 40		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	TLC339Q			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 3	25°C		1.4	5	mV
			−40°C to 125°C			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to $V_{DD} - 1$			V
			−40°C to 125°C	0 to $V_{DD} - 1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			125°C		84		
			−40°C		84		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		84		
			−40°C		84		
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 6 mA	25°C		300	400	mV
			125°C			800	
I_{OH}	High-level output current	V_{ID} = −1 V, V_O = 5 V	25°C		0.8	40	nA
			125°C			1	µA
I_{DD}	Supply current (four comparators)	Outputs low, No load	25°C		44	80	µA
			−40°C to 125°C			125	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to V_{DD}.

switching characteristics, V_{DD} = 5 V, T_A = 25°C (see Figure 3)

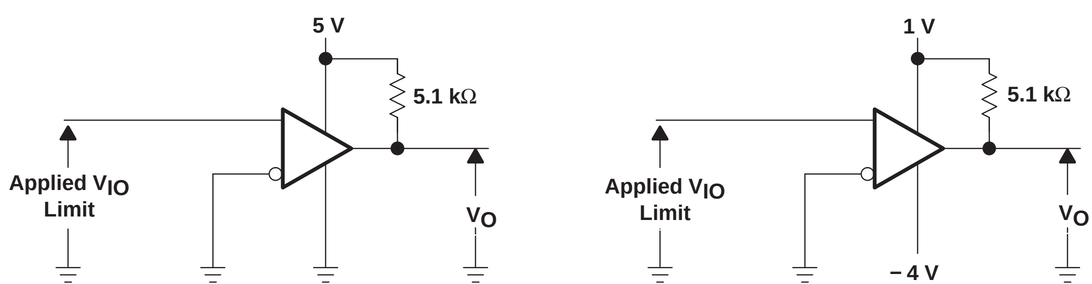
PARAMETER		TEST CONDITIONS		TLC139M, TLC339C TLC339I, TLC339M TLC339Q			UNIT
				MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high output	f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		4.5		µs
			Overdrive = 5 mV		2.5		
			Overdrive = 10 mV		1.7		
			Overdrive = 20 mV		1.2		
			Overdrive = 40 mV		1.0		
		V_I = 1.4 V step at IN+			1.1		
t_{PHL}	Propagation delay time, high-to-low level output	f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		3.6		µs
			Overdrive = 5 mV		2.1		
			Overdrive = 10 mV		1.3		
			Overdrive = 20 mV		0.85		
			Overdrive = 40 mV		0.55		
		V_I = 1.4 V step at IN+			0.10		
t_{THL}	Transition time, high-to-low level output	f = 10 kHz, C_L = 15pF	Overdrive = 50 mV		20		ns

PARAMETER MEASUREMENT INFORMATION

The TLC139 and TLC339 contain a digital output stage that, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for testing parameters such as input offset voltage, common-mode rejection, etc., are suggested.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.



(a) V_{IO} WITH V_{IC} = 0 V (b) V_{IO} WITH V_{IC} = 4 V

Figure 1. Method for Verifying That Input Offset Voltage Is Within Specified Limits

PARAMETER MEASUREMENT INFORMATION

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output changes state.

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching mode servo loop in which U1A generates a triangular waveform of approximately 20-mV amplitude. U1B acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1C through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

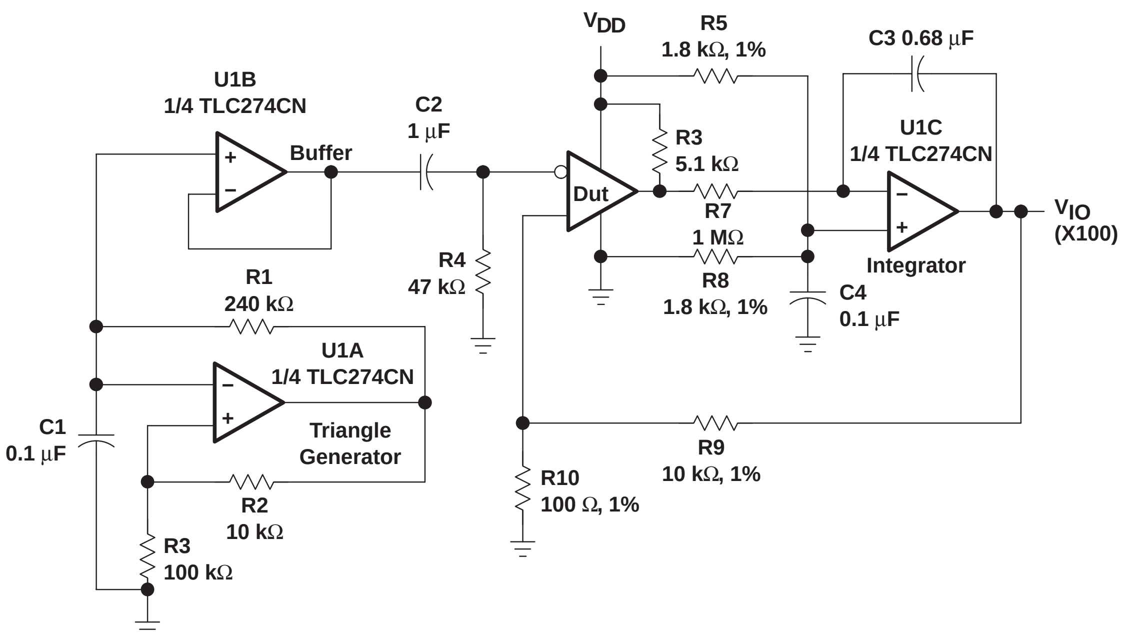
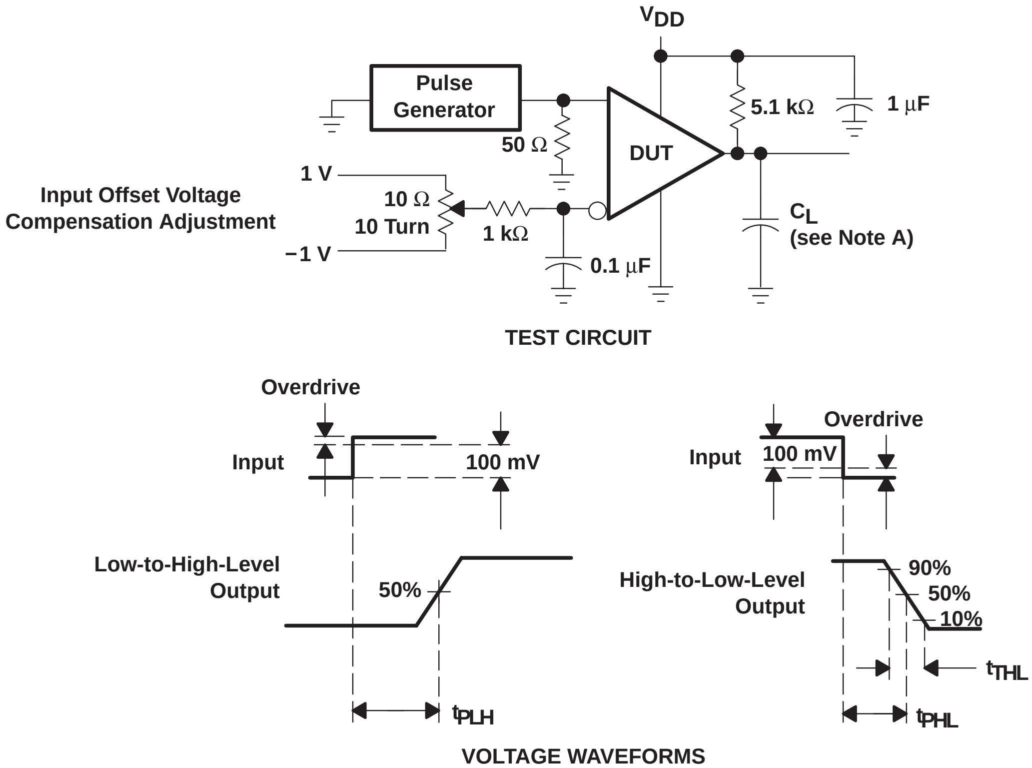


Figure 2. Circuit for Input Offset Voltage Measurement

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained, with a device in the socket to obtain the actual input current of the device.

PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Propagation delay time, low-to-high-level output, is measured from the leading edge of the input pulse, while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation delay time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input as shown in Figure 3, so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, causes the output to change state.



NOTE A: C_L includes probe and jig capacitance.

Figure 3. Propagation Delay, Rise, and Fall Times Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	4
I_{IB}	Input bias current	vs Free-air temperature	5
CMRR	Common-mode rejection ratio	vs Free-air temperature	6
k_{SVR}	Supply-voltage rejection ratio	vs Free-air temperature	7
I_{OH}	High-level output current	vs High-level output voltage vs Free-air temperature	8 9
V_{OL}	Low-level output voltage	vs Low-level output current vs Free-air temperature	10 11
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	12 13
t_{PLH}	Low-to-high level output propagation delay time	vs Supply voltage	14
t_{PHL}	Low-to-high level output propagation delay time	vs Supply voltage	15
	Overdrive voltage	vs Low-to-high-level output propagation delay time	16
t_f	Output fall time	vs Supply voltage	17
	Overdrive voltage	vs High-to-low-level output propagation delay time	18

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF INPUT OFFSET VOLTAGE

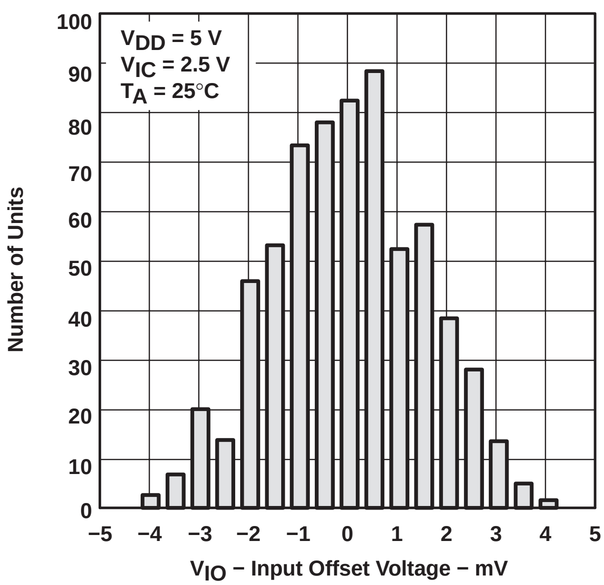


Figure 4

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

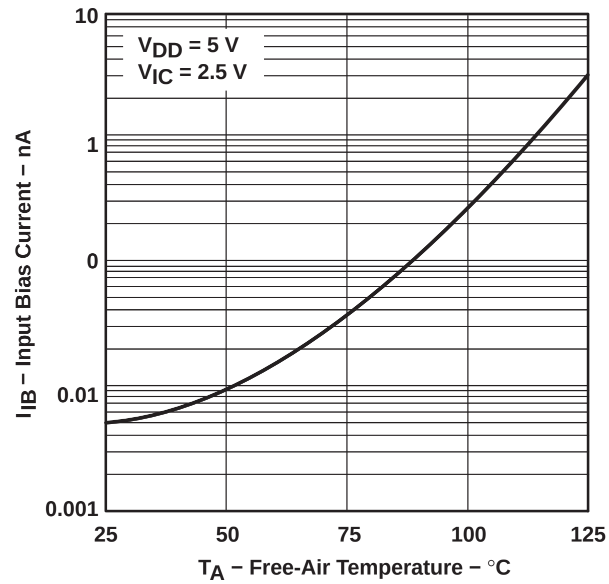


Figure 5

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

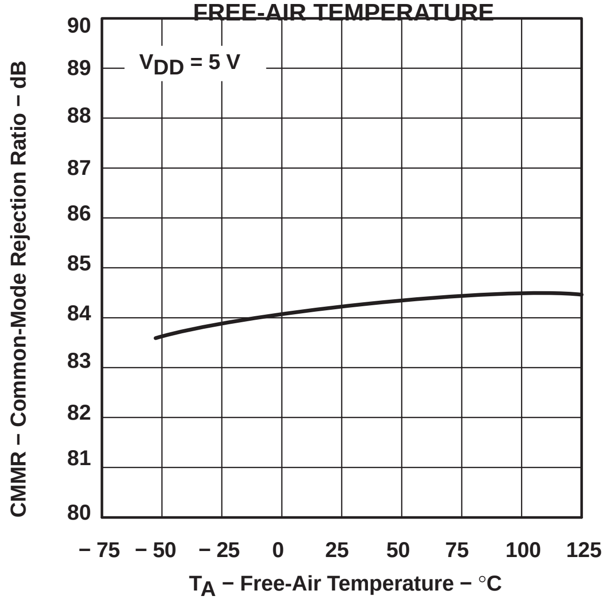


Figure 6

SUPPLY-VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

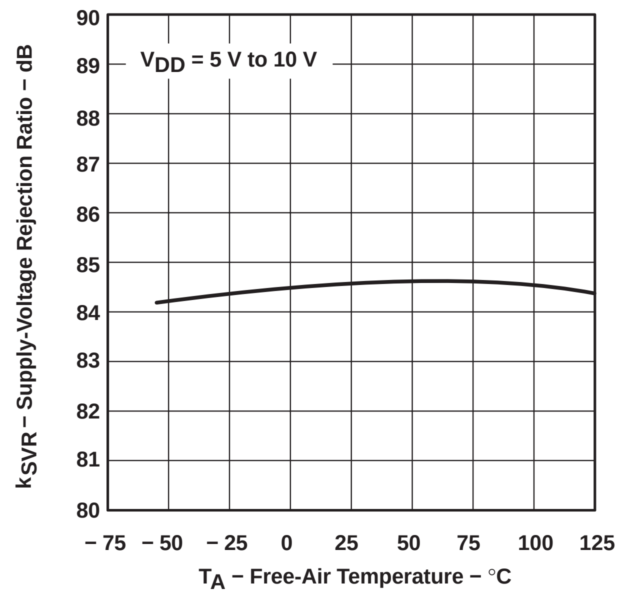


Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

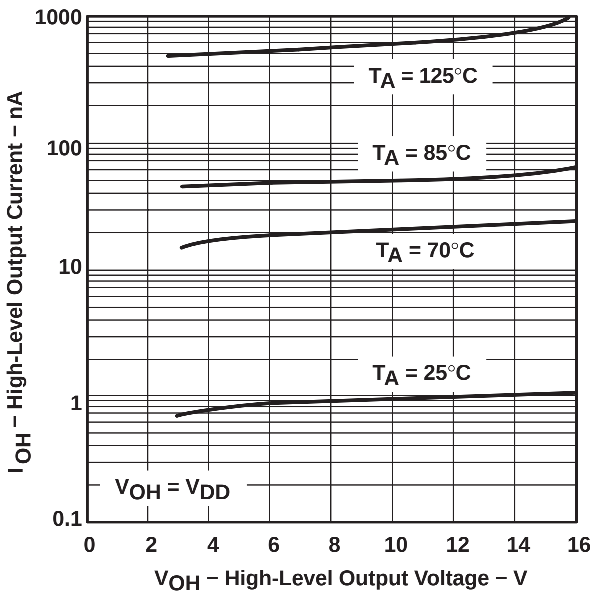


Figure 8

HIGH-LEVEL OUTPUT CURRENT vs FREE-AIR TEMPERATURE

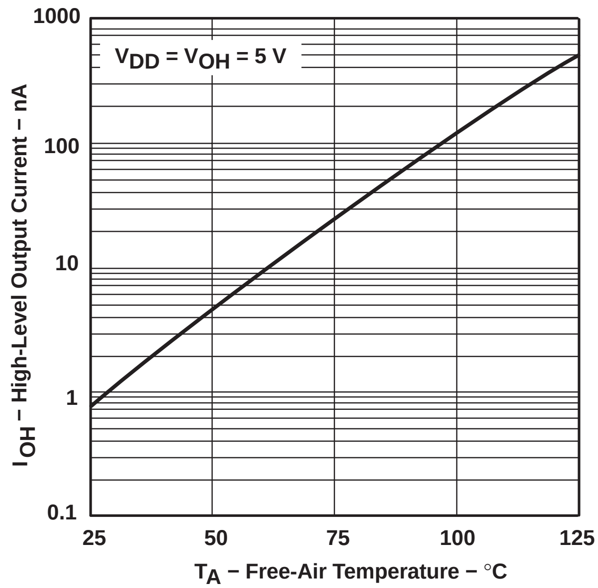


Figure 9

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

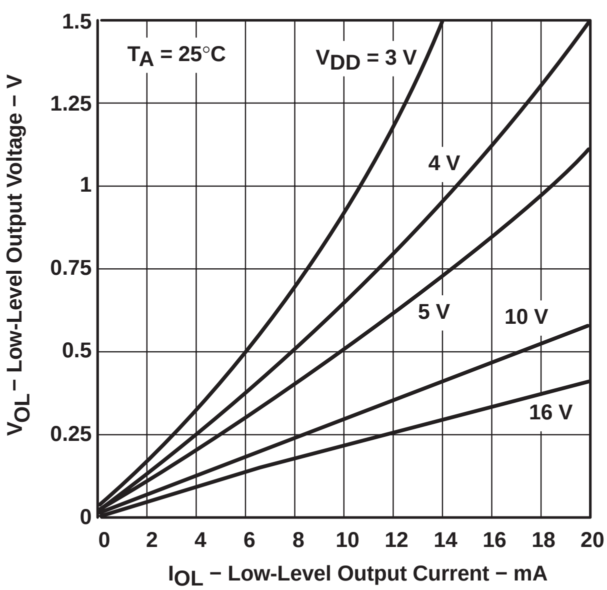


Figure 10

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

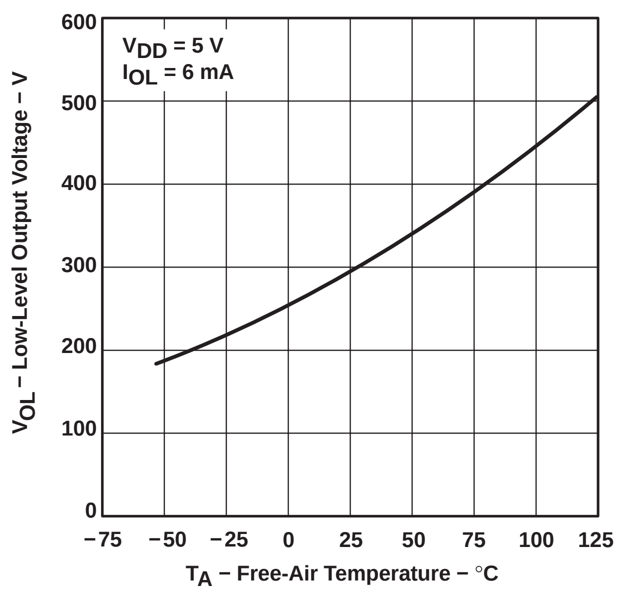


Figure 11

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

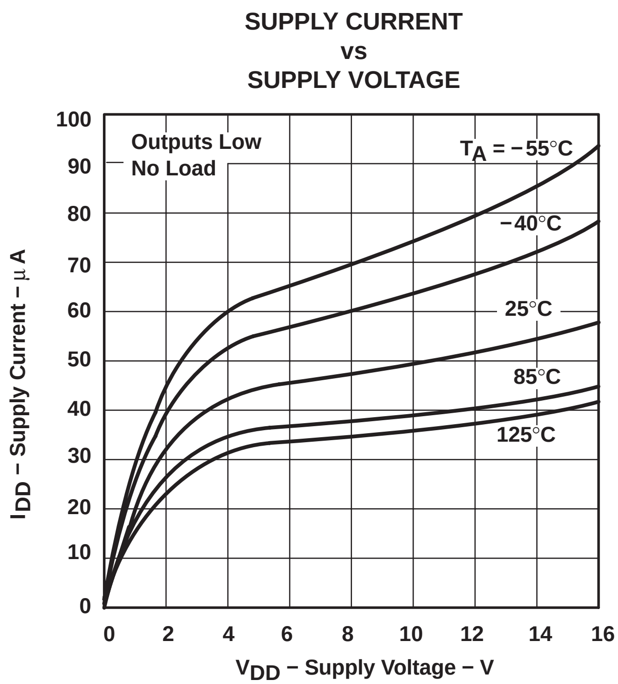


Figure 12

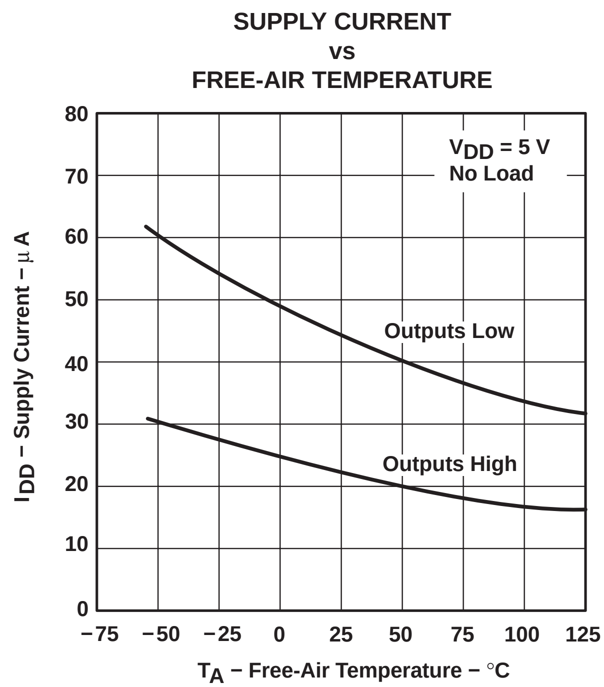


Figure 13

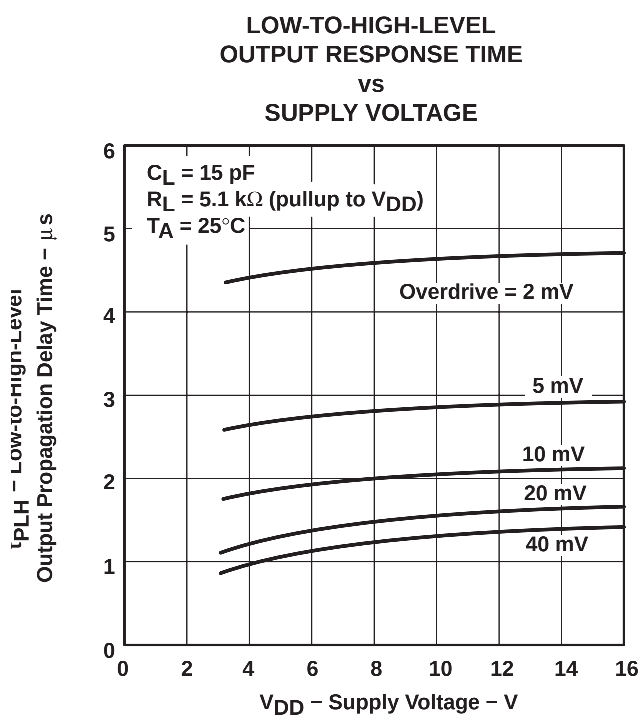


Figure 14

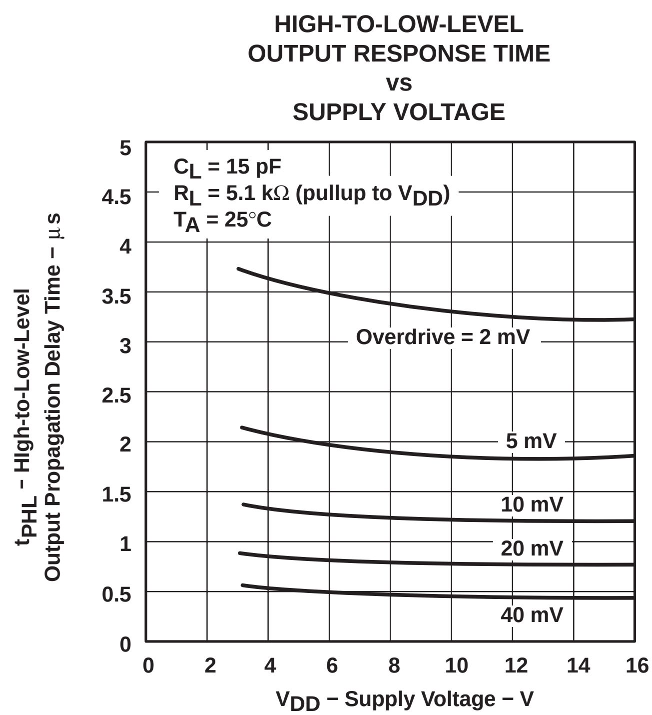


Figure 15

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LOW-TO-HIGH-LEVEL OUTPUT PROPAGATION DELAY FOR VARIOUS OVERDRIVE VOLTAGES

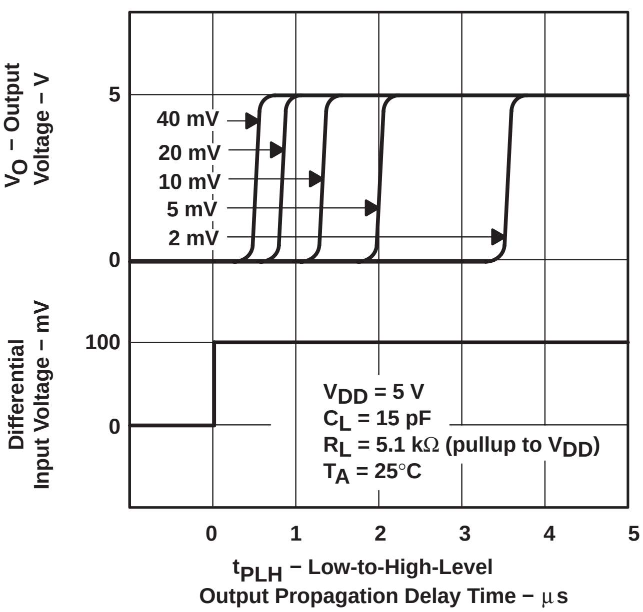


Figure 16

OUTPUT FALL TIME vs SUPPLY VOLTAGE

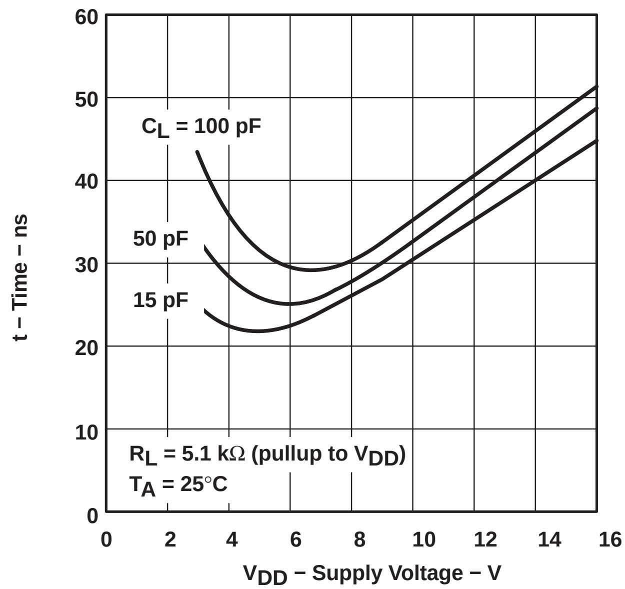


Figure 17

HIGH-TO-LOW-LEVEL OUTPUT PROPAGATION DELAY FOR VARIOUS OVERDRIVE VOLTAGES

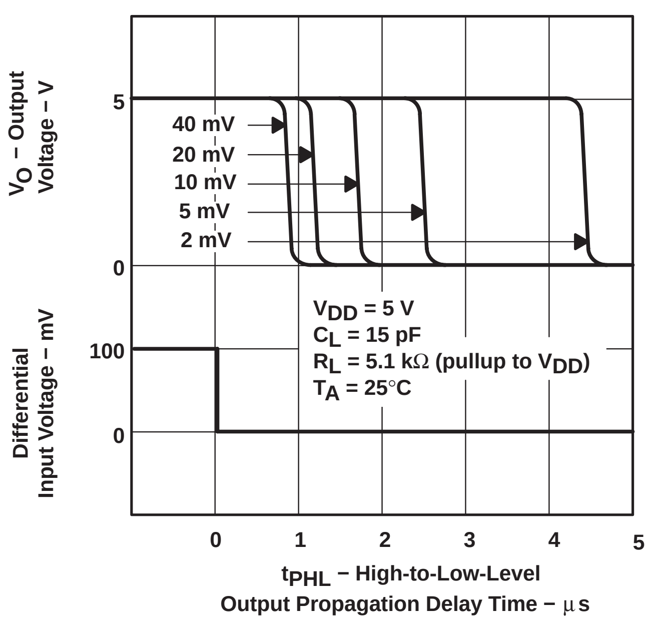


Figure 18

APPLICATION INFORMATION

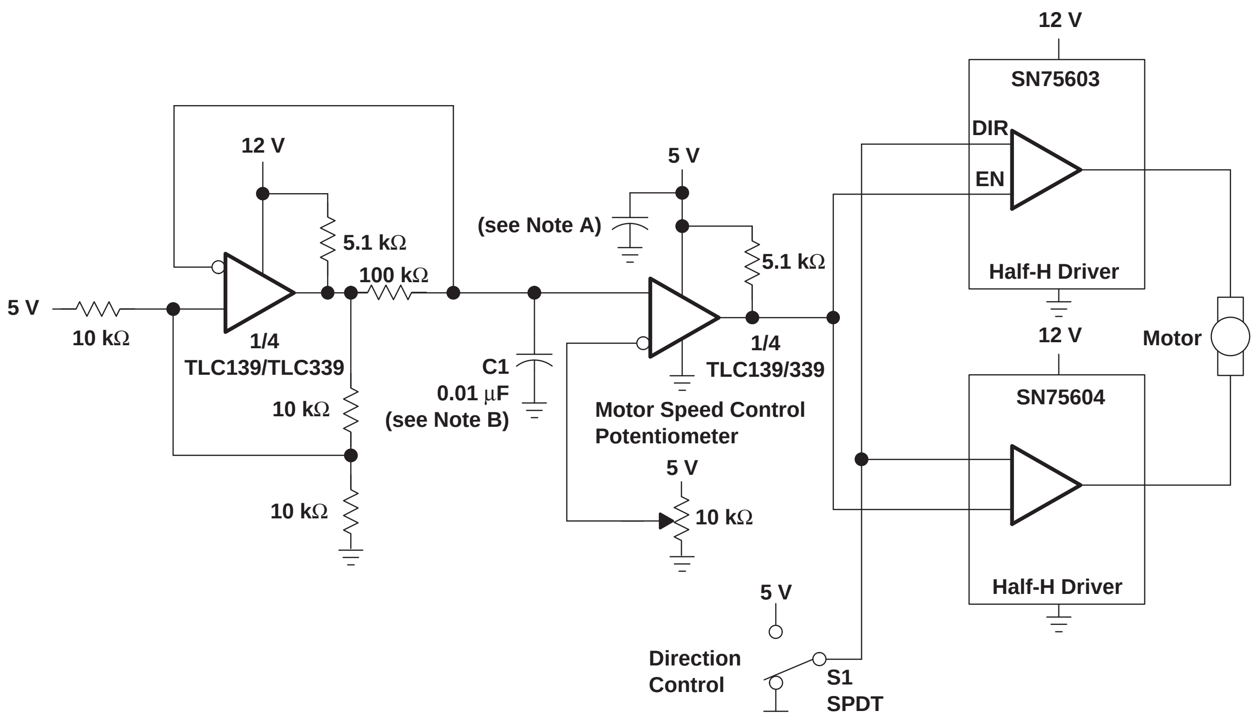
The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device is not damaged as long as the input current is limited to less than 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with V_{DD} = 5 V, both inputs must remain between −0.2 V and 4 V to assure proper device operation. To assure reliable operation, the supply should be decoupled with a capacitor (0.1 µF) positioned as close to the device as possible.

The output and supply currents require close observation since the TLC139/TLC339 does not provide current protection. For example, each output can source or sink a maximum of 20 mA; however, the total current to ground has an absolute maximum of 60 mA. This prohibits sinking 20 mA from each of the four outputs simultaneously since the total current to ground would be 80 mA.

The TLC139 and TLC339 have internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, exercise care when handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

Table of Applications

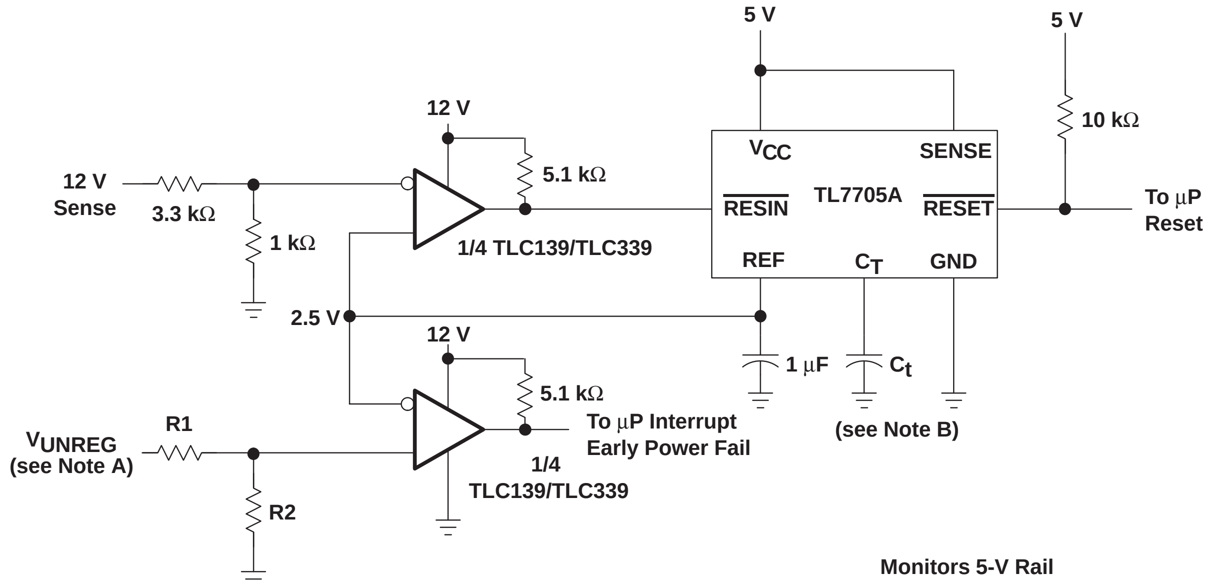
	FIGURE
Pulse-width-modulated motor speed controller	19
Enhanced supply supervisor	20
Two-phase nonoverlapping clock generator	21



NOTES: A. The recommended minimum capacitance is 10 µF to eliminate common ground switching noise.
B. Select C1 for change in oscillator frequency.

Figure 19. Pulse-Width-Modulated Motor Speed Controller

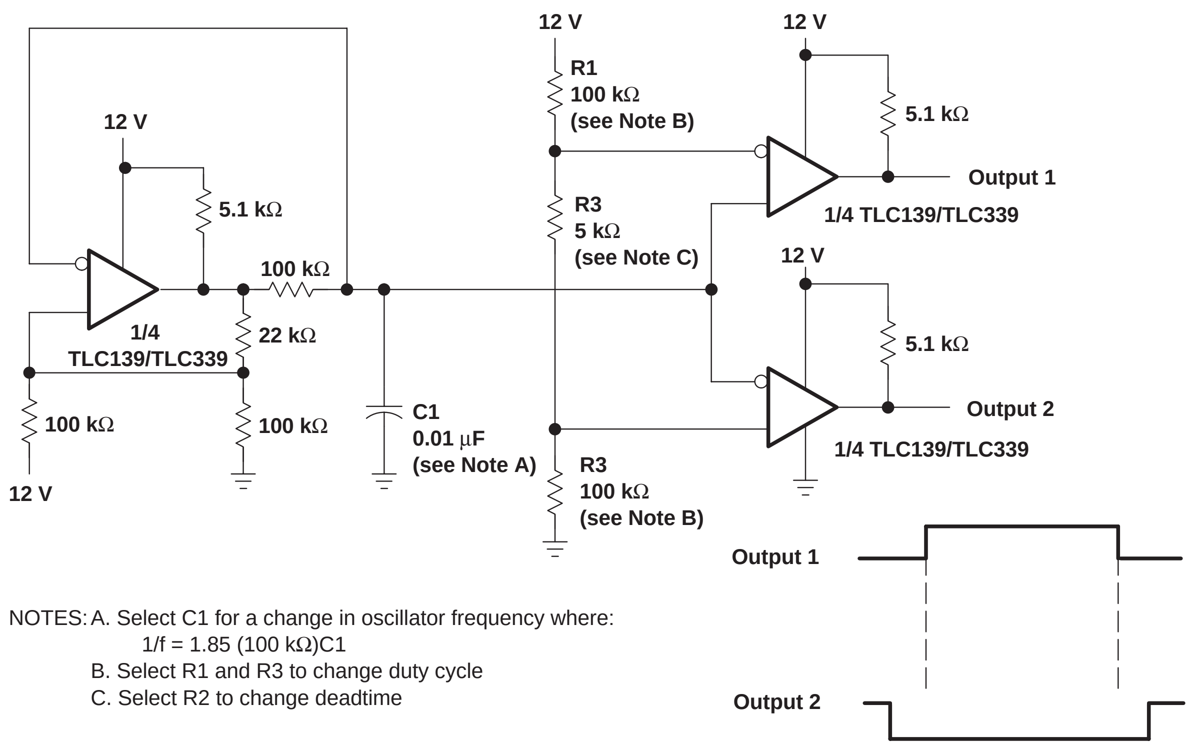
TYPICAL APPLICATION DATA



NOTES: A. $V_{UNREG} = 2.5\left(\frac{R1 + R2}{R2}\right)$

B. The value of C_t determines the time delay of reset.

Figure 20. Enhanced Supply Supervisor



NOTES: A. Select C1 for a change in oscillator frequency where:
$1/f = 1.85\ (100\ k\Omega)C1$
B. Select R1 and R3 to change duty cycle
C. Select R2 to change deadtime

Figure 21. Two-Phase Nonoverlapping Clock Generator

PACKAGING INFORMATION

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/Ball Finish	MSL Peak Temp [(3)]
5962-87659022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8765902CA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9555001NXDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC139MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TLC139MJ	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
TLC139MJB	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
TLC339CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLC339CDBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC339CDBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC339CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLC339CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLC339CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLC339CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC339CN10	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
TLC339CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC339CNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC339CNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC339CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC339CPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC339CPWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
TLC339CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC339CPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC339ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLC339IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLC339IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLC339IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLC339IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC339INE4	ACTIVE	PDIP	N	14	25	Pb-Free	CU NIPDAU	N / A for Pkg Type

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
						(RoHS)		
TLC339IPW	ACTIVE	TSSOP	PW	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC339IPWG4	ACTIVE	TSSOP	PW	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC339IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC339IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC339MD	ACTIVE	SOIC	D	14	50	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC339MDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC339MDR	ACTIVE	SOIC	D	14	2500	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC339MDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC339MN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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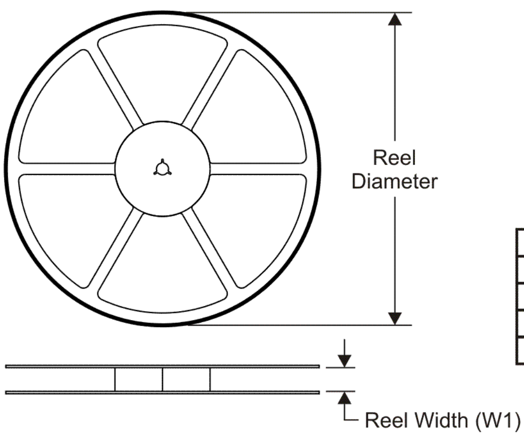
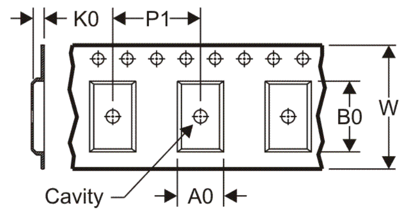
TAPE AND REEL INFORMATION

REEL DIMENSIONS

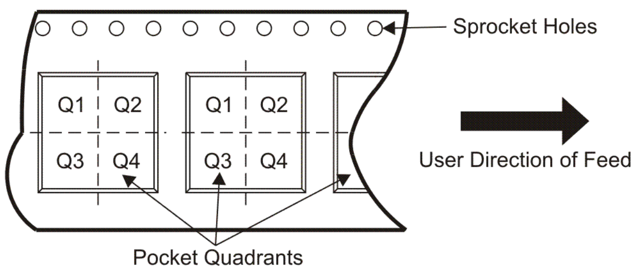


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

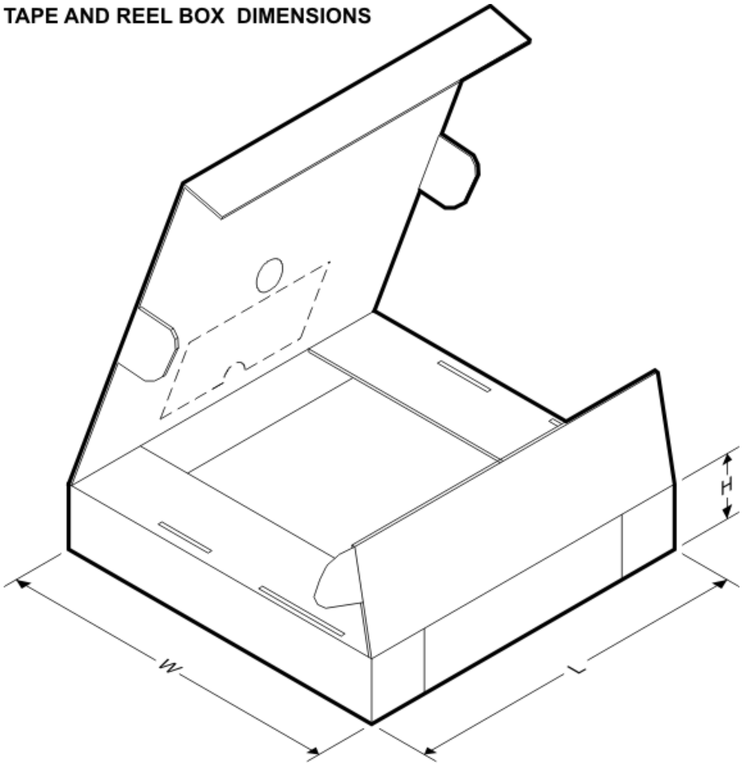
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC339CDBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TLC339CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC339CPWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
TLC339IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC339IPWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

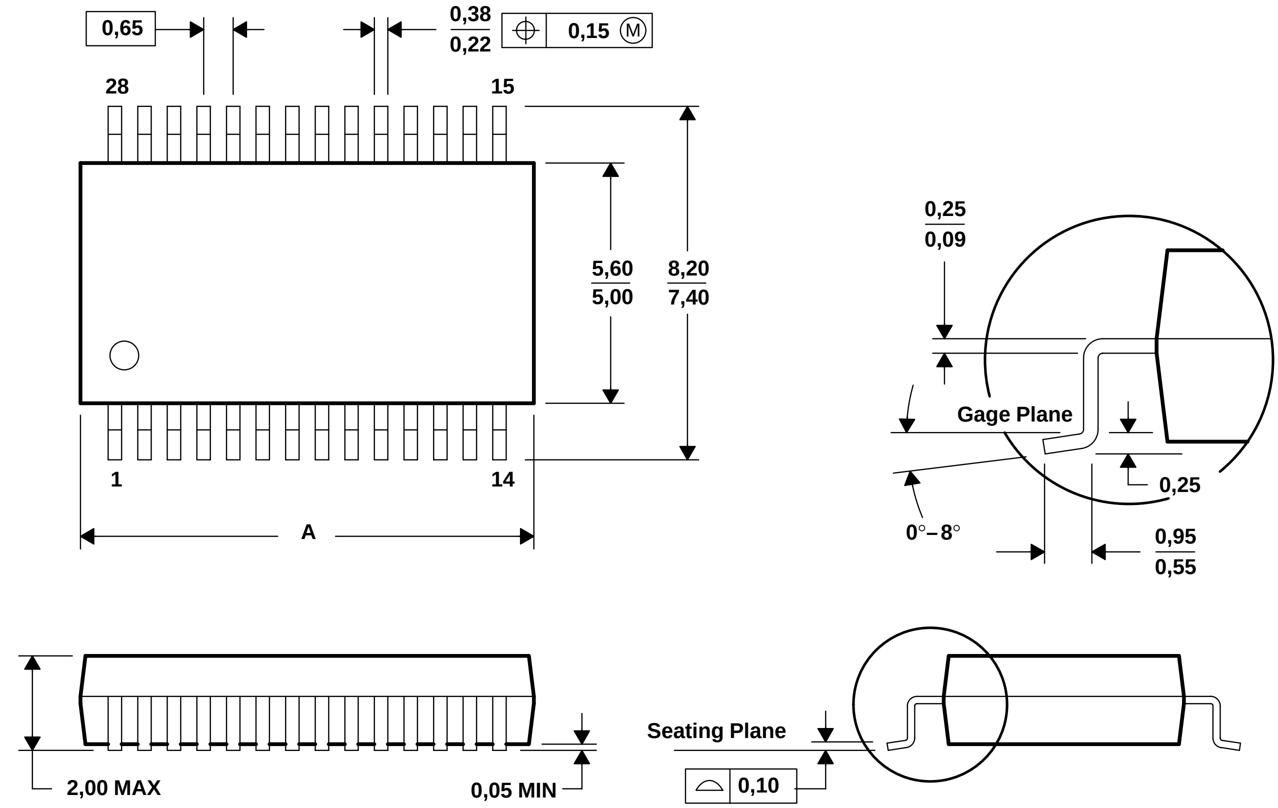


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC339CDBR	SSOP	DB	14	2000	346.0	346.0	33.0
TLC339CDR	SOIC	D	14	2500	346.0	346.0	33.0
TLC339CPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
TLC339IDR	SOIC	D	14	2500	346.0	346.0	33.0
TLC339IPWR	TSSOP	PW	14	2000	346.0	346.0	29.0

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



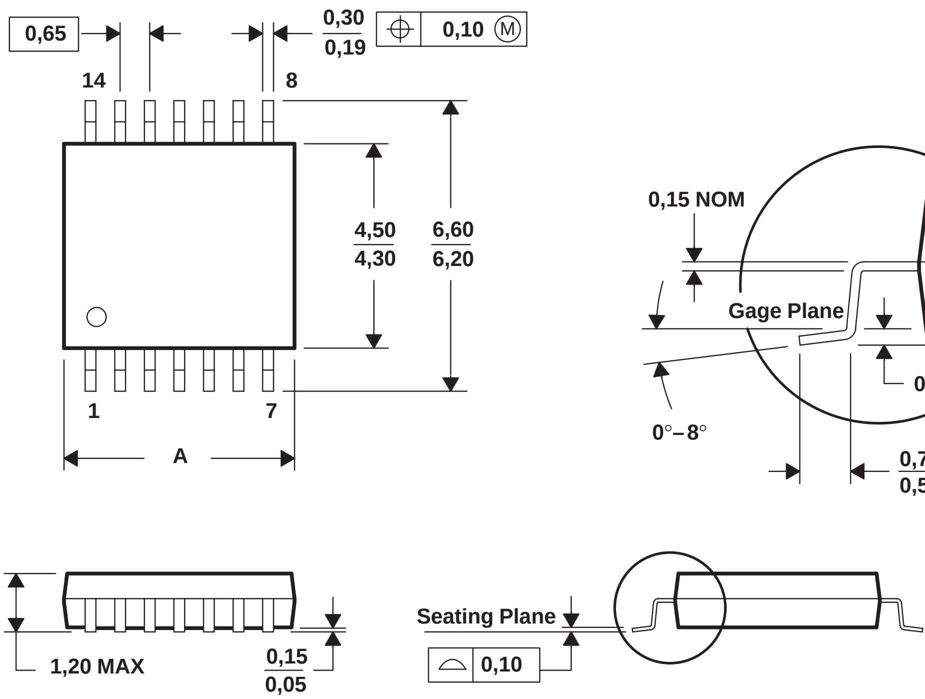
PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



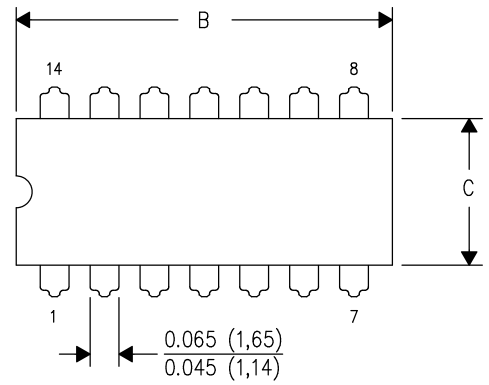
PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

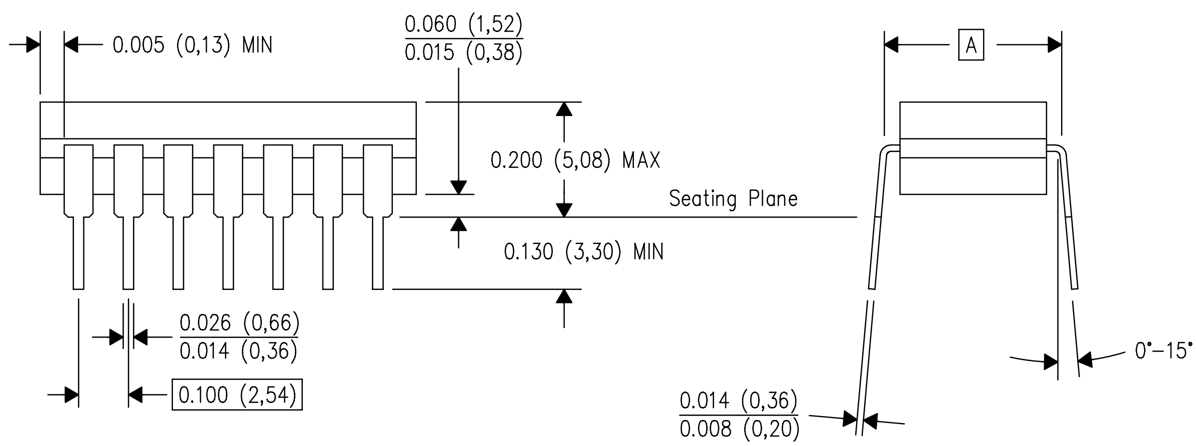
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

J (R–GDIP–T**) CERAMIC DUAL IN-LINE PACKAGE

14 LEADS SHOWN



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

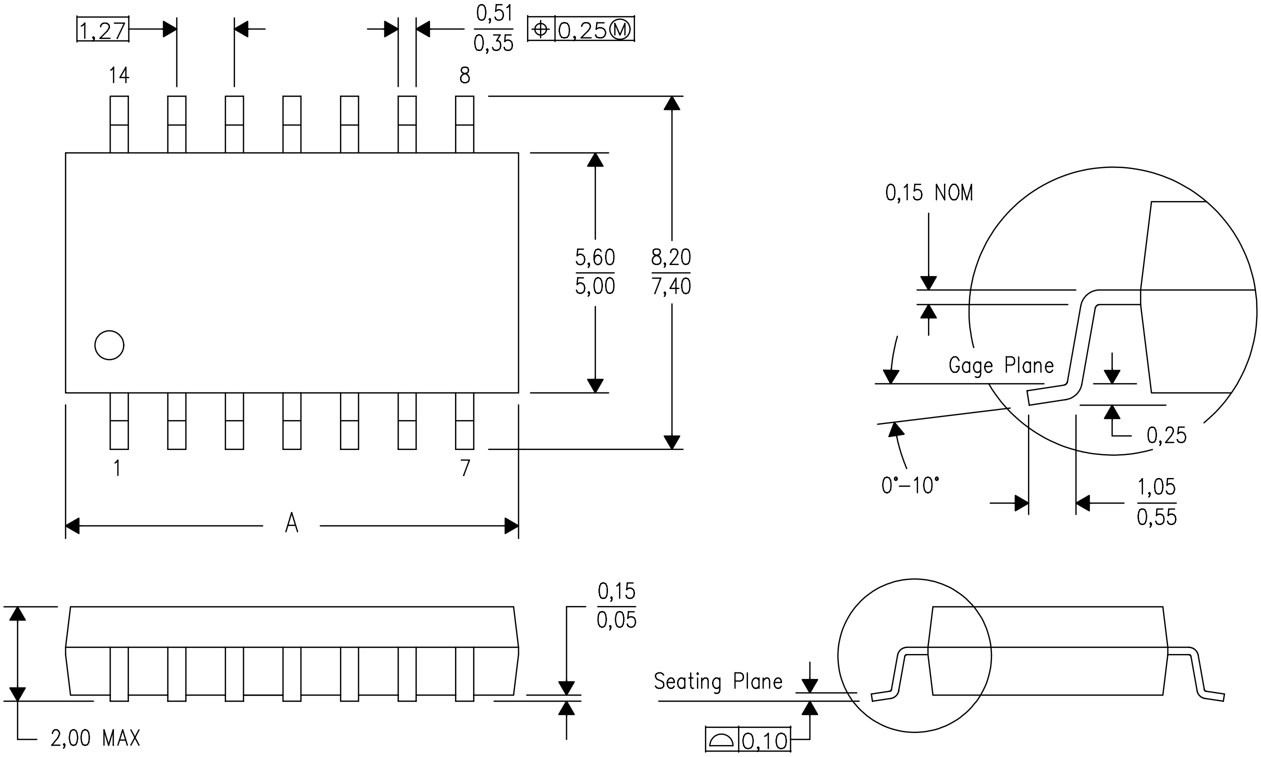


4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



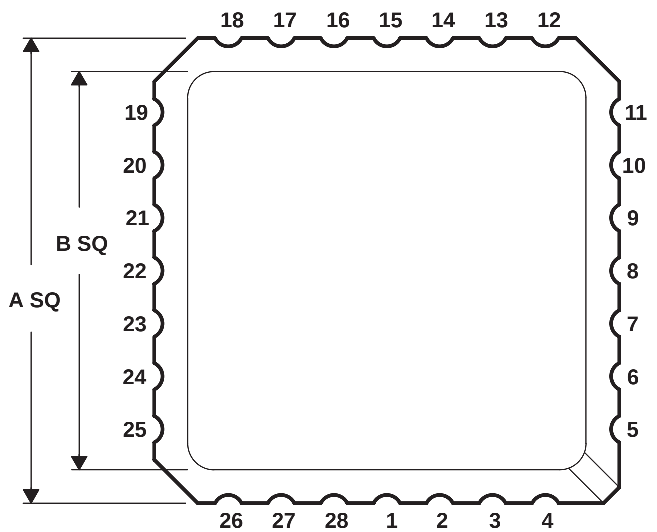
PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

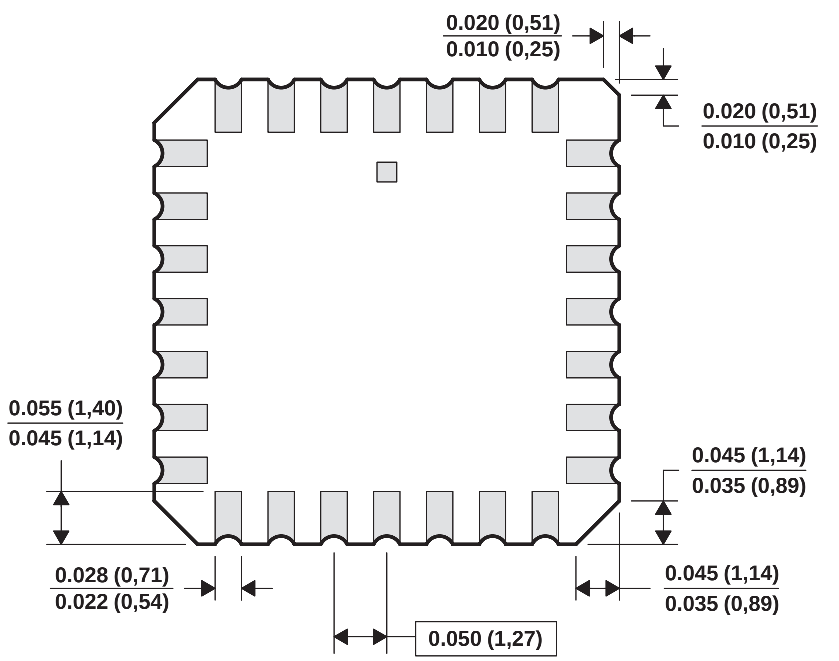
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

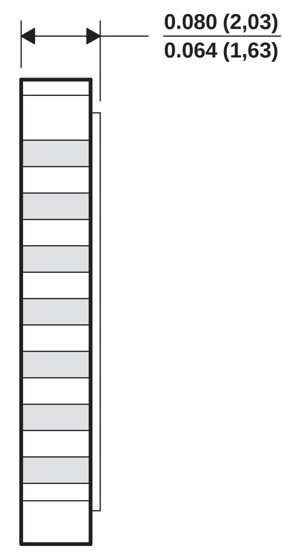
FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

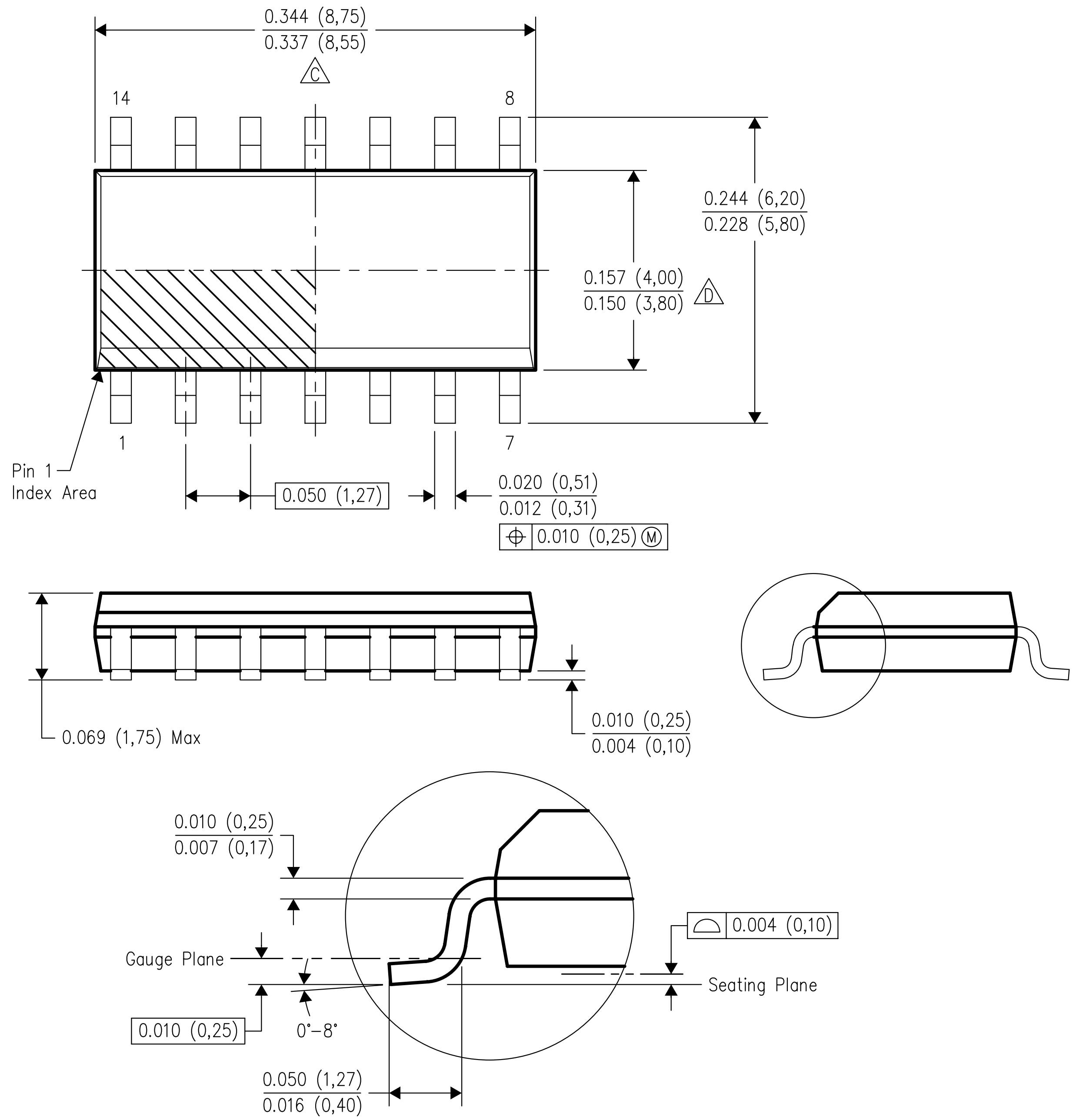




4040140 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE

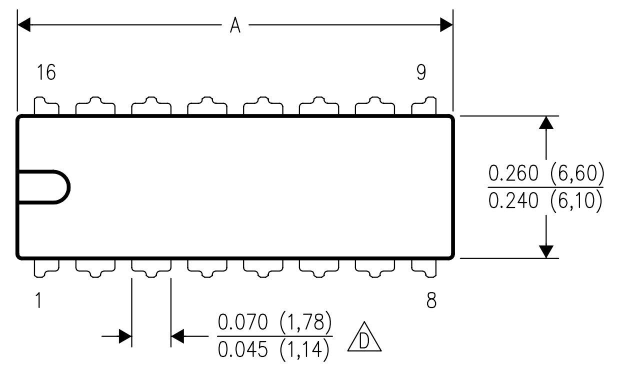


4040047–3/H 11/2006

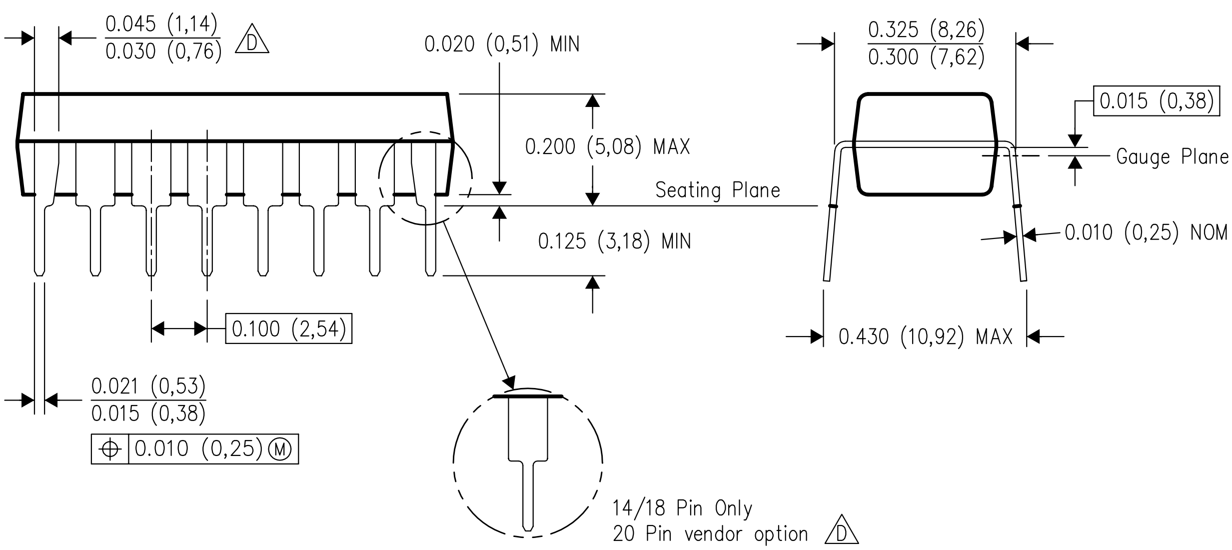
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
(C) MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
(C) Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
(D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

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Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
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		Wireless	www.ti.com/wireless

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