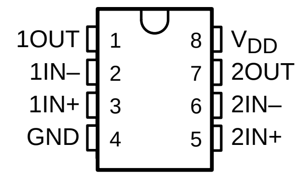
TLC352
LinCMOS™ DUAL DIFFERENTIAL COMPARATOR

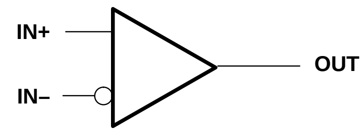
SLCS016A – SEPTEMBER 1985 – REVISED SEPTEMBER 2002

- **Single- or Dual-Supply Operation**
- **Wide Range of Supply Voltages 1.5 V to 18 V**
- **Very Low Supply Current Drain 150 μA Typ at 5 V 65 μA Typ at 1.4 V**
- **Built-In ESD Protection**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Extremely Low Input Bias Current 5 pA Typ**
- **Ultrastable Low Input Offset Voltage**
- **Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23 μV/ Month, Including the First 30 Days**
- **Common-Mode Input Voltage Range Includes Ground**
- **Outputs Compatible With TTL, MOS, and CMOS**
- **Pin-Compatible With LM393**

TLC352C, TLC352I . . . D OR P PACKAGE
(TOP VIEW)



symbol (each comparator)



description

This device is fabricated using LinCMOS™ technology and consists of two independent voltage comparators, each designed to operate from a single power supply. Operation from dual supplies is also possible if the difference between the two supplies is 1.4 V to 18 V. Each device features extremely high input impedance (typically greater than 10^{12} Ω), which allows direct interface to high-impedance sources. The output are n-channel open-drain configurations and can be connected to achieve positive-logic wired-AND relationships. The capability of the TLC352 to operate from 1.4-V supply makes this device ideal for low-voltage battery applications.

The TLC352 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

The TLC352C is characterized for operation from 0°C to 70°C. The TLC352I is characterized for operation over the industrial temperature range of – 40°C to 85°C.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE	
		SMALL-OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	5 mV	TLC352CD	TLC352CP
– 40°C to 85°C	5 mV	TLC352ID	TLC352IP

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC352 CDR).

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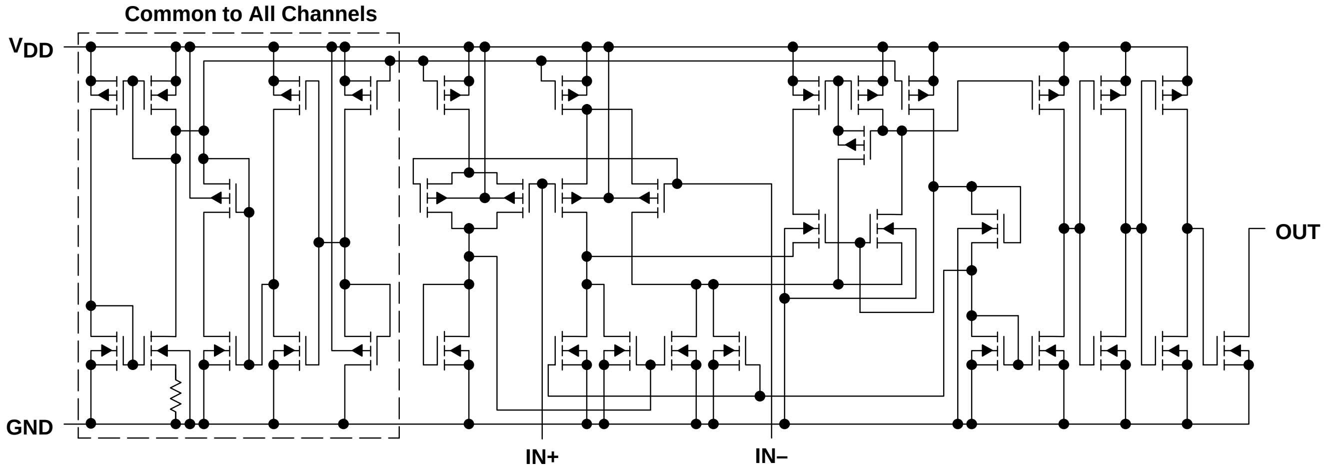
equivalent schematic (each comparator)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . 18 V
Differential input voltage, V_{ID} (see Note 2) . . . ± 18 V
Input voltage, V_I . . . V_{DD}
Input voltage range, V_I . . . – 0.3 V to 18 V
Output voltage, V_O . . . 18 V
Input current, I_I . . . ± 5 mA
Output current, I_O . . . 20 mA
Duration of output short circuit to ground (see Note 3) . . . unlimited
Continuous total dissipation . . . See Dissipation Rating Table
Operating free-air temperature range, T_A TLC352C . . . 0°C to 70°C
TLC352I . . . – 40°C to 85°C
Storage temperature range . . . – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values except differential voltages are with respect to the network ground.
2. Differential voltages are at IN+ with respect to IN –.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW
P	500 mW	N/A	N/A	500 mW	500 mW

recommended operating conditions

		TLC352C		TLC352I		UNIT
		MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}		1.4	16	1.4	16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0	3.5	0	3.5	V
	V_{DD} = 10 V	0	8.5	0	8.5	
Operating free-air temperature, T_A		0	70	– 40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC352C			TLC352I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$ min, See Note 4	25°C		2	5		2	5	mV
			Full range			6.5			7	
I_{IO}	Input offset current		25°C		1			1		pA
			MAX			0.3			1	nA
I_{IB}	Input bias current		25°C		5			5		pA
			MAX			0.6			2	nA
V_{ICR}	Common-mode input voltage range		Full range	0 to 0.2			0 to 0.2			V
V_{OL}	Low-level output voltage		25°C		100	200		100	200	mV
			Full range			200			200	
I_{OL}	Low-level output current	V_{ID} = – 0.5 V, V_{OL} = 0.3 V	25°C	1	1.6		1	1.6		mA
I_{DD}	Supply current (two comparators)	V_{ID} = 0.5 V, No load	25°C		65	150		65	150	µA
			Full range			200			200	

† All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC352C, – 40°C to 85°C for TLC352I. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 1.25 V or below 150 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC352C MIN	TLC352C TYP	TLC352C MAX	TLC352I MIN	TLC352I TYP	TLC352I MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$ min,	See Note 5	25°C		1	5		1	5	mV
				Full range			6.5			7	
I_{IO}	Input offset current			25°C		1			1		pA
				MAX			0.3			1	nA
I_{IB}	Input bias current			25°C		5			5		pA
				MAX			0.6			2	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD} – 1			0 to V_{DD} – 1			V
				Full range	0 to V_{DD} – 1.5			0 to V_{DD} – 1.5			
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1	µA
V_{OL}	Low-level output voltage	V_{ID} = 1 V,	I_{OL} = 4 mA	25°C		150	400		150	400	mV
				Full range			700			700	
I_{OL}	Low-level output current	V_{ID} = – 1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		mA
I_{DD}	Supply current (two comparators)	V_{ID} = 1 V,	No load	25°C		0.15	0.3		0.15	0.3	mA
				Full range			0.4			0.4	

† All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC352C, – 40°C to 85°C for TLC352I. IMPORTANT: See Parameter Measurement Information.

NOTE 5: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TLC352C, TLC352I MIN	TLC352C, TLC352I TYP	TLC352C, TLC352I MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ,, C_L = 15 pF‡, See Note 6	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

‡ C_L includes probe and jig capacitance.

NOTE 6: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLC352 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternative for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output changes state.

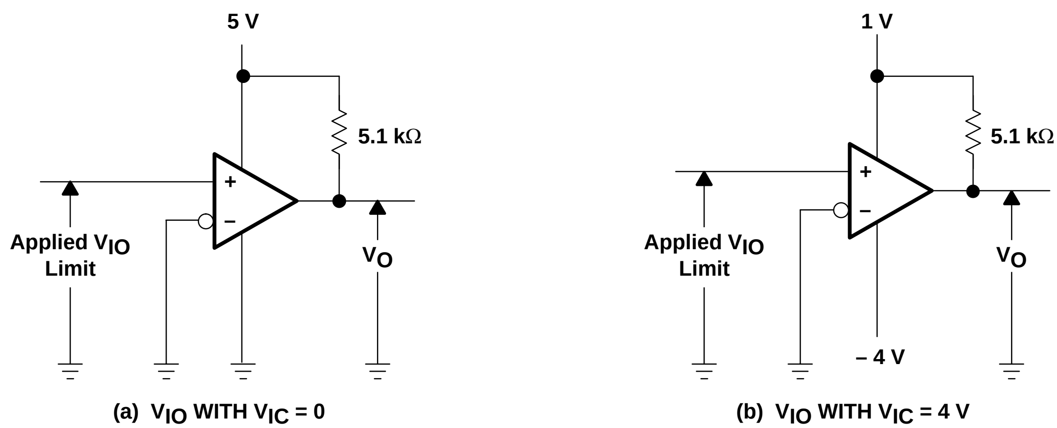


Figure 1. Method for Verifying That Input Offset Voltage Is Within Specified Limits

PARAMETER INFORMATION

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

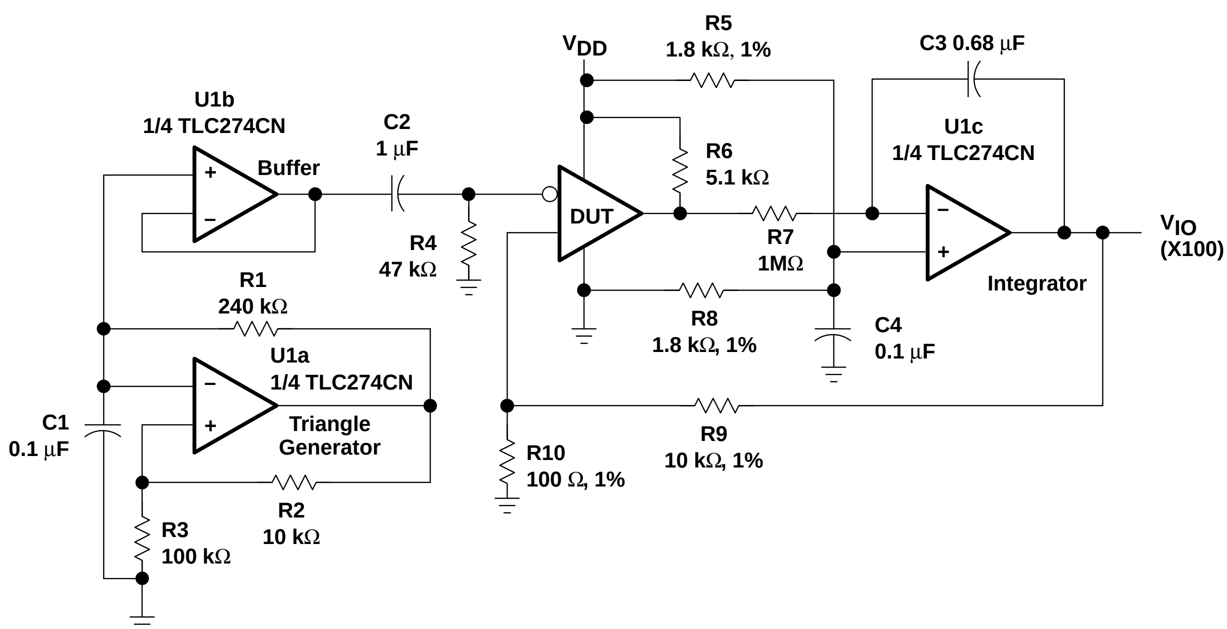
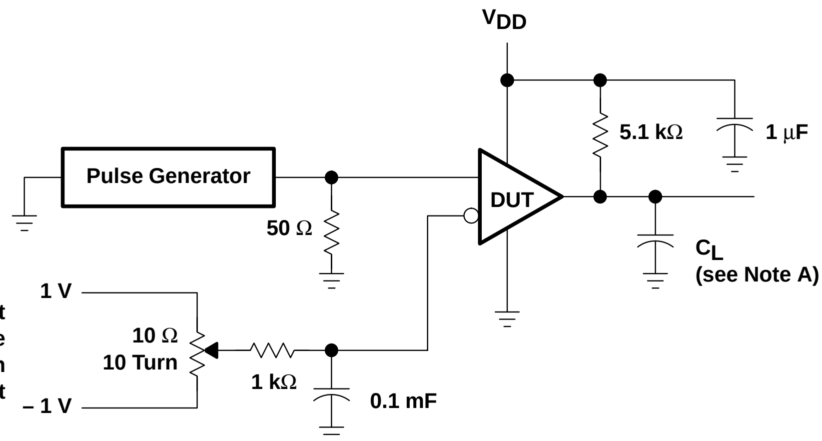


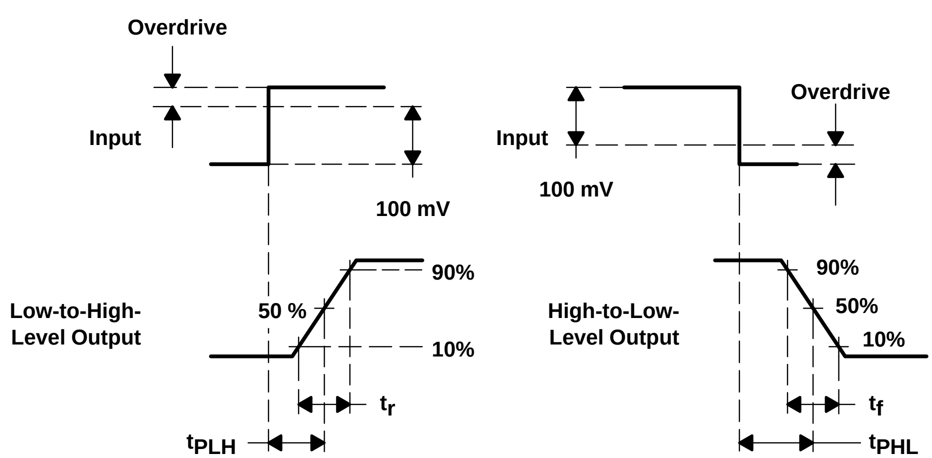
Figure 2. Circuit for Input Offset Voltage Measurement

PARAMETER MEASUREMENT INFORMATION

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output, is measured from the leading edge of the input pulse, while response time, high-to-low level output, is measured from the trailing edge of the input pulse. Response-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, causes the output to change state.



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

Figure 3. Response, Rise, and Fall Times Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLC352CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC352CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC352CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC352CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC352CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC352CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC352CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC352CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC352ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC352IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC352IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC352IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC352IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC352IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC352IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC352IPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC352IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC352IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and

package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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