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TLVx172 36-V, Single-Supply, Low-Power Operational Amplifiers for Cost-Sensitive Systems

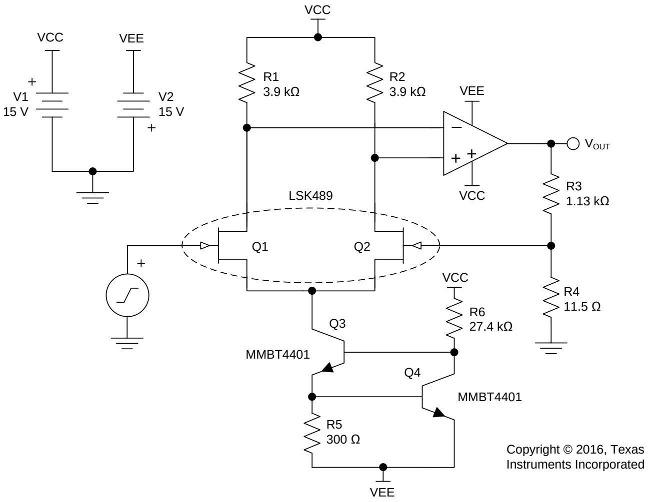
1 Features

- Supply Range: 4.5 V to 36 V, ±2.25 V to ±18 V
- Low Noise: 9 nV/√Hz
- Low Offset Drift: ±1 µV/°C (typical)
- EMI-Hardened
- Input Range Includes the Negative Supply
- Rail-to-Rail Output
- Gain Bandwidth: 10 MHz
- Slew Rate: 10 V/µs
- Low Quiescent Current: 1.6 mA per Amplifier
- High Common-Mode Rejection: 116 dB (typical)
- Low Input Bias Current: 10 pA

2 Applications

- TFT-LCD Drive Circuits
- Touch-Screen Displays
- Wireless LANs
- Portable Instrumentation
- Analog-to-Digital Converter (ADC) Buffers
- Active Filters
- Line Drivers or Line Receivers
- Ultrasound
- Currency Counters
- Transducer Amplifiers

Simplified Schematic



3 Description

The TLVx172 family of electromagnetic interference (EMI)-hardened, 36-V, single-supply, low-noise operational amplifiers (op amps) features a THD+N of 0.0002% at 1 kHz with the ability to operate on supplies ranging from 4.5 V (±2.25 V) to 36 V (±18 V). These features, along with low noise and very high PSRR, make the TLVx172 an excellent choice for microvolt-level signal amplification. The TLVx172 family of devices offer good offset and drift, a high bandwidth of 10 MHz, and a slew rate of 10 V/µs with only 2.3 mA (max) of quiescent current over temperature.

Unlike most operational amplifiers that are specified at only one supply voltage, the TLVx172 family of operational amplifiers is specified from 4.5 V to 36 V. Input signals beyond the supply rails do not cause phase reversal. The TLVx172 family is stable with capacitive loads up to 300 pF. The input can operate 100 mV below the negative rail and within 2 V of the positive rail for normal operation. Note that these devices can operate with a full rail-to-rail input 100 mV beyond the positive rail, but with reduced performance within 2 V of the positive rail.

The TLVx172 operational amplifiers are specified from –40°C to +125°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV172	SOIC (8)	4.90 mm × 3.91 mm
	SC70 (5)	2.00 mm × 1.25 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
TLV2172	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm
TLV4172	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 Revision History

DATE	REVISION	NOTES
November 2016	*	Initial release.

5 Device Comparison

Device Comparison

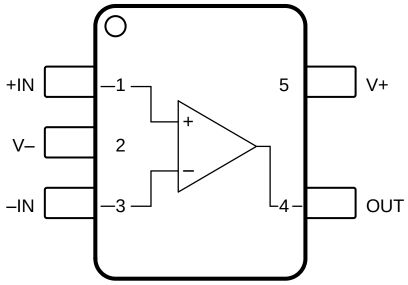
DEVICE	PACKAGE
TLV172 (single)	SC70-5, SOT-23-5, SOIC-8
TLV2172 (dual)	SOIC-8, VSSOP-8
TLV4172 (quad)	SOIC-14, TSSOP-14

Device Family Comparison

DEVICE	QUIESCENT CURRENT (I_Q)	GAIN BANDWIDTH PRODUCT (GBP)	VOLTAGE NOISE DENSITY (e_n)
TLVx172	1600 µA	10 MHz	9 nV/$\sqrt{Hz}$
TLVx171	525 µA	3.0 MHz	16 nV/$\sqrt{Hz}$
TLVx170	125 µA	1.2 MHz	22 nV/$\sqrt{Hz}$

6 Pin Configuration and Functions

**TLV172: DCK Package
5-Pin SC70
Top View**



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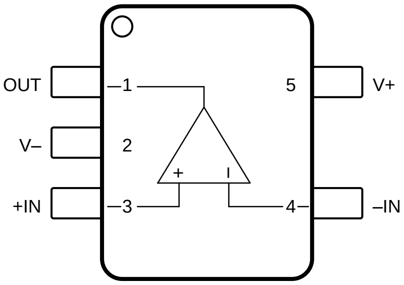
**TLV172: DBV Package
5-Pin SOT-23
Top View**



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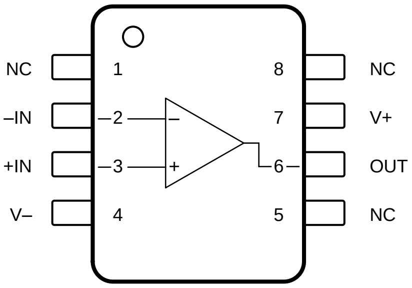
**TLV172: D Package
8-Pin SOIC
Top View**



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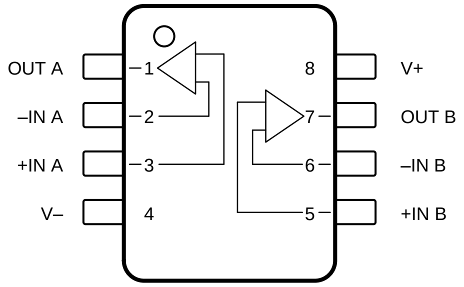
Pin Functions: TLV172

PIN				I/O	DESCRIPTION
NAME	SC70 (DCK)	SOT-23 (DBV)	SOIC (D)		
–IN	3	4	2	I	Negative (inverting) input
+IN	1	3	3	I	Positive (noninverting) input
NC	—	—	1, 5, 8	—	No internal connection (can be left floating)
OUT	4	1	6	O	Output
V–	2	2	4	—	Negative (lowest) power supply
V+	5	5	7	—	Positive (highest) power supply

**TLV2172: D and DGK Packages
8-Pin SOIC and VSSOP
Top View**



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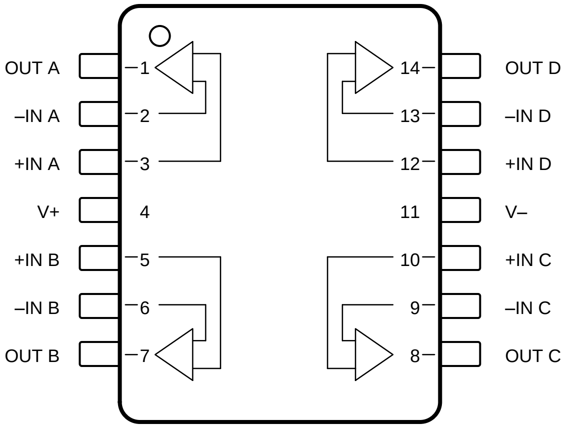
Pin Functions: TLV2172

PIN			I/O	DESCRIPTION
NAME	SOIC (D)	VSSOP (DGK)		
–IN A	2	2	I	Inverting input, channel A
–IN B	6	6	I	Inverting input, channel B
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
V–	4	4	—	Negative (lowest) power supply
V+	8	8	—	Positive (highest) power supply

TLV4172: D and PW Packages
14-Pin SOIC and TSSOP
Top View



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Pin Functions: TLV4172

PIN			I/O	DESCRIPTION
NAME	SOIC (D)	TSSOP (PW)		
–IN A	2	2	I	Inverting input, channel A
–IN B	6	6	I	Inverting input, channel B
–IN C	9	9	I	Inverting input, channel C
–IN D	13	13	I	Inverting input, channel D
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
+IN C	10	10	I	Noninverting input, channel C
+IN D	12	12	I	Noninverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	8	8	O	Output, channel C
OUT D	14	14	O	Output, channel D
V–	11	11	—	Negative (lowest) power supply
V+	4	4	—	Positive (highest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Voltage	Supply voltage, V+ to V−		–20	20	V
	Single-supply voltage			40	
	Signal input pin(2)	Common-mode	(V–) – 0.5	(V+) + 0.5	
		Differential(3)	–0.5	0.5	
Current	Signal input pin		–10	10	mA
	Output short-circuit(4)		Continuous		
Temperature	Operating, T_A		–55	150	°C
	Junction, T_J			150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transient conditions that exceed these voltage ratings must be current limited to 10 mA or less.
(3) See the *Electrical Overstress* section for more information.
(4) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, (V+) – (V–)	Single-supply	4.5		36	V
	Dual-supply	±2.25		±18	
Specified temperature		–40		125	°C

7.4 Thermal Information: TLV172

THERMAL METRIC[1]		TLV172			UNIT
		D (SOIC)	DBV (SOT-23)	DCK (SC70)	
		8 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.5	227.9	285.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80.6	115.7	60.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.1	65.9	78.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	31.0	10.7	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.6	65.3	77.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: TLV2172

THERMAL METRIC[1]		TLV2172		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.1	158	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.8	48.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.6	78.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	22.5	3.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.1	77.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Thermal Information: TLV4172

THERMAL METRIC[1]		TLV4172		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	82.7	111.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.3	40.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.3	54.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.9	3.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37	53.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.7 Electrical Characteristics

at T_A = 25°C, V_S = ±2.25 V to ±18 V, $V_{CM} = V_{OUT} = V_S / 2$, and R_L = 10 kΩ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	T_A = 25°C			0.5	1.7	mV
		T_A = –40°C to +125°C				2	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C			1		µV/°C
PSRR	Power-supply rejection ratio	V_S = 4 V to 36 V, T_A = –40°C to +125°C		100	120		dB
	Channel separation, dc				5		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current	T_A = 25°C			±10		pA
I_{OS}	Input offset current	T_A = 25°C			±2		pA
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			2.5		μV_{PP}
e_n	Input voltage noise density	f = 100 Hz			14		nV/√Hz
		f = 1 kHz			9		nV/√Hz
i_n	Input current noise density	f = 1 kHz			1.6		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range(1)			(V–) – 0.1		(V+) – 2	V
CMRR	Common-mode rejection ratio	V_S = ±18 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V, T_A = –40°C to +125°C		94	116		dB
INPUT IMPEDANCE							
	Differential				100 || 4		MΩ || pF
	Common-mode				6 || 4		10^{13} Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.35 V < V_O < (V+) – 0.35 V, T_A = –40°C to +125°C		97	115		dB
		(V–) + 0.5 V < V_O < (V+) – 0.5 V, R_L = 2 kΩ, T_A = –40°C to +125°C			107		
FREQUENCY RESPONSE							
GBP	Gain bandwidth product				10		MHz
SR	Slew rate	G = +1			10		V/µs
t_S	Settling time	To 0.1%, V_S = ±18 V, G = +1, 10-V step			2		µs
		To 0.01% (12-bit), V_S = ±18 V, G = +1, 10-V step			3.2		
	Overload recovery time	V_{IN} × gain > V_S			200		ns
THD+N	Total harmonic distortion + noise	V_S = 36 V, G = +1, f = 1 kHz, V_O = 3.5 V_{RMS}			0.0002%		
OUTPUT							
V_O	Voltage output swing from rail	V_S = ±18 V, R_L = 10 kΩ	T_A = 25°C		70		mV
			T_A = –40°C to +125°C		95		
		V_S = ±18 V, R_L = 2 kΩ	T_A = 25°C		330	400	
			T_A = –40°C to +125°C		470	530	
I_{SC}	Short-circuit current				±75		mA
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*		pF
R_O	Open-loop output resistance	f = 1 MHz, I_O = 0 A			60		Ω
POWER SUPPLY							
V_S	Specified voltage range			4.5		36	V
I_Q	Quiescent current per amplifier	I_O = 0 A, T_A = –40°C to +125°C			1.6	2.3	mA

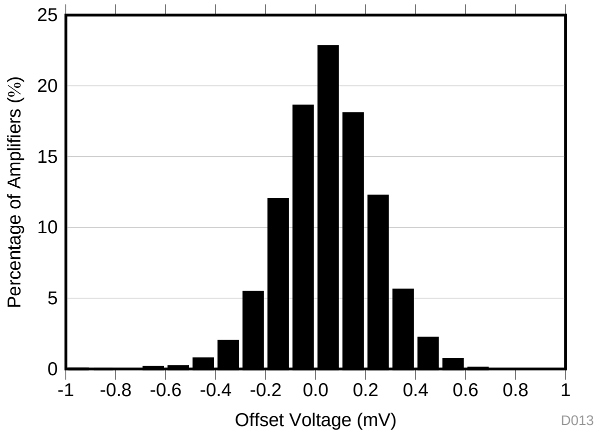
(1) The input range can be extended beyond (V+) – 2 V up to V+. See the *Typical Characteristics* and *Application and Implementation* sections for additional information.

7.8 Typical Characteristics

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

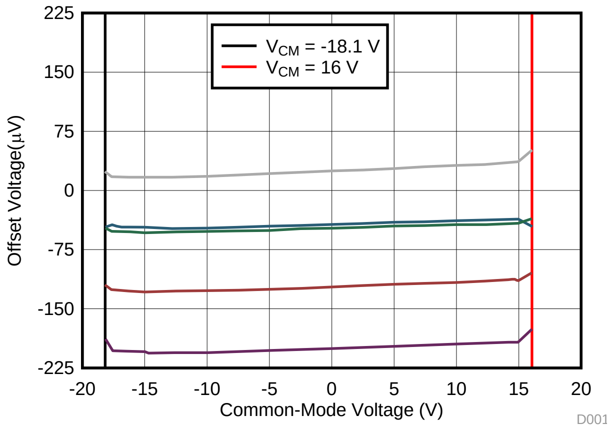
Table 1. Characteristic Performance Measurements

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage vs Common-Mode Voltage	Figure 2
Offset Voltage vs Common-Mode Voltage (Upper Stage)	Figure 3
Input Bias Current vs Temperature	Figure 4
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 5
CMRR and PSRR vs Frequency (Referred-to-Input)	Figure 6
0.1-Hz to 10-Hz Noise	Figure 7
Input Voltage Noise Spectral Density vs Frequency	Figure 8
Quiescent Current vs Supply Voltage	Figure 9
Open-Loop Gain and Phase vs Frequency	Figure 10
Closed-Loop Gain vs Frequency	Figure 11
Open-Loop Output Impedance vs Frequency	Figure 12
Small-Signal Overshoot vs Capacitive Load	Figure 13, Figure 14
No Phase Reversal	Figure 15
Small-Signal Step Response (10 mV)	Figure 16, Figure 17
Large-Signal Step Response	Figure 18, Figure 19
Large-Signal Settling Time	Figure 20, Figure 21
Short-Circuit Current vs Temperature	Figure 22
Maximum Output Voltage vs Frequency	Figure 23
EMIRR IN+ vs Frequency	Figure 24



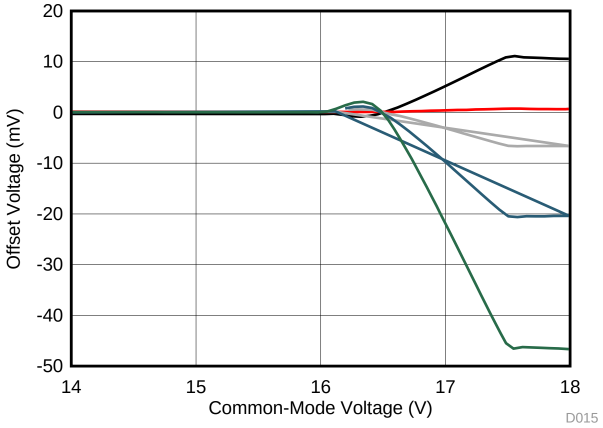
Distribution taken from 5185 amplifiers

Figure 1. Offset Voltage Production Distribution Histogram



5 typical units shown, V_S = ±18 V

Figure 2. Offset Voltage vs Common-Mode Voltage



5 typical units shown, V_S = ±18 V

Figure 3. Offset Voltage vs Common-Mode Voltage (Upper Stage)

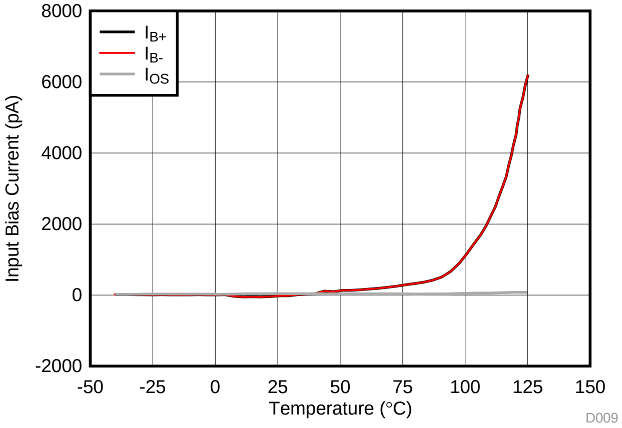


Figure 4. Input Bias Current vs Temperature

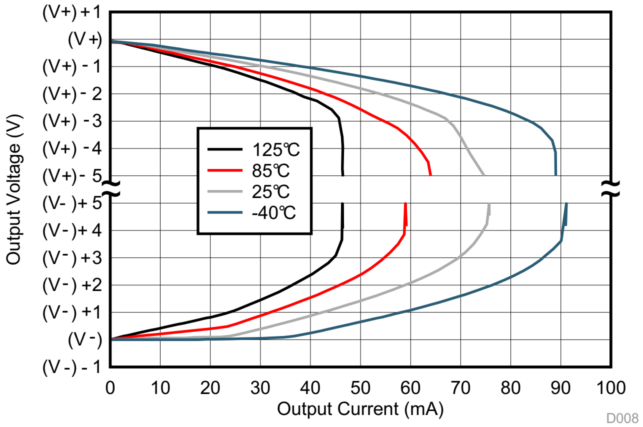


Figure 5. Output Voltage Swing vs Output Current (Maximum Supply)

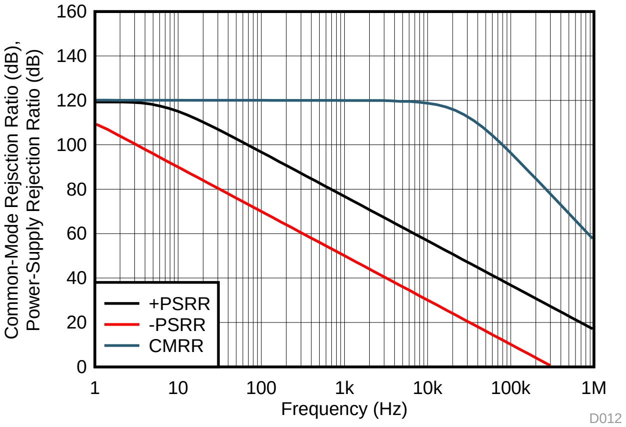


Figure 6. CMRR and PSRR vs Frequency (Referred-to-Input)

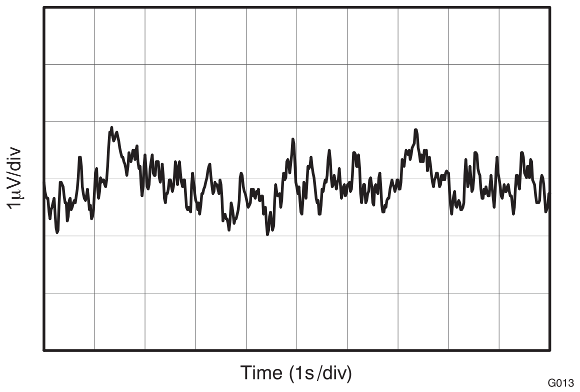


Figure 7. 0.1-Hz to 10-Hz Noise

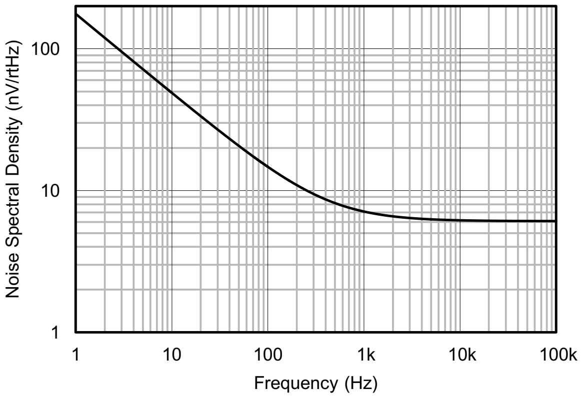


Figure 8. Input Voltage Noise Spectral Density vs Frequency

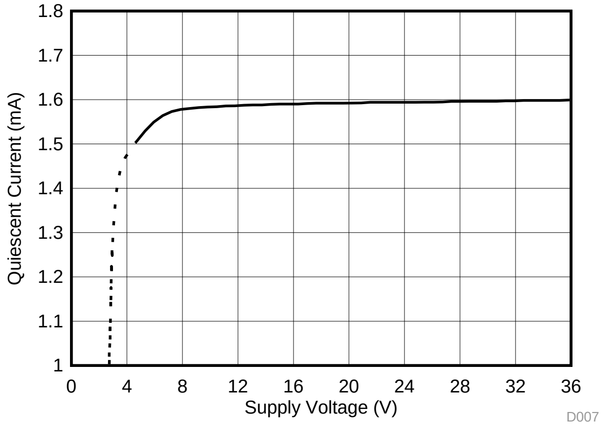
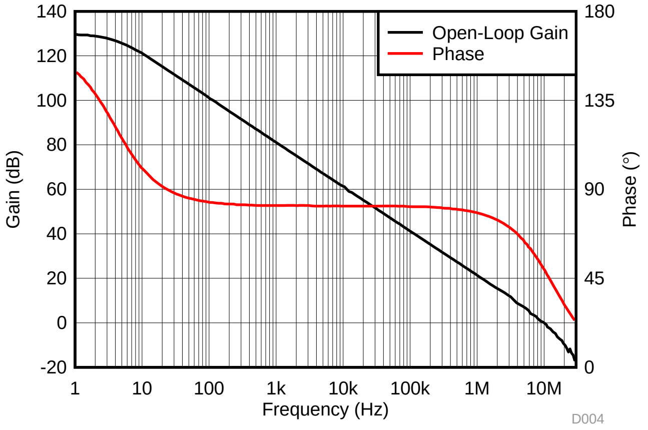


Figure 9. Quiescent Current vs Supply Voltage



C_{LOAD} = 15 pF

Figure 10. Open-Loop Gain and Phase vs Frequency

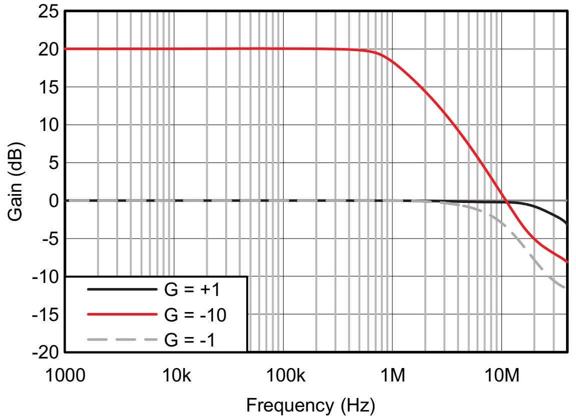


Figure 11. Closed-Loop Gain vs Frequency

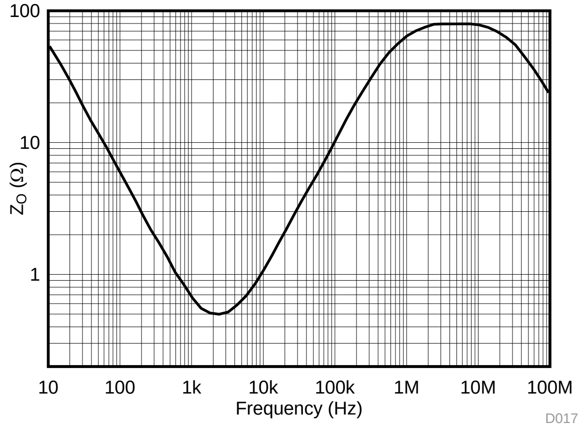
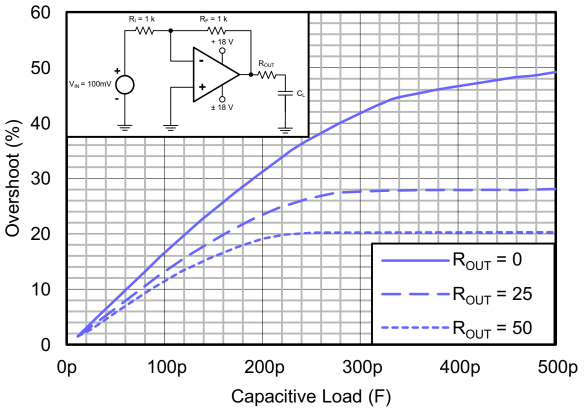
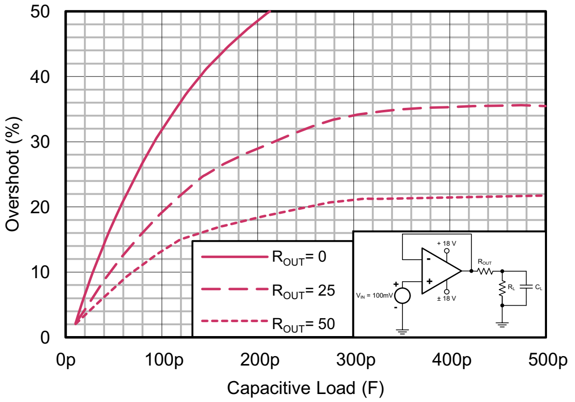


Figure 12. Open-Loop Output Impedance vs Frequency



100-mV output step, G = –1

Figure 13. Small-Signal Overshoot vs Capacitive Load



100-mV output step, G = +1

Figure 14. Small-Signal Overshoot vs Capacitive Load

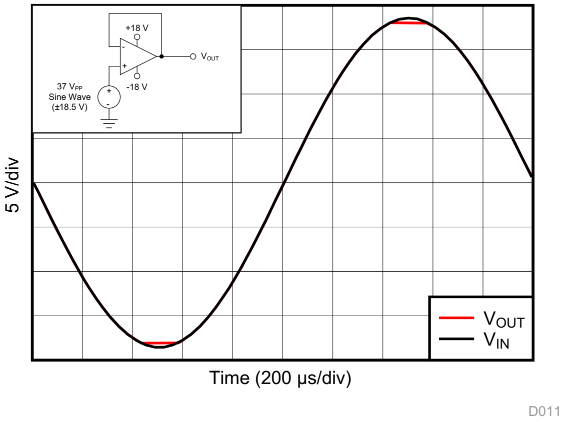
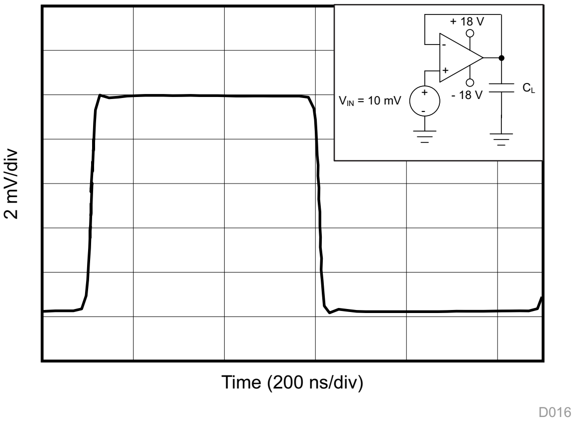
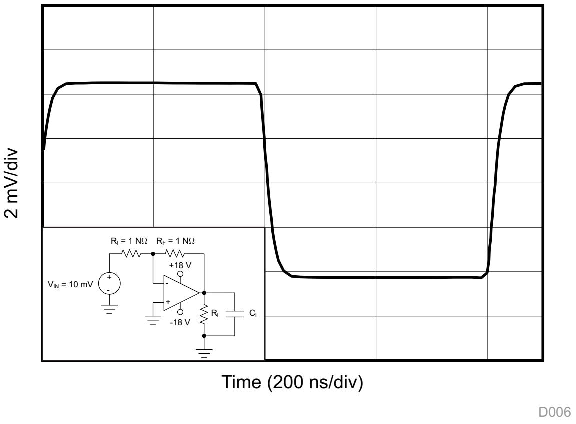


Figure 15. No Phase Reversal



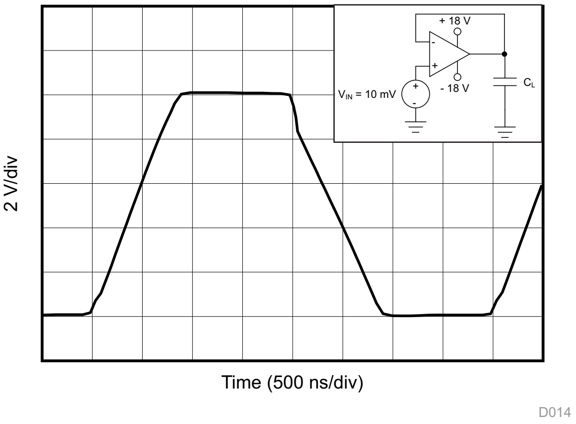
C_L = 10 pF

Figure 16. Small-Signal Step Response (10 mV)



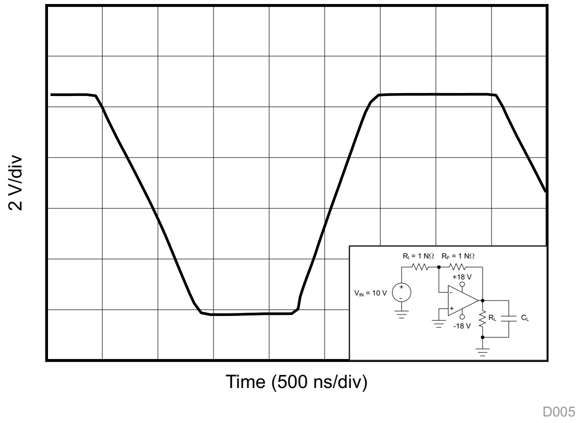
R_L = 1 kΩ, C_L = 10 pF

Figure 17. Small-Signal Step Response (10 mV)



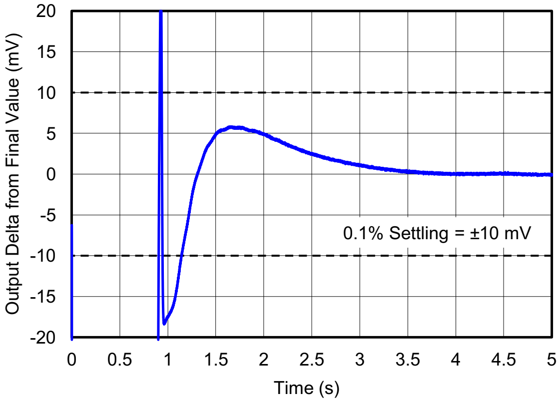
C_L = 10 pF

Figure 18. Large-Signal Step Response



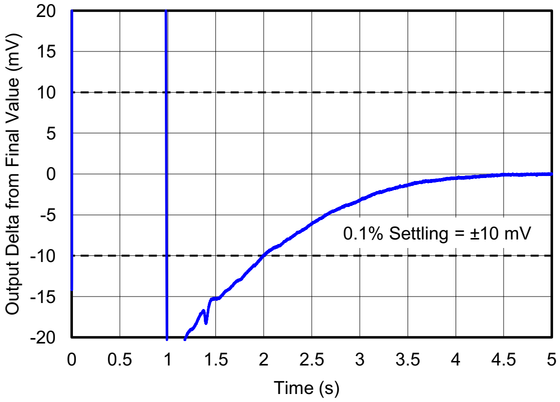
R_L = 1 kΩ, C_L = 10 pF

Figure 19. Large-Signal Step Response



10-V positive step, G = +1, C_L = 10 pF

Figure 20. Large-Signal Settling Time



10-V negative step, G = +1, C_L = 10 pF

Figure 21. Large-Signal Settling Time

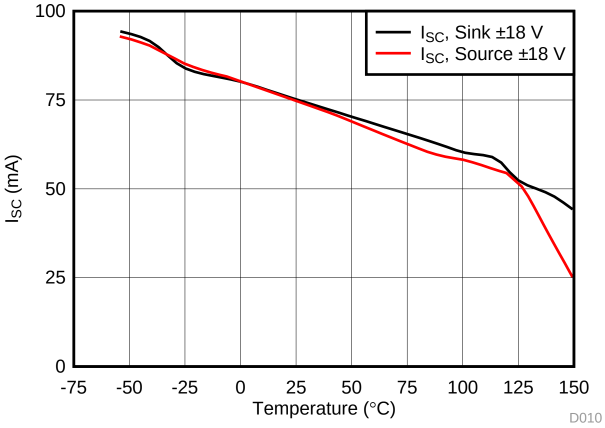


Figure 22. Short-Circuit Current vs Temperature

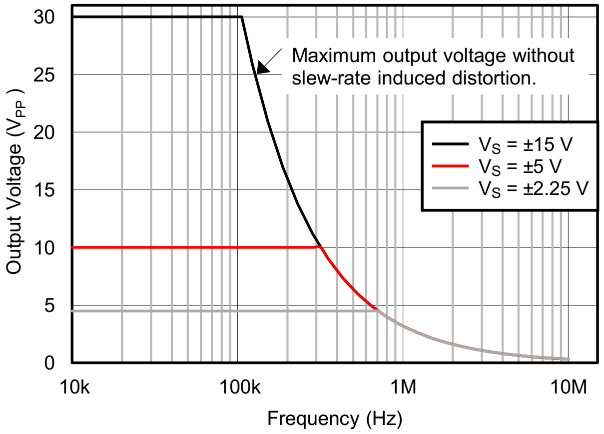
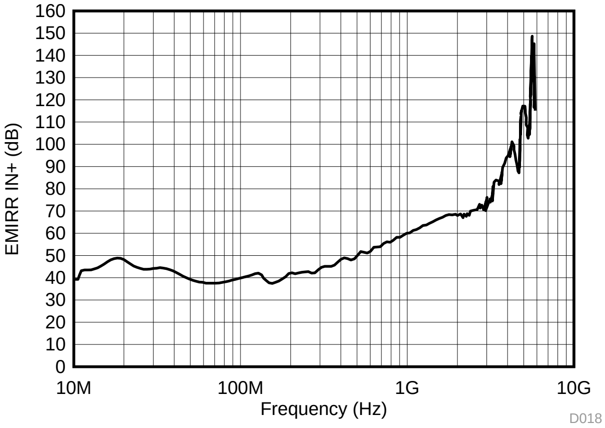


Figure 23. Maximum Output Voltage vs Frequency



P_{RF} = –10 dBm, V_{SUPPLY} = ±18 V, V_{CM} = 0 V

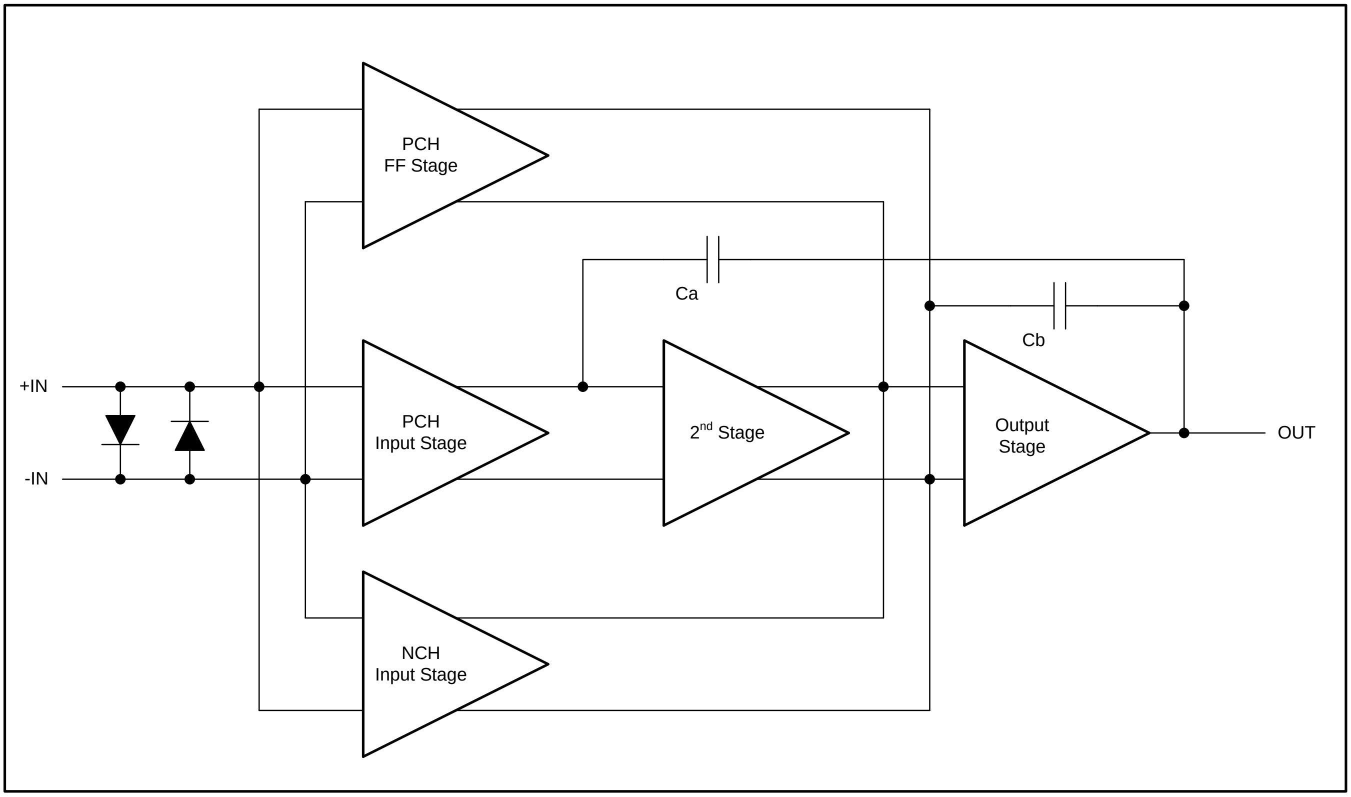
Figure 24. EMIRR IN+ vs Frequency

8 Detailed Description

8.1 Overview

The TLVx172 family of operational amplifiers provides high overall performance, making these devices ideal for many general-purpose applications. The excellent offset drift of only 2 μV/°C provides excellent stability over the entire temperature range. In addition, the family offers very good overall performance with high CMRR, PSRR, and A_{OL}.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Characteristics

The TLVx172 family of amplifiers is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

Feature Description (continued)

8.3.2 Phase-Reversal Protection

The TLVx172 family has an internal phase-reversal protection. Many operational amplifiers exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the TLVx172 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in Figure 25.

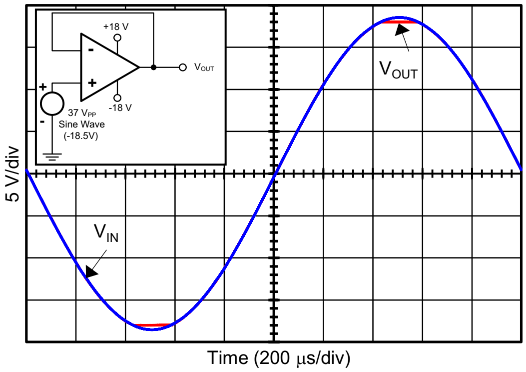


Figure 25. No Phase Reversal

8.3.3 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits for protection from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. Figure 26 illustrates the ESD circuits contained in the TLVx172 (indicated by the dashed box). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

Feature Description (continued)

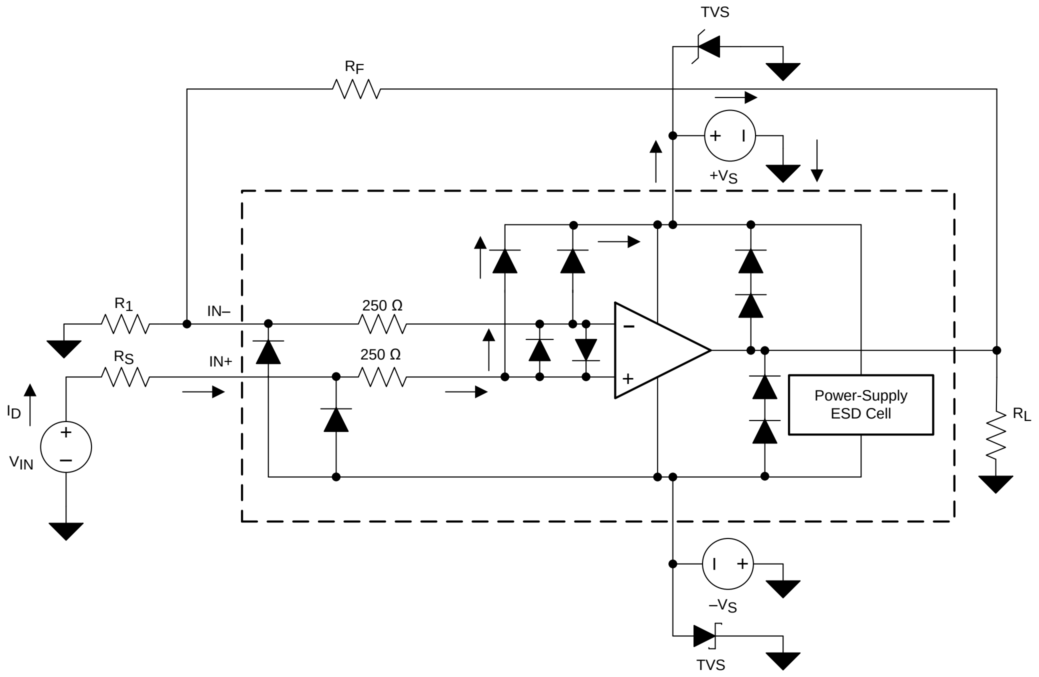


Figure 26. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the TLVx172 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit, as shown in Figure 26, the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

Figure 26 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage (V+) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, then one of the upper input steering diodes conducts and directs current to V+. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Feature Description (continued)

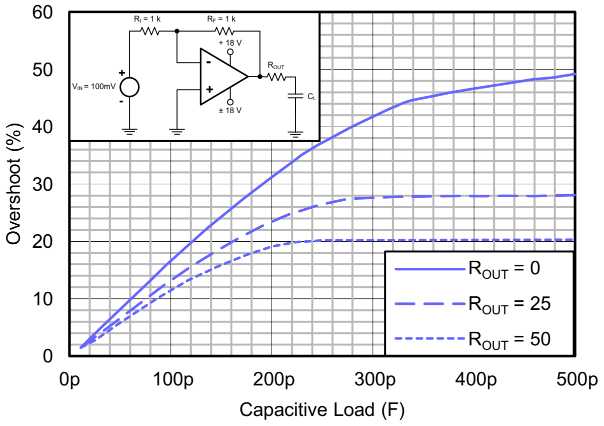
Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies (V+ or V–) are at 0 V. Again, this question depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see Figure 26. Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

The TLVx172 input pins are protected from excessive differential voltage with back-to-back diodes; see Figure 26. In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, then limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the input signal current. This input series resistor degrades the low-noise performance of the TLVx172. Figure 26 illustrates an example configuration that implements a current-limiting feedback resistor.

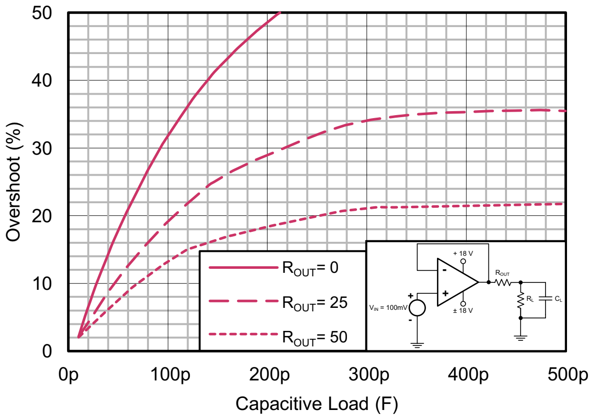
8.3.4 Capacitive Load and Stability

The dynamic characteristics of the TLVx172 are optimized for common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. Figure 27 and Figure 28 show graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}. Also, see the *Feedback Plots Define Op Amp AC Performance* application note for details of analysis techniques and application circuits.



100-mV output step, G = –1

Figure 27. Small-Signal Overshoot vs Capacitive Load



100-mV output step, G = +1

Figure 28. Small-Signal Overshoot vs Capacitive Load

8.4 Device Functional Modes

8.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the TLVx172 family extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in Table 2.

Table 2. Typical Performance for Common-Mode Voltages Within 2 V of the Positive Supply

PARAMETER	MIN	TYP	MAX	UNIT
Input common-mode voltage	(V+) – 2		(V+) + 0.1	V
Offset voltage		7		mV
Offset voltage vs temperature		12		µV/°C
Common-mode rejection		65		dB
Open-loop gain		60		dB
Gain-bandwidth product		0.3		MHz
Slew rate		0.3		V/µs

8.4.2 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from the saturated state to the linear state. The output devices of the operational amplifier enter the saturation region when the output voltage exceeds the rated operating voltage, either resulting from the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices need time to return back to the normal state. After the charge carriers return back to the equilibrium state, the device begins to slew at the normal slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLVx172 is approximately 2 µs.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLVx172 family of operational amplifiers provides high overall performance in a large number of general-purpose applications. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1-µF capacitors are adequate. Follow the additional recommendations in the *Layout Guidelines* section in order to achieve the maximum performance from this device. Many applications can introduce capacitive loading to the output of the amplifier (potentially causing instability). One method of stabilizing the amplifier in such applications is to add an isolation resistor between the amplifier output and the capacitive load. The design process for selecting this resistor is given in the *Typical Application* section.

9.2 Typical Application

This circuit can be used to drive capacitive loads (such as cable shields, reference buffers, MOSFET gates, and diodes). The circuit uses an isolation resistor (R_{ISO}) to stabilize the output of an operational amplifier. R_{ISO} modifies the open-loop gain of the system to ensure that the circuit has sufficient phase margin.

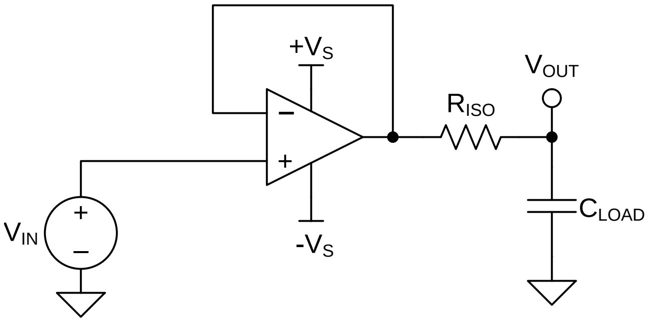


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Figure 29. Unity-Gain Buffer With R_{ISO} Stability Compensation

9.2.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (±15 V)
- Capacitive loads: 100 pF, 1000 pF, 0.01 µF, 0.1 µF, and 1 µF
- Phase margin: 45° and 60°

9.2.2 Detailed Design Procedure

Figure 29 shows a unity-gain buffer driving a capacitive load. Equation 1 shows the transfer function for the circuit in Figure 29. Not shown in Figure 29 is the open-loop output resistance of the operational amplifier, R_o.

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + \left(R_o + R_{ISO}\right) \times C_{LOAD} \times s} \tag{1}$$

The transfer function in Equation 1 has a pole and a zero. The frequency of the pole (f_p) is determined by (R_o + R_{ISO}) and C_{LOAD}. Components R_{ISO} and C_{LOAD} determine the frequency of the zero (f_z). A stable system is obtained by selecting R_{ISO} such that the rate of closure (ROC) between the open-loop gain (A_{OL}) and 1/β is 20 dB per decade. Figure 30 depicts the concept. The 1/β curve for a unity-gain buffer is 0 dB.

Typical Application (continued)

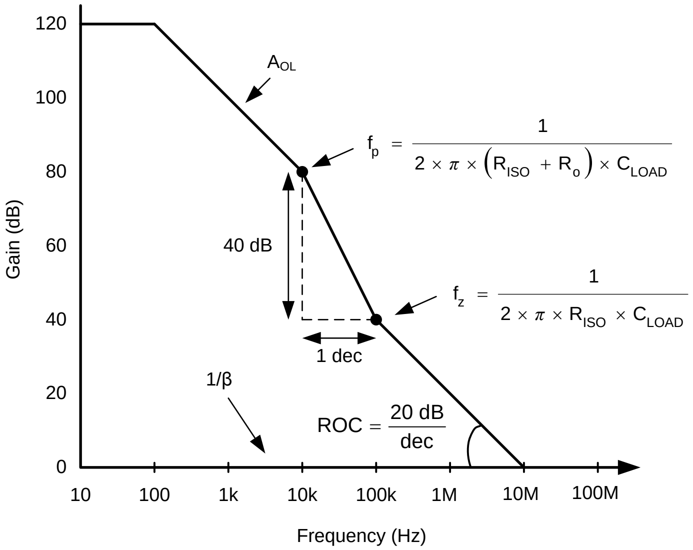

Figure 30. Unity-Gain Amplifier With R_{ISO} Compensation

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of R_o. In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and ac gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. Table 3 shows the overshoot percentage and ac gain peaking that correspond to phase margins of 45° and 60°. For more details on this design and other alternative devices that can be used in place of the TLV172, see the *Capacitive Load Drive Solution Using an Isolation Resistor* precision design.

Table 3. Phase Margin versus Overshoot and AC Gain Peaking

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

9.2.3 Application Curve

Using the described methodology, the values of R_{ISO} that yield phase margins of 45º and 60º for various capacitive loads were determined. The results are shown in Figure 31.

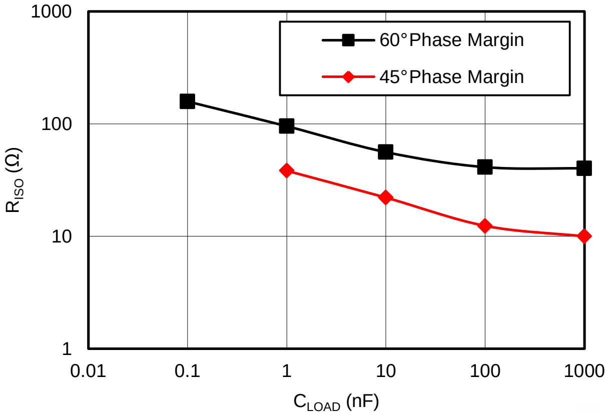

Figure 31. Isolation Resistor Required for Various Capacitive Loads to Achieve a Target Phase Margin

10 Power Supply Recommendations

The TLVx172 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 33, keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

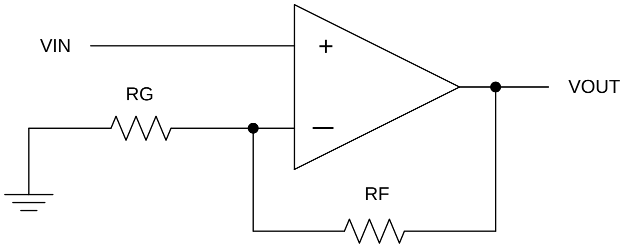

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Figure 32. Schematic Representation

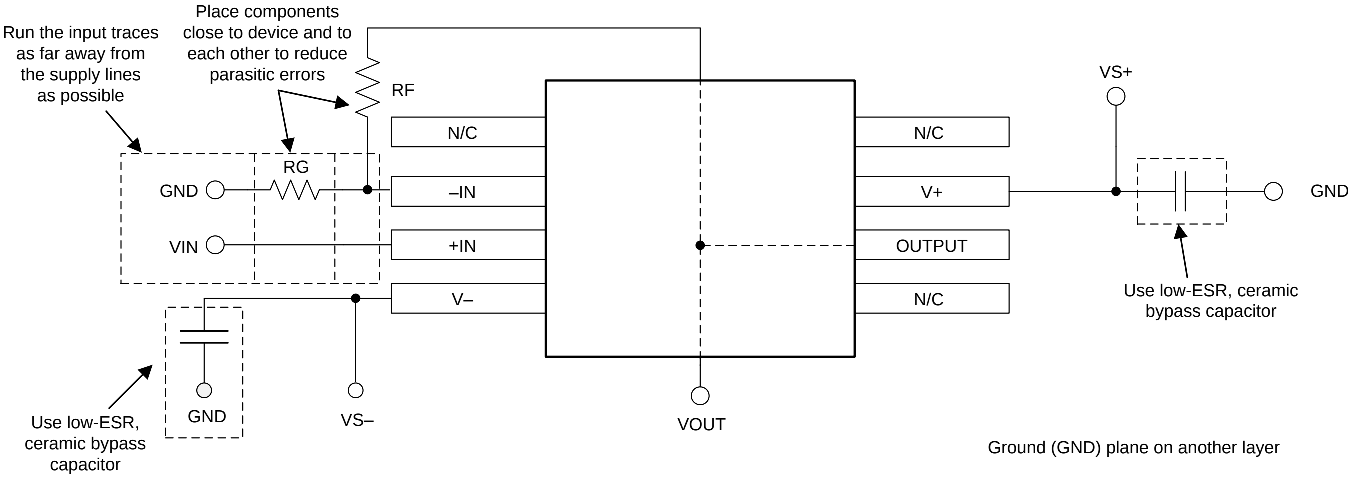

Figure 33. Operational Amplifier Board Layout for a Noninverting Configuration

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 TINA-TI™ (Free Software Download)

TINA-TI™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macromodels in addition to a range of both passive and active models. TINA-TI™ provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI™ offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, thus creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or the TINA-TI™ software be installed. Download the free TINA-TI™ software from the TINA-TI™ folder.

12.1.1.2 DIP Adapter EVM

The DIP Adapter EVM tool provides an easy, low-cost way to prototype small surface-mount devices. The evaluation tool uses these TI packages: D or U (SOIC-8), PW (TSSOP-8), DGK (VSSOP-8), DBV (SOT23-6, SOT23-5, and SOT23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6). The DIP adapter EVM can also be used with terminal strips or can be wired directly to existing circuits.

12.1.1.3 Universal Op Amp EVM

The Universal Op Amp EVM is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of device package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, VSSOP, TSSOP, and SOT23 packages are all supported.

NOTE

These boards are unpopulated, so users must provide their own devices. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

12.1.1.4 TI Precision Designs

TI precision designs are analog solutions created by TI’s precision analog applications experts and offer the theory of operation, component selection, simulation, a complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI precision designs are available online at www.ti.com/ww/en/analog/precision-designs/.

12.1.1.5 WEBENCH® Filter Designer

The WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH® filter designer allows optimized filter designs to be created by using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® design center, the WEBENCH® filter designer allows complete multistage active filter solutions to be designed, optimized, and simulated within minutes.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *Feedback Plots Define Op Amp AC Performance* (SBOA015)
- *EMI Rejection Ratio of Operational Amplifiers* Application Report (SBOA128)
- *Compensate Transimpedance Amplifiers Intuitively* Application Report (SBOA055)
- *Noise Analysis for High-Speed Op Amps* Application Report (SBOA066)

12.3 Related Links

Table 4 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV172	Click here	Click here	Click here	Click here	Click here
TLV2172	Click here	Click here	Click here	Click here	Click here
TLV4172	Click here	Click here	Click here	Click here	Click here

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 Trademarks

TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
DesignSoft is a trademark of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

12.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV172IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	18VV	Samples
TLV172IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	18VV	Samples
TLV172IDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	15W	Samples
TLV172IDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	15W	Samples
TLV172IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV172	Samples
TLV2172IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	14P6	Samples
TLV2172IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	14P6	Samples
TLV2172IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL2172	Samples
TLV4172IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	TLV4172	Samples
TLV4172IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV4172	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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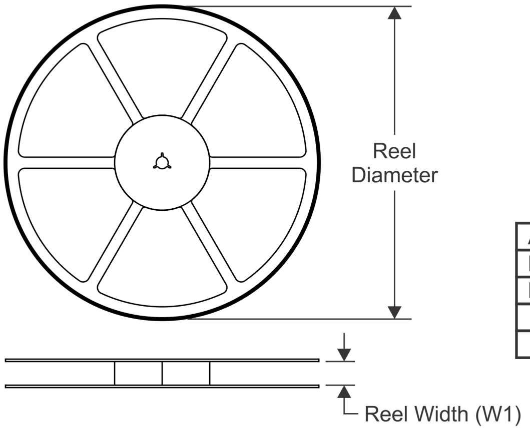
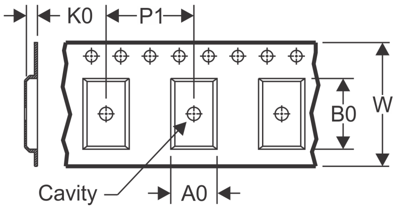
TAPE AND REEL INFORMATION

REEL DIMENSIONS

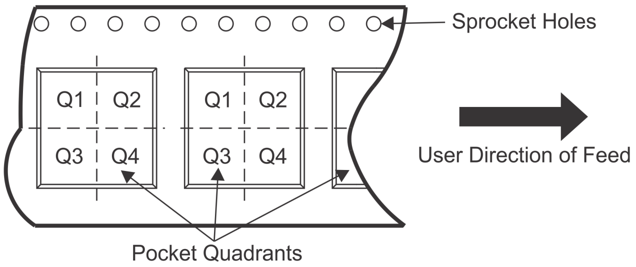


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

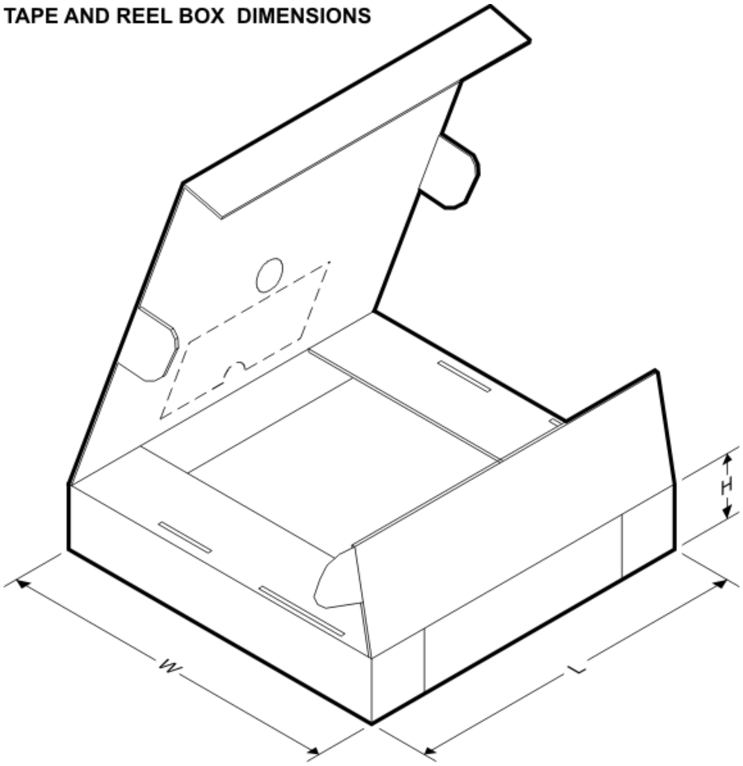
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV172IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV172IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV172IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV172IDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV172IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2172IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2172IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2172IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV4172IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV4172IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

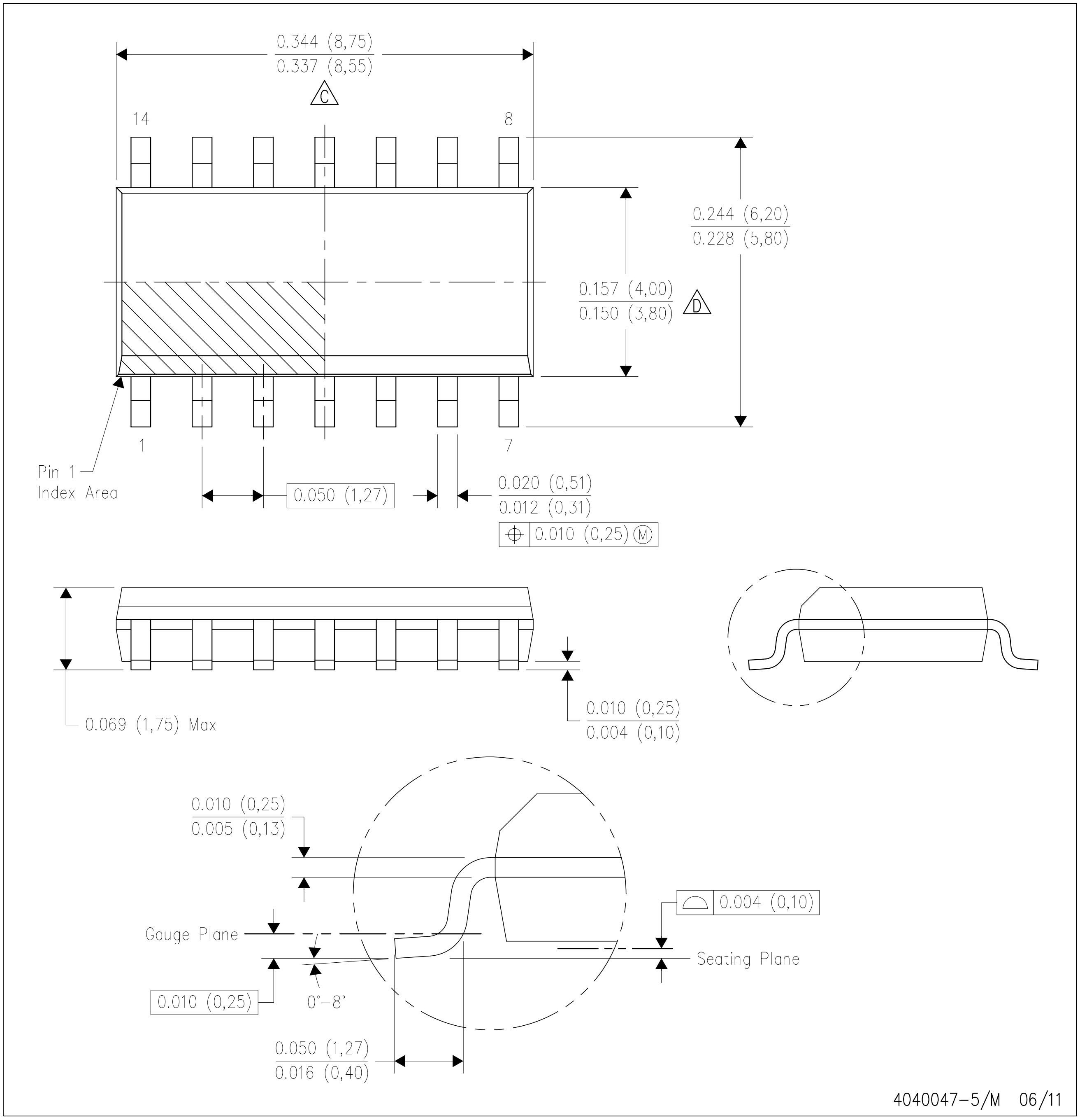
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

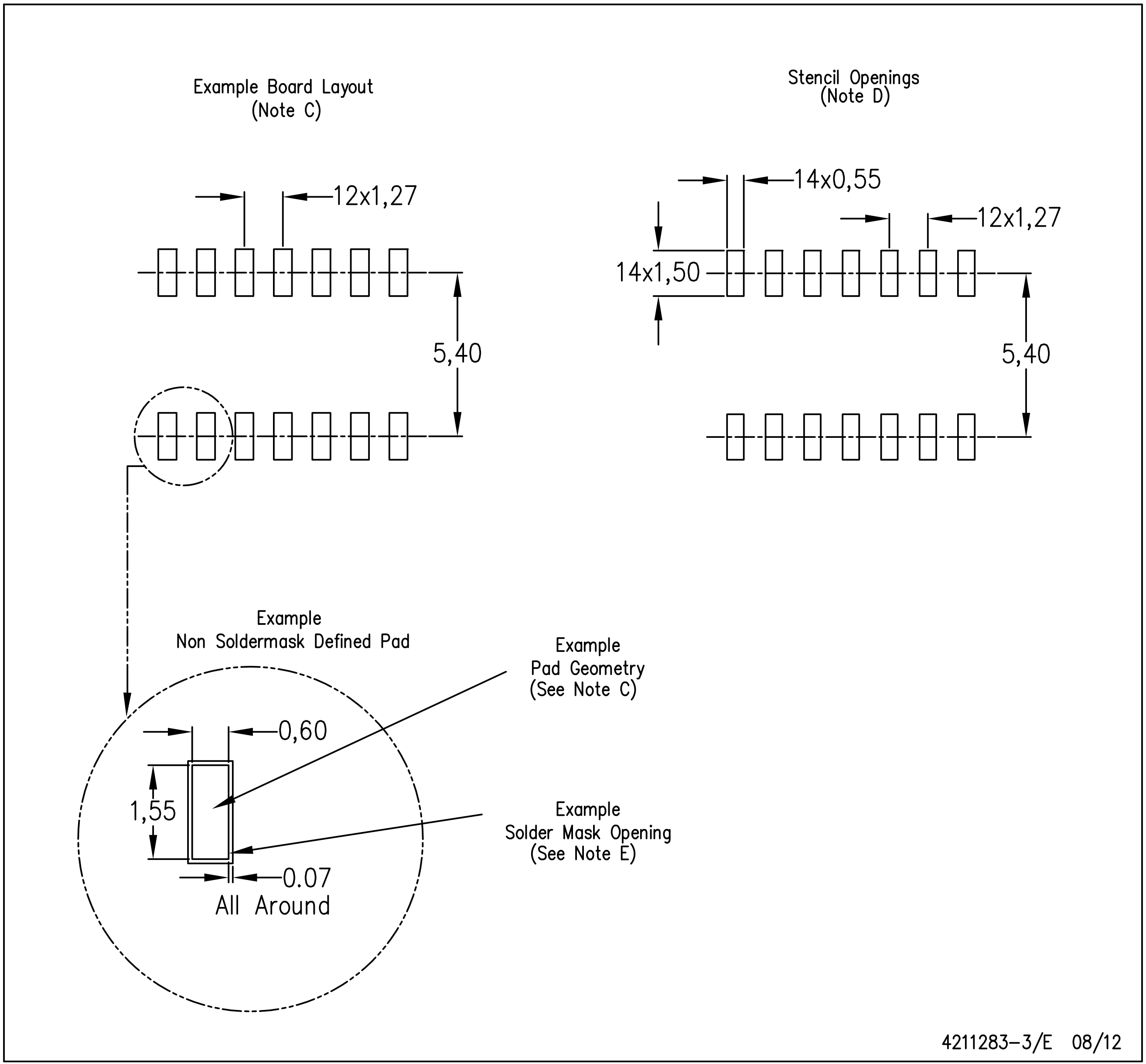
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV172IDBVR	SOT-23	DBV	5	3000	223.0	270.0	35.0
TLV172IDBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
TLV172IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TLV172IDCKT	SC70	DCK	5	250	180.0	180.0	18.0
TLV172IDR	SOIC	D	8	2500	367.0	367.0	35.0
TLV2172IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV2172IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
TLV2172IDR	SOIC	D	8	2500	367.0	367.0	35.0
TLV4172IDR	SOIC	D	14	2500	367.0	367.0	38.0
TLV4172IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



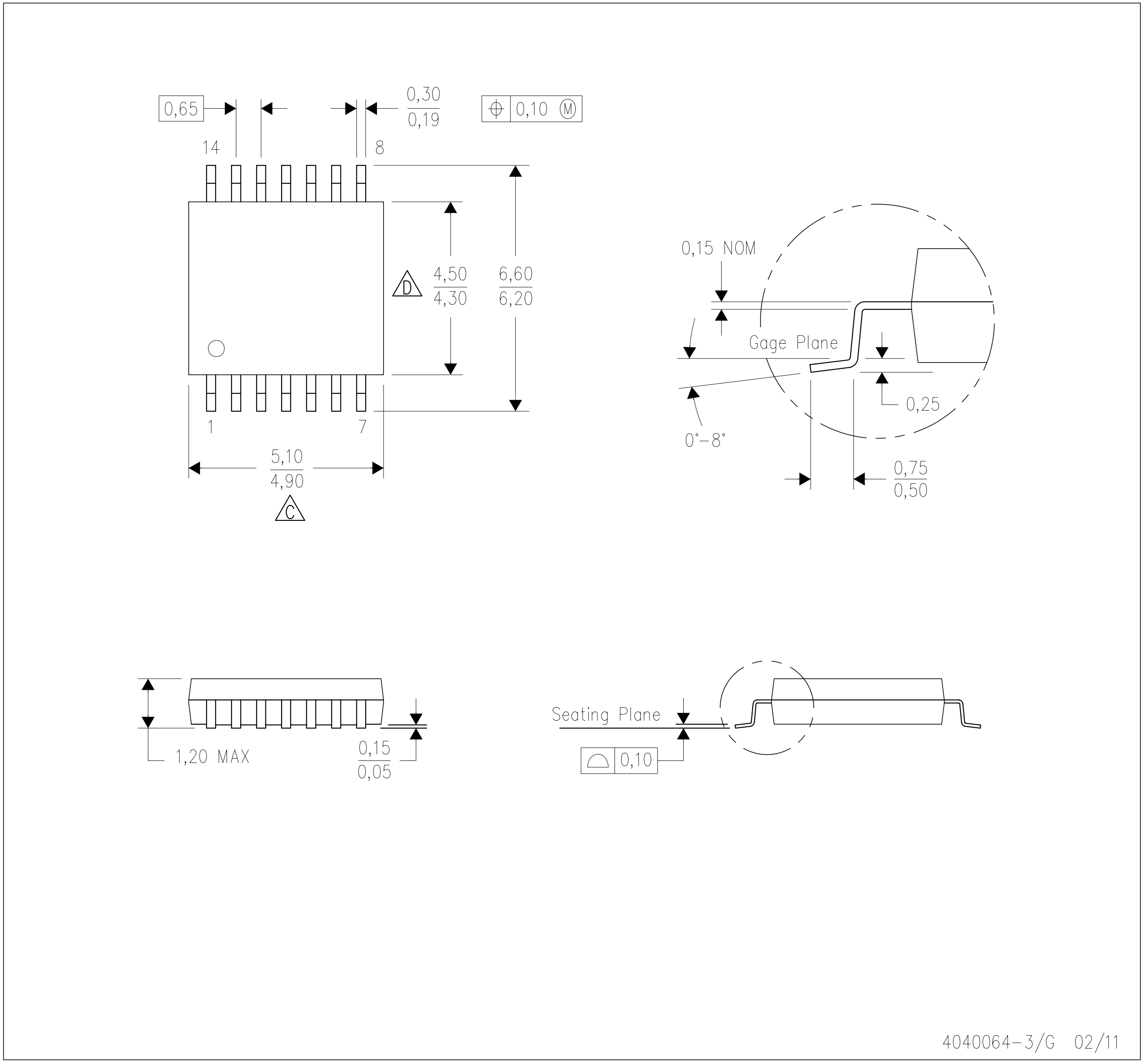
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



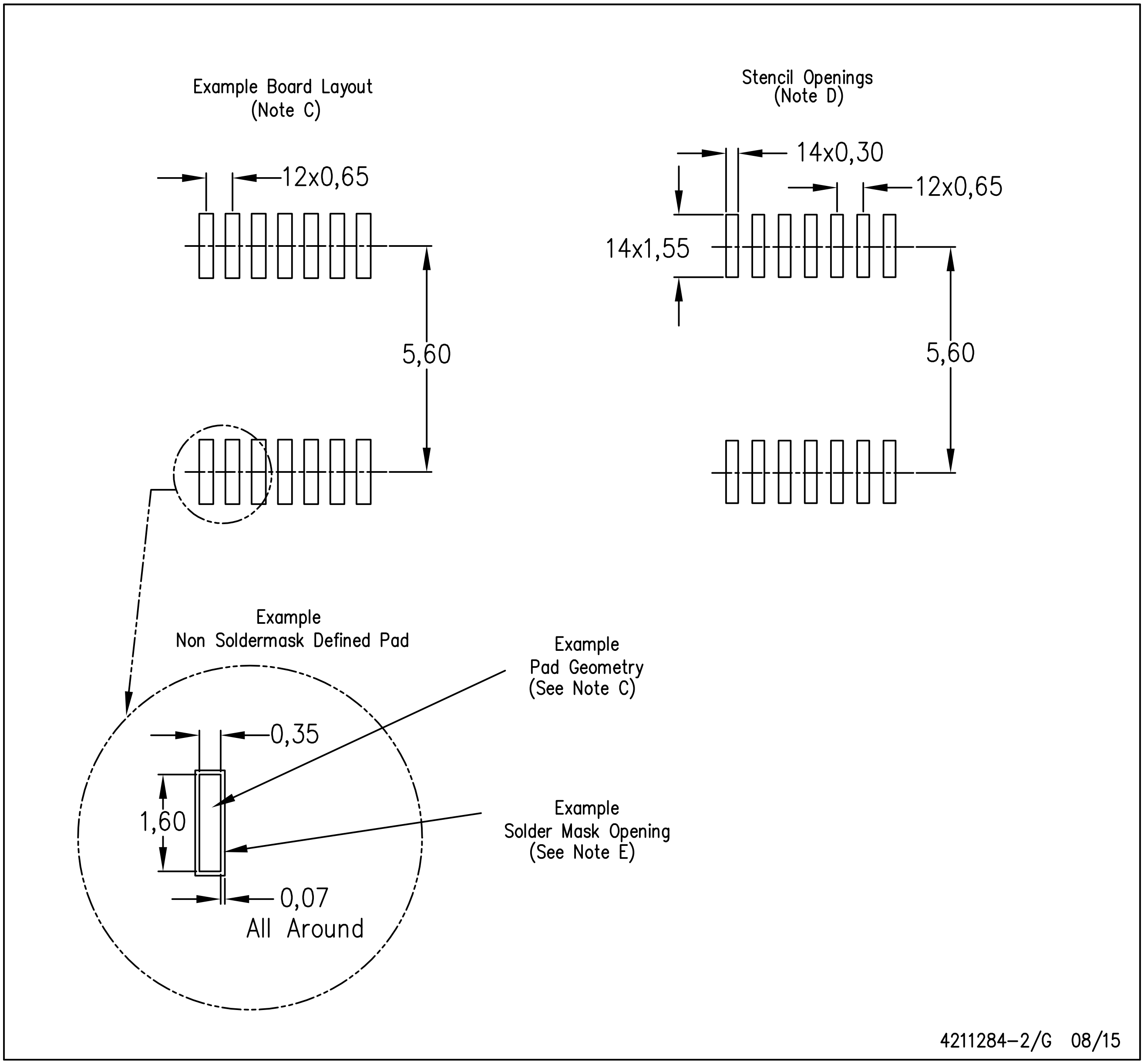
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



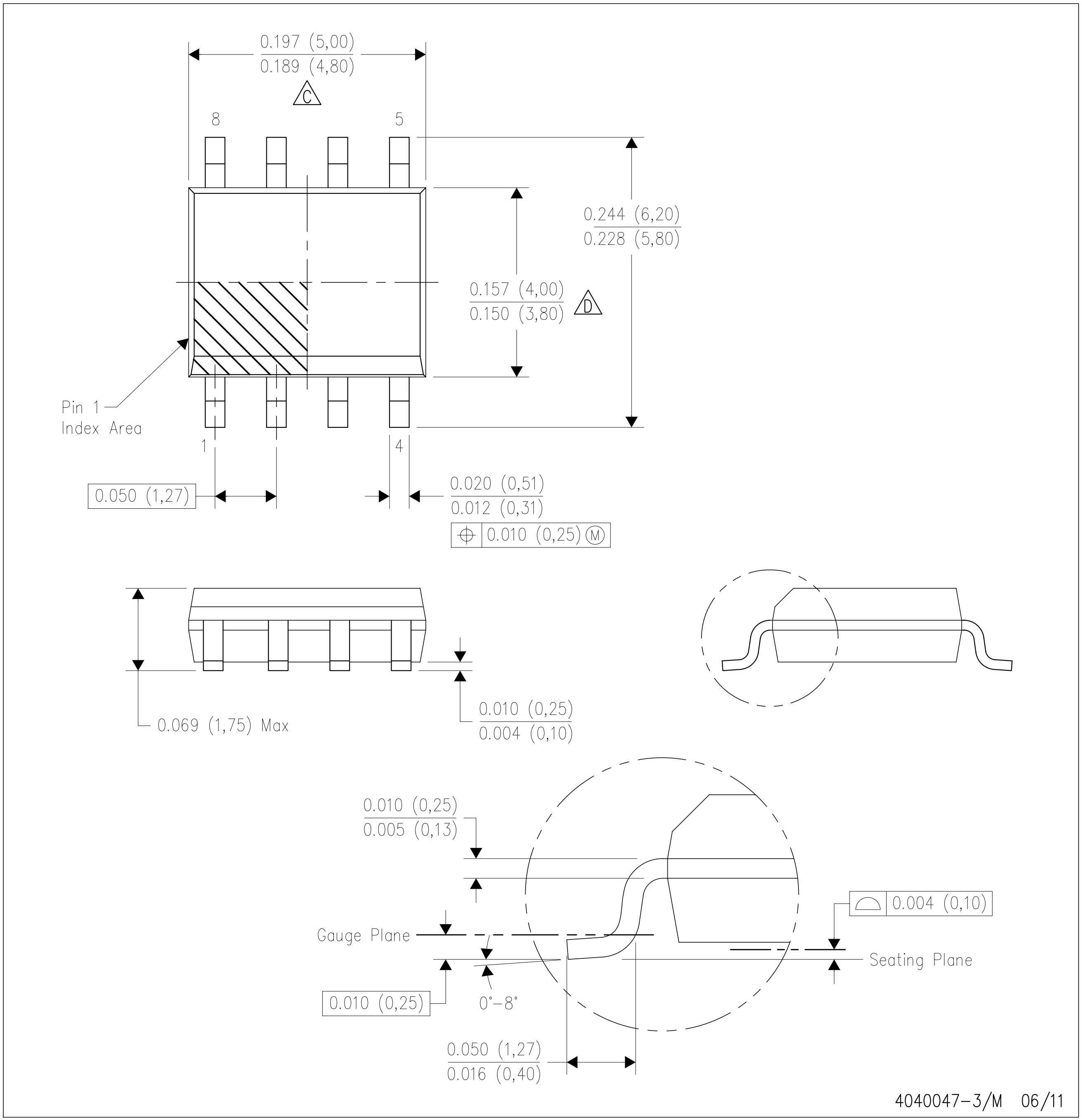
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



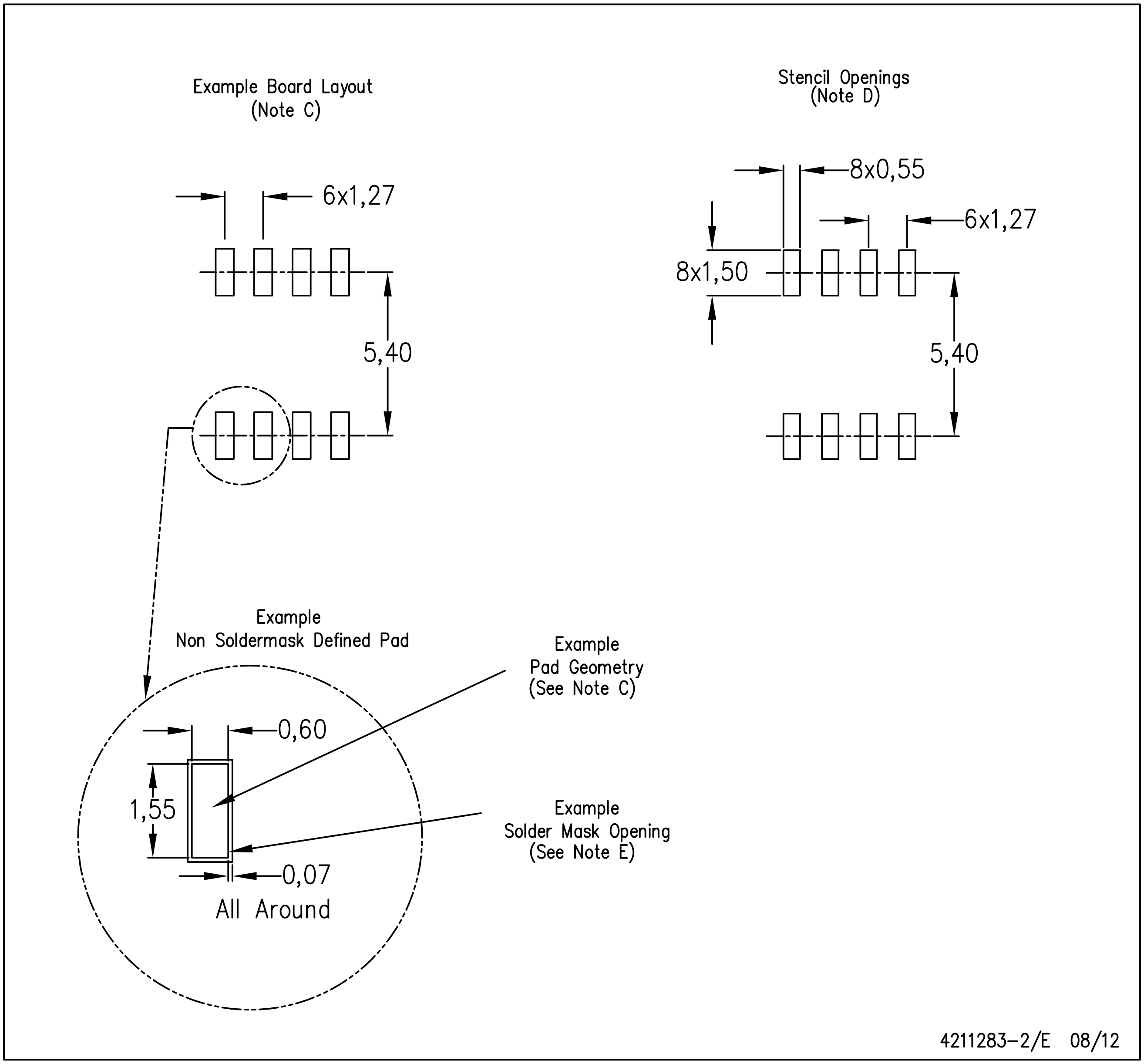
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



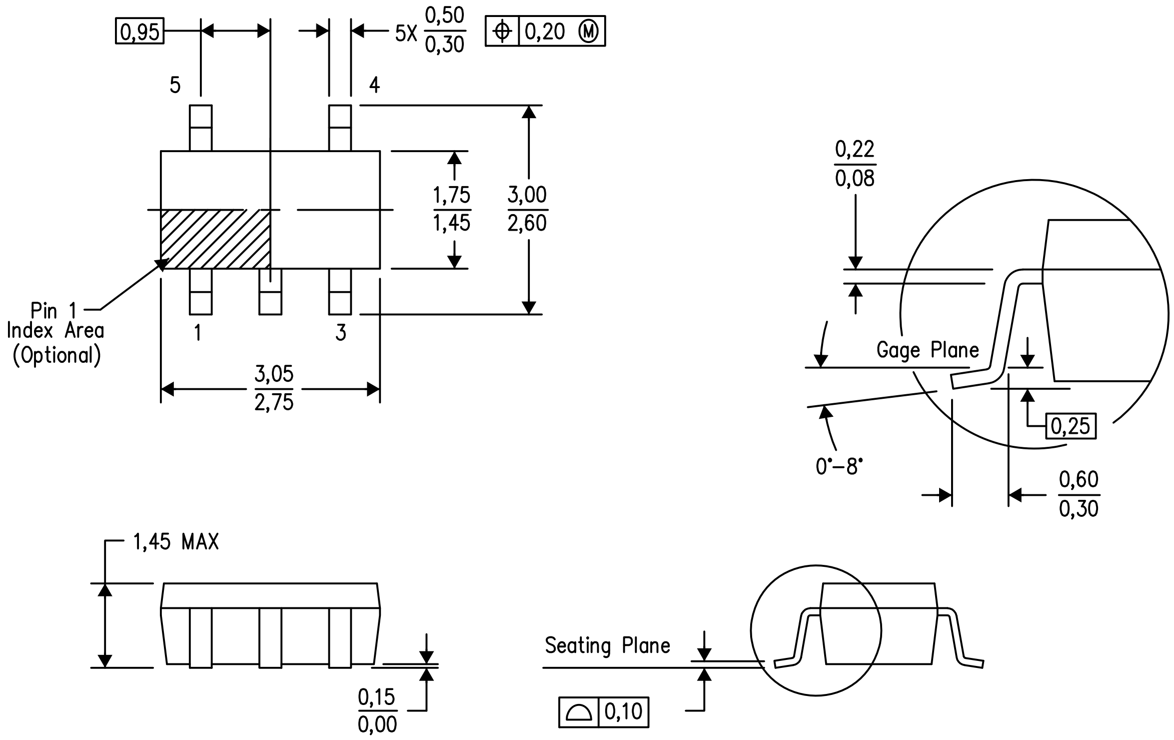
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



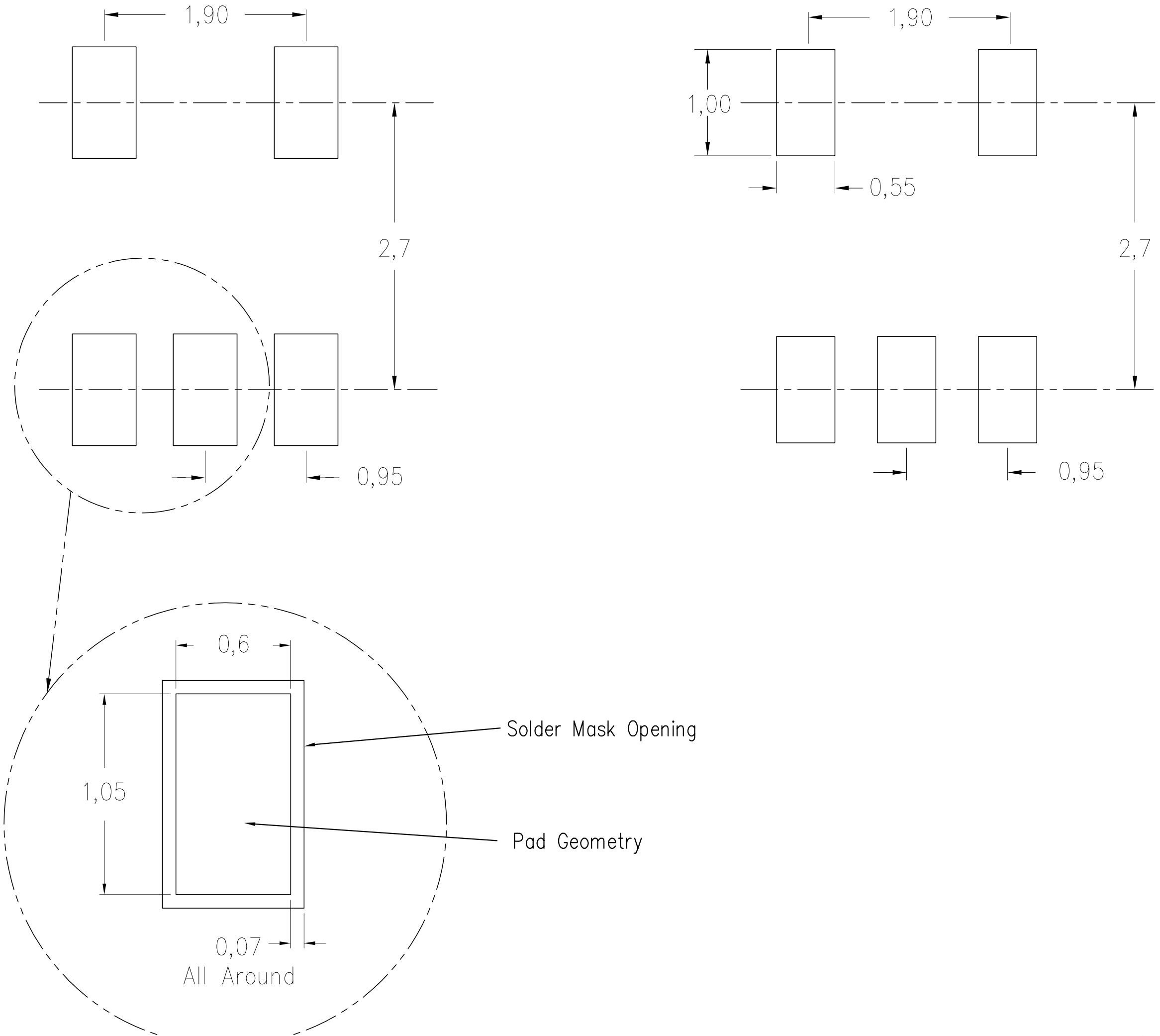
4073253–4/N 12/14

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO–178 Variation AA.

DBV (R-PDSO-G5) PLASTIC SMALL OUTLINE

Example Board Layout

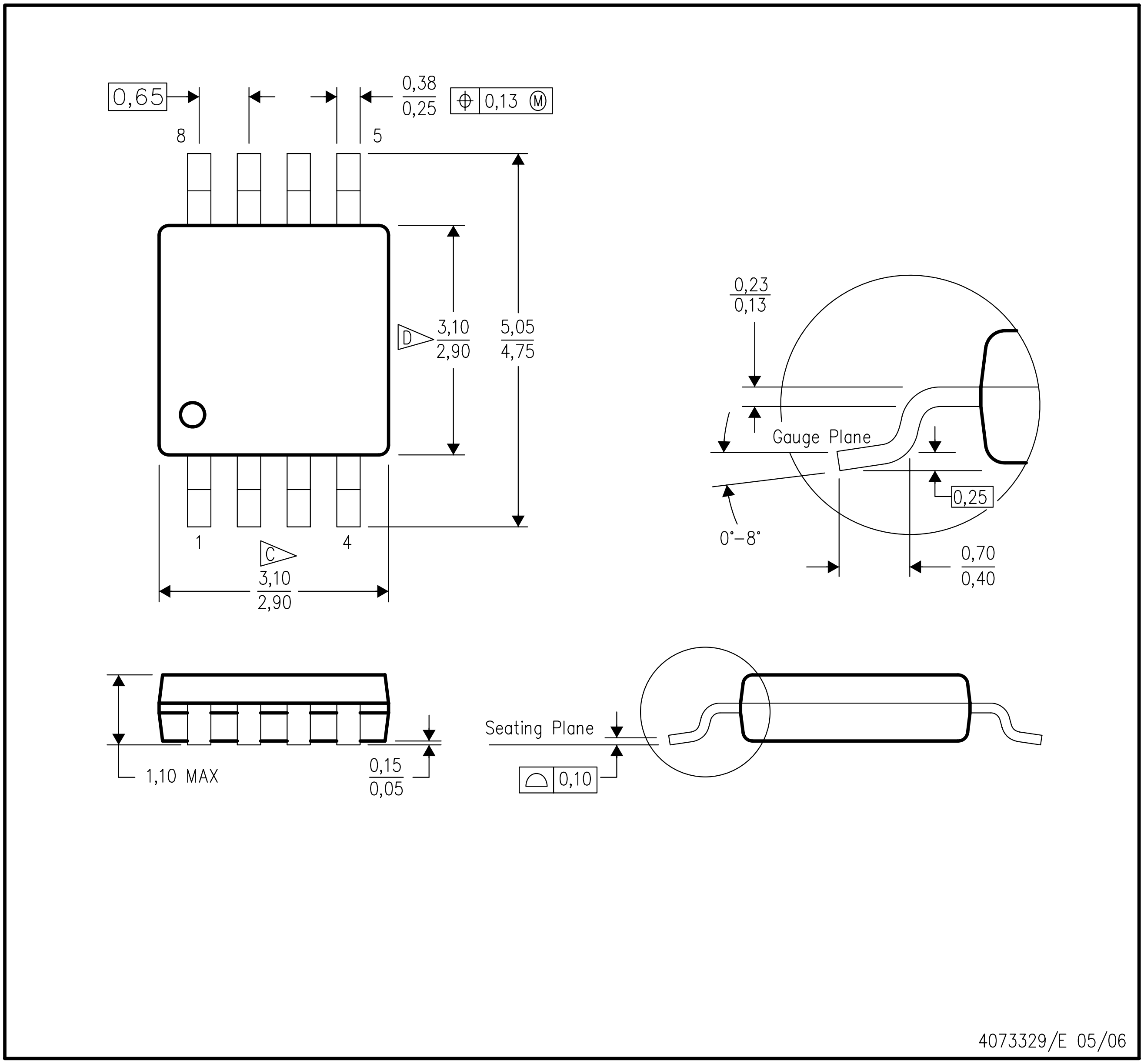
Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



4209593-3/C 08/11

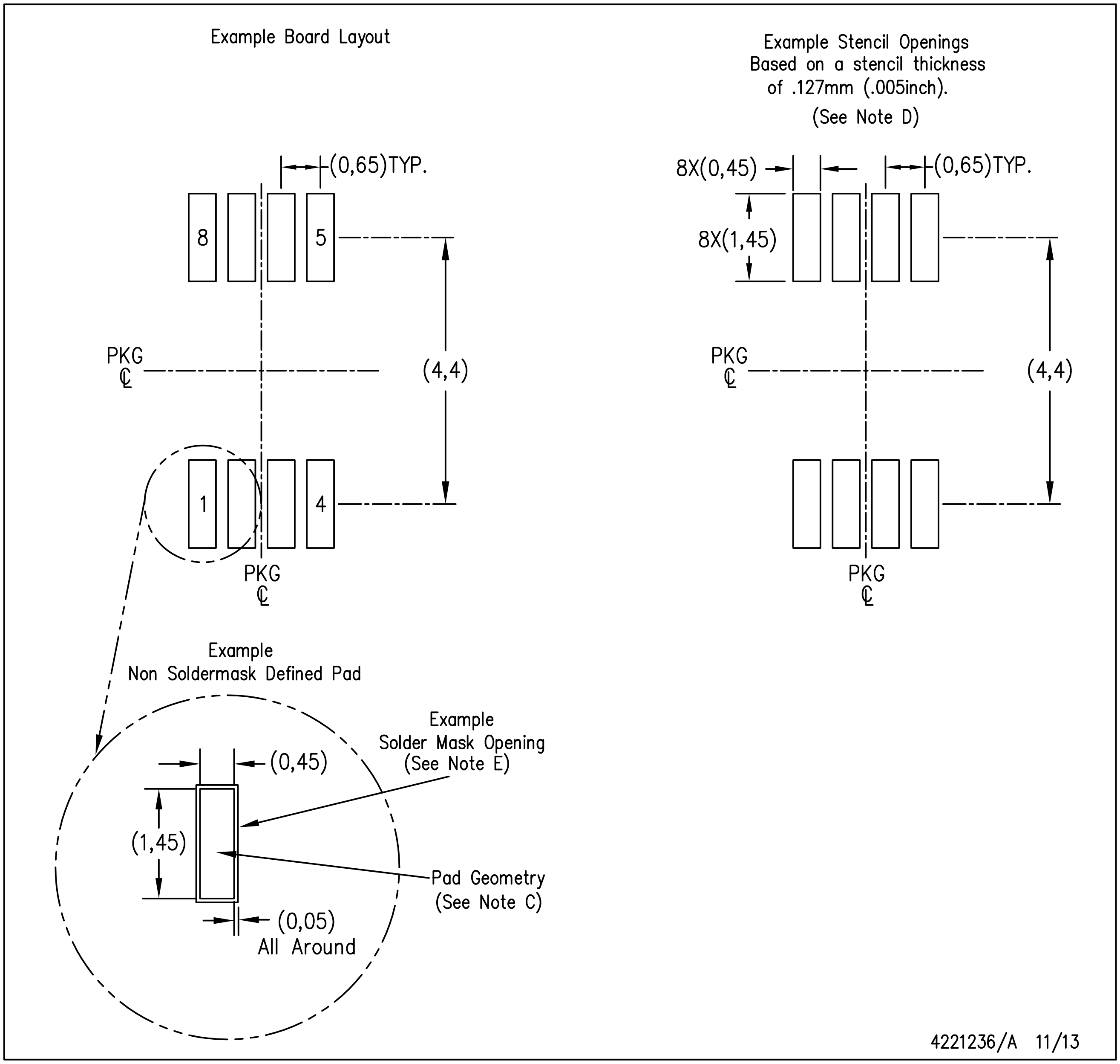
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



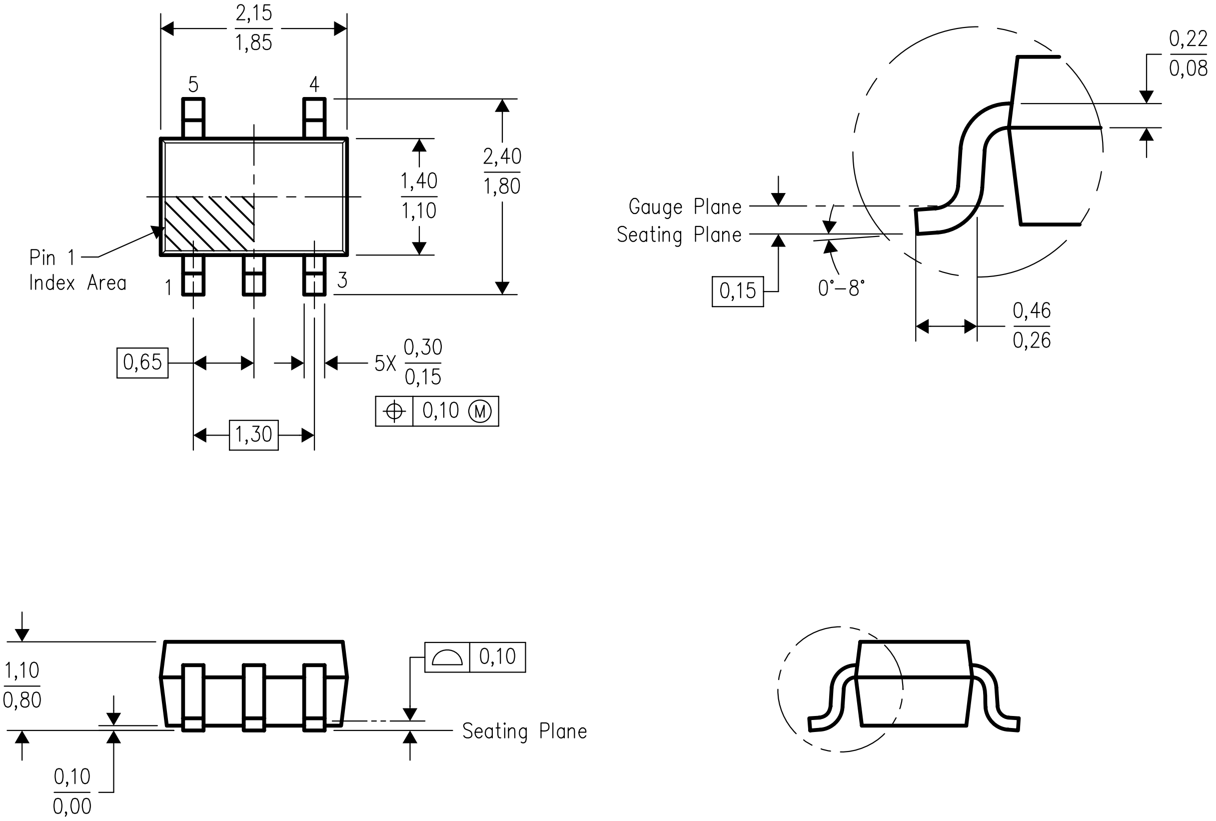
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

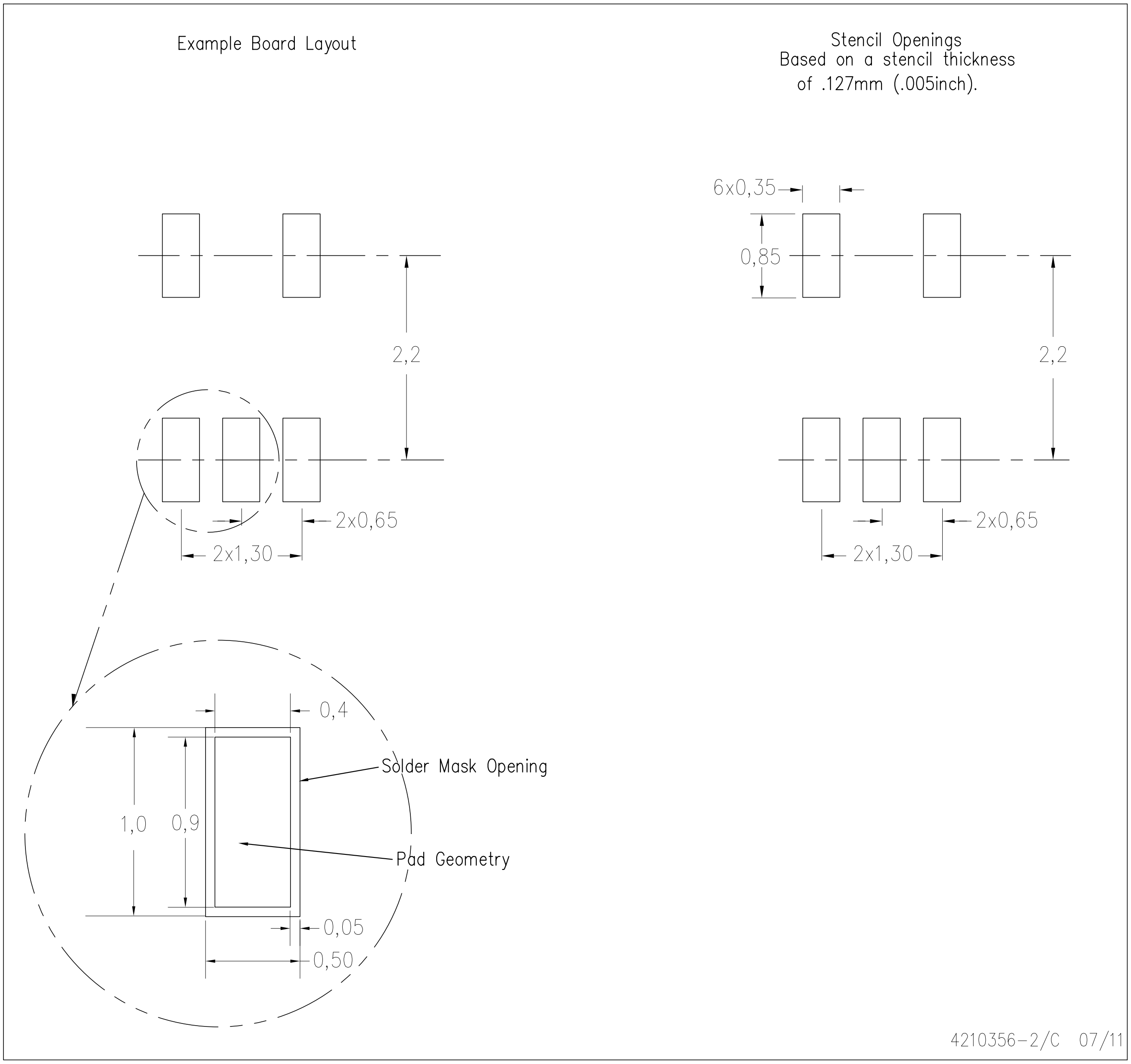
DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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