



## 4.5ns Rail-to-Rail, High-Speed Comparator in Microsize Packages

### FEATURES

- HIGH SPEED: 4.5ns
- RAIL-TO-RAIL I/O
- SUPPLY VOLTAGE: +2.7V to +5.5V
- PUSH-PULL CMOS OUTPUT STAGE
- SHUTDOWN (TLV3501 only)
- MICRO PACKAGES:  
SOT23-6 (single)  
SOT23-8 (dual)
- LOW SUPPLY CURRENT: 3.2mA

### APPLICATIONS

- AUTOMATIC TEST EQUIPMENT
- WIRELESS BASE STATIONS
- THRESHOLD DETECTOR
- ZERO-CROSSING DETECTOR
- WINDOW COMPARATOR

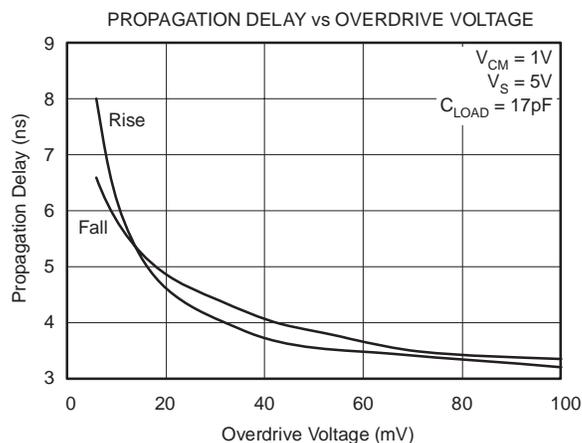
### TLV350x RELATED PRODUCTS

FEATURES	PRODUCT
Precision Ultra-Fast, Low-Power Comparator	TLC3016
Differential Output Comparator	TL712
High-Speed Op Amp, 16-Bit Accurate, 150MHz	OPA300
High-Speed Op Amp, Rail-to-Rail, 38MHz	OPA350
High-Speed Op Amp with Shutdown, 250MHz	OPA357

### DESCRIPTION

The TLV350x family of push-pull output comparators feature a fast 4.5ns propagation delay and operation from +2.7V to +5.5V. Beyond-the-rails input common-mode range makes it an ideal choice for low-voltage applications. The rail-to-rail output directly drives either CMOS or TTL logic.

Microsize packages provide options for portable and space-restricted applications. The single (TLV3501) is available in SOT23-6 and SO-8 packages. The dual (TLV3502) comes in the SOT23-8 and SO-8 packages.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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## ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	+5.5V
Signal Input Terminals, Voltage(2)	(V-) - 0.3V to (V+) + 0.3V
Signal Input Terminals, Current(2)	10mA
Output Short Circuit(3)	74mA
Operating Temperature	-40°C to +125°C
Storage Temperature	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
ESD Rating (Human Body Model)	3000V
Charged-Device Model (CDM)	500V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current limited to 10mA or less.
- (3) Short-circuit to ground, one comparator per package.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

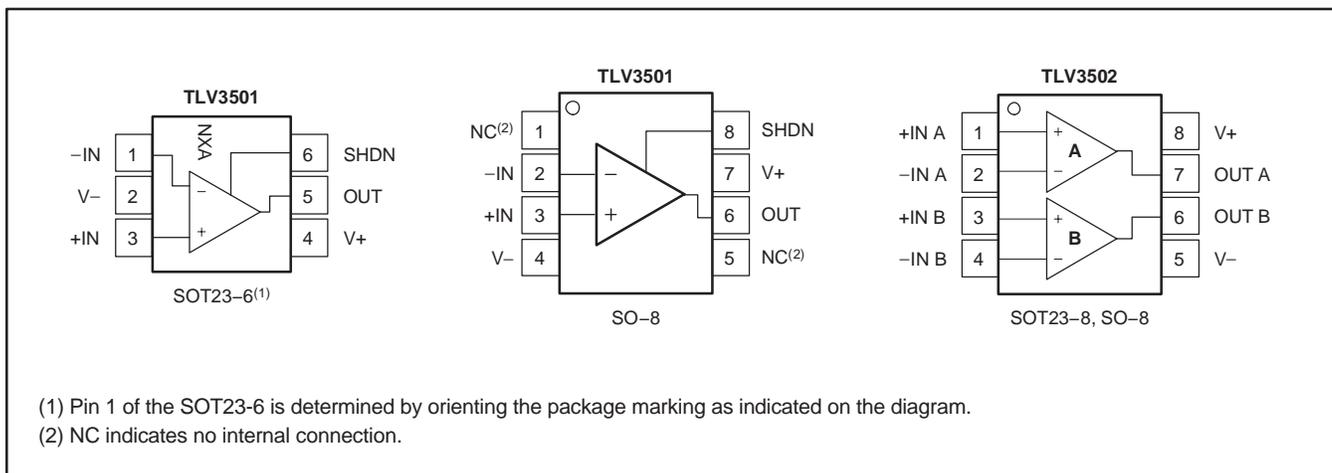
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
TLV3501	SOT23-6	DBV	NXA
TLV3501	SO-8	D	TLV3501A
TLV3502	SOT23-8	DCN	NXC
TLV3502	SO-8	D	TLV3502A

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

## PIN CONFIGURATIONS



## ELECTRICAL CHARACTERISTICS

**Boldface** limits apply over the specified temperature range,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

At  $T_A = +25^\circ\text{C}$  and  $V_S = +2.7\text{V}$  to  $+5.5\text{V}$ , unless otherwise noted.

PARAMETER	CONDITION	TLV3501, TLV3502			UNITS
		MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b>					
Input Offset Voltage <sup>(1)</sup>	$V_{OS}$	$V_{CM} = 0\text{V}, I_O = 0\text{mA}$	$\pm 1$	$\pm 6.5$	mV
<b>vs Temperature</b>	$dV_{OS}/dT$	<b><math>T_A = -40^\circ\text{C}</math> to <math>+125^\circ\text{C}</math></b>	$\pm 5$		$\mu\text{V}/^\circ\text{C}$
<b>vs Power Supply</b>	PSRR	$V_S = 2.7\text{V}$ to $5.5\text{V}$	100	400	$\mu\text{V}/\text{V}$
Input Hysteresis			6		mV
<b>INPUT BIAS CURRENT</b>					
Input Bias Current	$I_B$	$V_{CM} = V_{CC}/2$	$\pm 2$	$\pm 10$	pA
Input Offset Current <sup>(2)</sup>	$I_{OS}$	$V_{CM} = V_{CC}/2$	$\pm 2$	$\pm 10$	pA
<b>INPUT VOLTAGE RANGE</b>					
Common-Mode Voltage Range	$V_{CM}$		$(V-) - 0.2\text{V}$		V
Common-Mode Rejection	CMRR	$V_{CM} = -0.2\text{V}$ to $(V+) + 0.2\text{V}$	57	70	dB
		<b><math>V_{CM} = -0.2\text{V}</math> to <math>(V+) + 0.2\text{V}</math></b>	<b>55</b>		<b>dB</b>
<b>INPUT IMPEDANCE</b>					
Common-Mode			$10^{13} \parallel 2$		$\Omega \parallel \text{pF}$
Differential			$10^{13} \parallel 4$		$\Omega \parallel \text{pF}$
<b>SWITCHING CHARACTERISTICS</b>					
Propagation Delay Time <sup>(3)</sup>	$T_{(pd)}$	$\Delta V_{IN} = 100\text{mV}$ , Overdrive = $20\text{mV}$	4.5	6.4	ns
		<b><math>\Delta V_{IN} = 100\text{mV}</math>, Overdrive = <math>20\text{mV}</math></b>		<b>7</b>	<b>ns</b>
		$\Delta V_{IN} = 100\text{mV}$ , Overdrive = $5\text{mV}$	7.5	10	ns
		<b><math>\Delta V_{IN} = 100\text{mV}</math>, Overdrive = <math>5\text{mV}</math></b>		<b>12</b>	<b>ns</b>
Propagation Delay Skew <sup>(4)</sup>	$\Delta t_{(SKEW)}$	$\Delta V_{IN} = 100\text{mV}$ , Overdrive = $20\text{mV}$	0.5		ns
Maximum Toggle Frequency	$f_{MAX}$	Overdrive = $50\text{mV}$ , $V_S = 5\text{V}$	80		MHz
Rise Time <sup>(5)</sup>	$t_R$		1.5		ns
Fall Time <sup>(5)</sup>	$t_F$		1.5		ns
<b>OUTPUT</b>					
Voltage Output from Rail	$V_{OH}, V_{OL}$	$I_{OUT} = \pm 1\text{mA}$	30	50	mV
<b>SHUTDOWN</b>					
$t_{OFF}$			30		ns
$t_{ON}$			100		ns
$V_L$ (comparator is enabled) <sup>(6)</sup>				$(V+) - 1.7\text{V}$	V
$V_H$ (comparator is disabled) <sup>(6)</sup>		$(V+) - 0.9\text{V}$			V
Input Bias Current of Shutdown Pin			2		pA
$I_{QSD}$ (quiescent current in shutdown)			2		$\mu\text{A}$
<b>POWER SUPPLY</b>					
Specified Voltage	$V_S$		+2.7	+5.5	V
Operating Voltage Range				2.2 to 5.5	V
Quiescent Current	$I_Q$	$V_S = 5\text{V}, V_O = \text{High}$	3.2	5	mA
<b>TEMPERATURE RANGE</b>					
Specified Range			-40	+125	$^\circ\text{C}$
Operating Range			-40	+125	$^\circ\text{C}$
Storage Range			-65	+150	$^\circ\text{C}$
Thermal Resistance	$\theta_{JA}$				
SOT23-5			200		$^\circ\text{C}/\text{W}$
SOT23-8			200		$^\circ\text{C}/\text{W}$
SO-8			150		$^\circ\text{C}/\text{W}$

(1)  $V_{OS}$  is defined as the average of the positive and the negative switching thresholds.

(2) The difference between  $I_{B+}$  and  $I_{B-}$ .

(3) Propagation delay cannot be accurately measured with low overdrive on automatic test equipment. This parameter is ensured by characterization and testing at  $100\text{mV}$  overdrive.

(4) The difference between the propagation delay going high and the propagation delay going low.

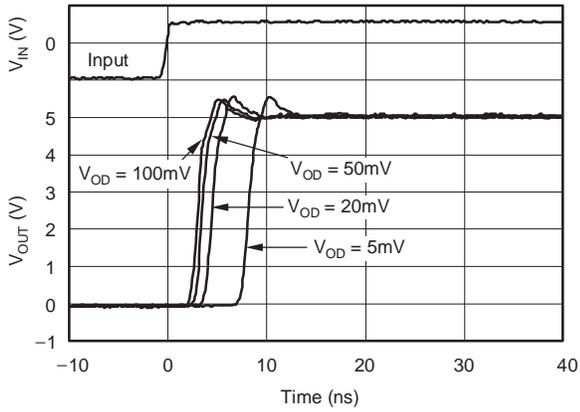
(5) Measured between 10% of  $V_S$  and 90% of  $V_S$ .

(6) When the shutdown pin is within  $0.9\text{V}$  of the most positive supply, the part is disabled. When it is more than  $1.7\text{V}$  below the most positive supply, the part is enabled.

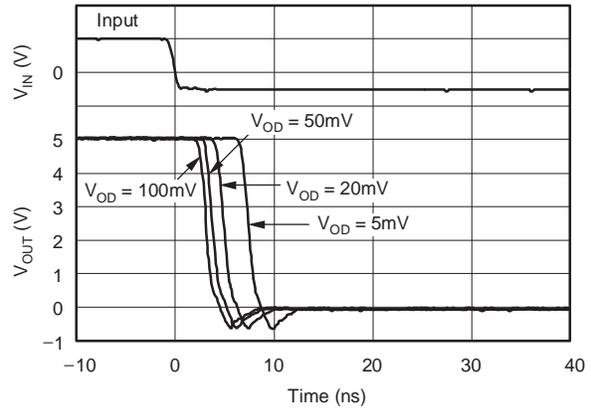
**TYPICAL CHARACTERISTICS**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +5\text{V}$ , and Input Overdrive = 100mV, unless otherwise noted.

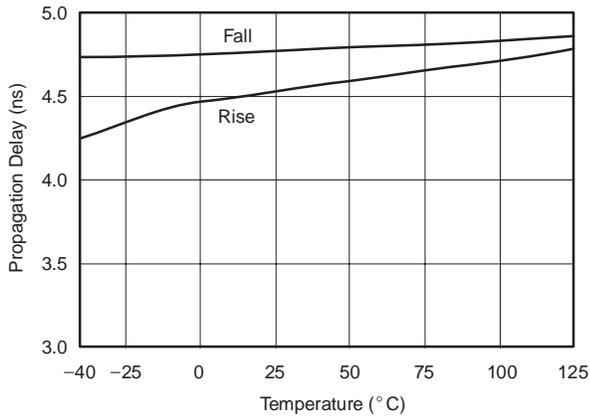
OUTPUT RESPONSE FOR VARIOUS OVERDRIVE VOLTAGES (rising)



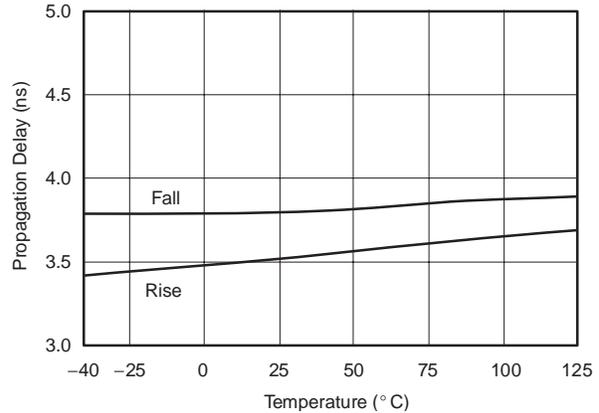
OUTPUT RESPONSE FOR VARIOUS OVERDRIVE VOLTAGES (falling)



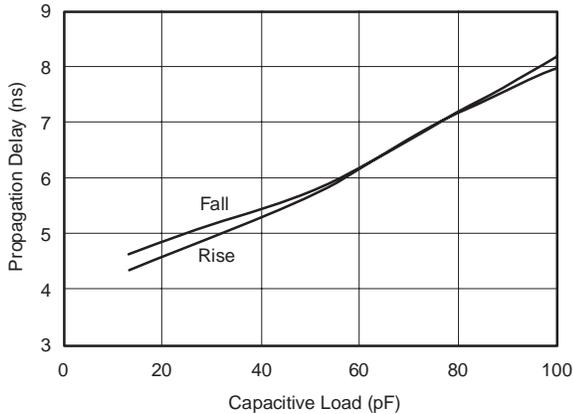
PROPAGATION DELAY vs TEMPERATURE ( $V_{OD} = 20\text{mV}$ )



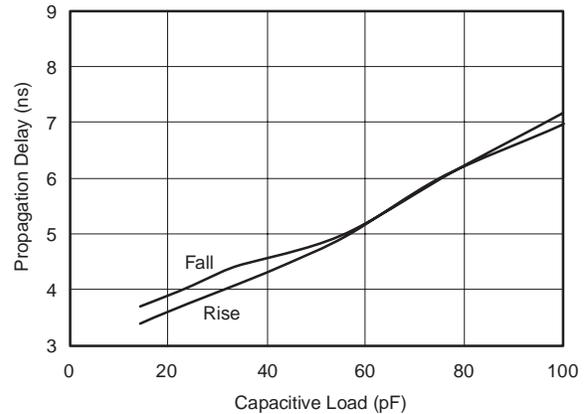
PROPAGATION DELAY vs TEMPERATURE ( $V_{OD} = 50\text{mV}$ )



PROPAGATION DELAY vs CAPACITIVE LOAD ( $V_{OD} = 20\text{mV}$ )

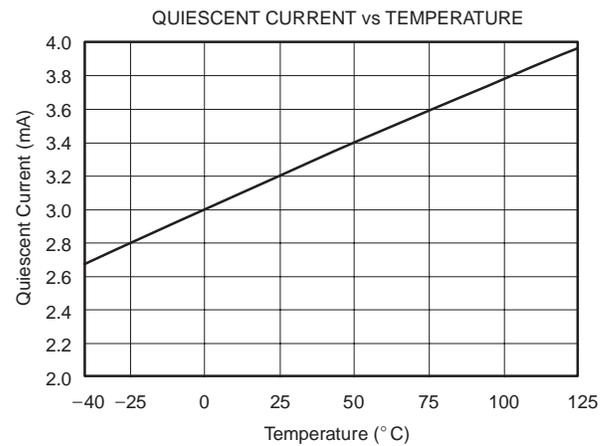
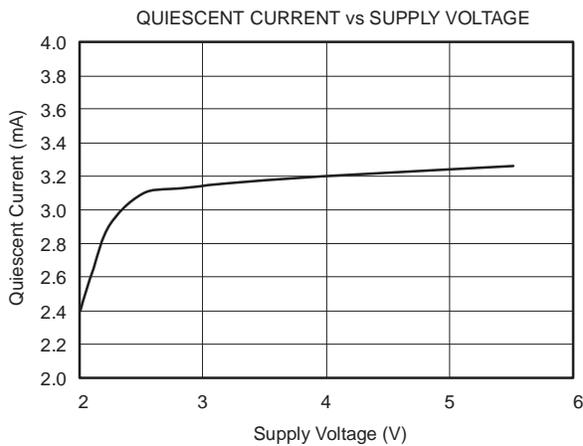
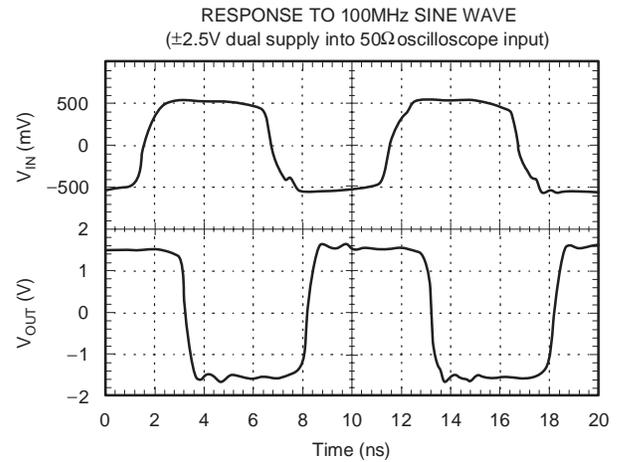
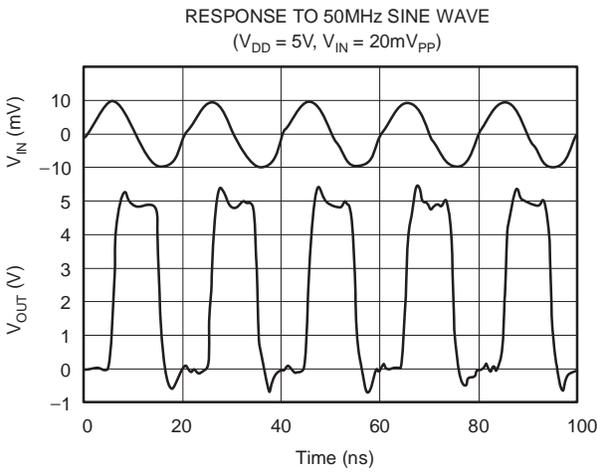
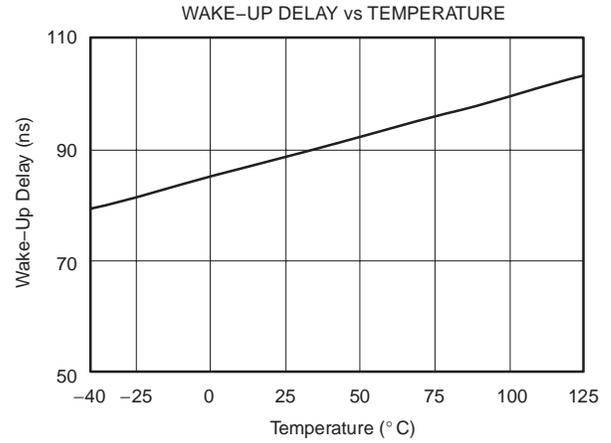
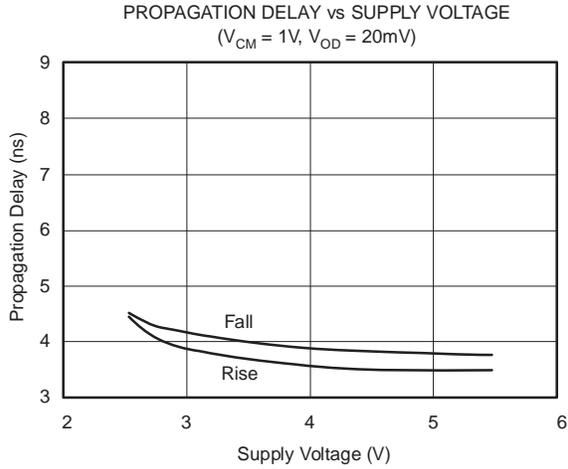


PROPAGATION DELAY vs CAPACITIVE LOAD ( $V_{OD} = 50\text{mV}$ )



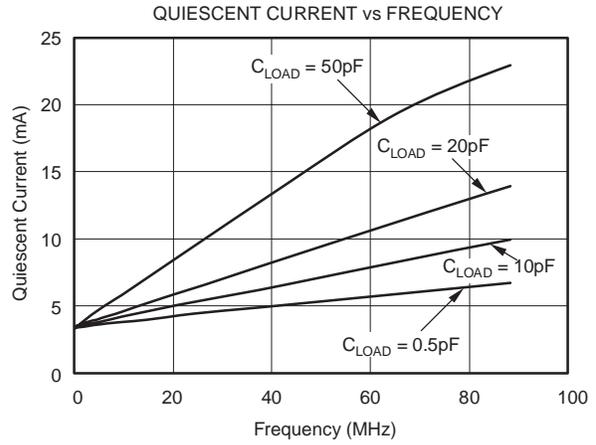
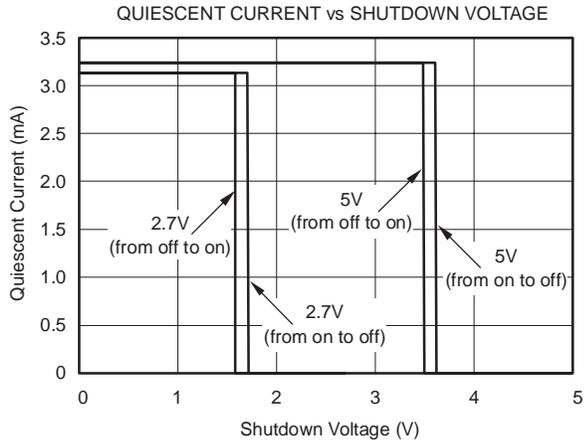
**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +5\text{V}$ , and Input Overdrive = 100mV, unless otherwise noted.



**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +5\text{V}$ , and Input Overdrive = 100mV, unless otherwise noted.



## APPLICATIONS INFORMATION

The TLV3501 and TLV3502 both feature high-speed response and includes 6mV of internal hysteresis for improved noise immunity with an input common-mode range that extends 0.2V beyond the power-supply rails.

### SHUTDOWN

A shutdown pin allows the device to go into idle when it is not in use. When the shutdown pin is high, the device draws about 2μA and the output goes to high impedance. When the shutdown pin is low, the TLV3501 is active. When the TLV3501 shutdown feature is not used, simply connect the shutdown pin to the most negative supply, as shown in Figure 1. It takes about 100ns to come out of shutdown mode. The TLV3502 does not have the shutdown feature.

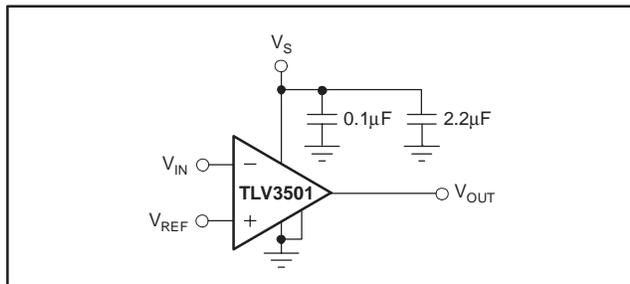


Figure 1. Basic Connections for the TLV3501

### OPERATING VOLTAGE

TLV3501 comparators are specified for use on a single supply from +2.7V to +5.5V (or a dual supply from ±1.35V to ±2.75V) over a temperature range of -40°C to +125°C. The device continues to function below this range, but performance is not specified.

### ADDING EXTERNAL HYSTERESIS

The TLV350x has a robust performance when used with a good layout. However, comparator inputs have little noise immunity within the range of specified offset voltage (±5mV). For slow moving or noisy input signals, the comparator output may display multiple switching as input signals move through the switching threshold. In such applications, the 6mV of internal hysteresis of the TLV350x might not be sufficient. In cases where greater noise immunity is desired, external hysteresis may be added by connecting a small amount of feedback to the positive

input. Figure 2 shows a typical topology used to introduce 25mV of additional hysteresis, for a total of 31mV hysteresis when operating from a single 5V supply. Total hysteresis is approximated by Equation 1:

$$V_{\text{HYST}} = \frac{(V_+) \times R_1}{R_1 + R_2} + 6\text{mV} \quad (1)$$

$V_{\text{HYST}}$  sets the value of the transition voltage required to switch the comparator output by enlarging the threshold region, thereby reducing sensitivity to noise.

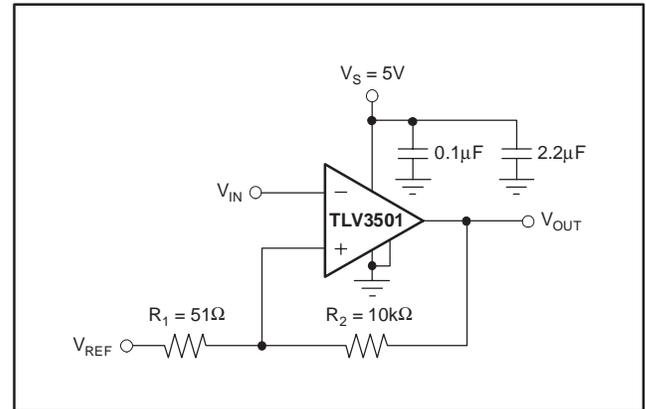


Figure 2. Adding Hysteresis to the TLV350x

### INPUT OVER-VOLTAGE PROTECTION

Device inputs are protected by ESD diodes that will conduct if the input voltages exceed the power supplies by more than approximately 300mV. Momentary voltages greater than 300mV beyond the power supply can be tolerated if the input current is limited to 10mA. This limiting is easily accomplished with a small input resistor in series with the comparator, as shown in Figure 3.

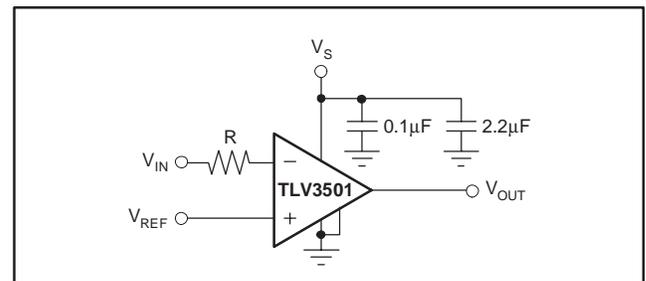


Figure 3. Input Current Protection for Voltages Exceeding the Supply Voltage

### RELAXATION OSCILLATOR

The TLV350x can easily be configured as a simple and inexpensive relaxation oscillator. In Figure 4, the R2 network sets the trip threshold at 1/3 and 2/3 of the supply. Since this is a high-speed circuit, the resistor values are rather low in order to minimize the effect of parasitic capacitance. The positive input alternates between 1/3 of V+ and 2/3 of V+ depending on whether the output is low or high. The time to charge (or discharge) is  $0.69R_1C$ . Therefore, the period is  $1.38R_1C$ . For 62pF and 1kΩ as shown in Figure 4, the output is calculated to be 10.9MHz. An implementation of this circuit oscillated at 9.6MHz. Parasitic capacitance and component tolerances explain the difference between theory and actual performance.

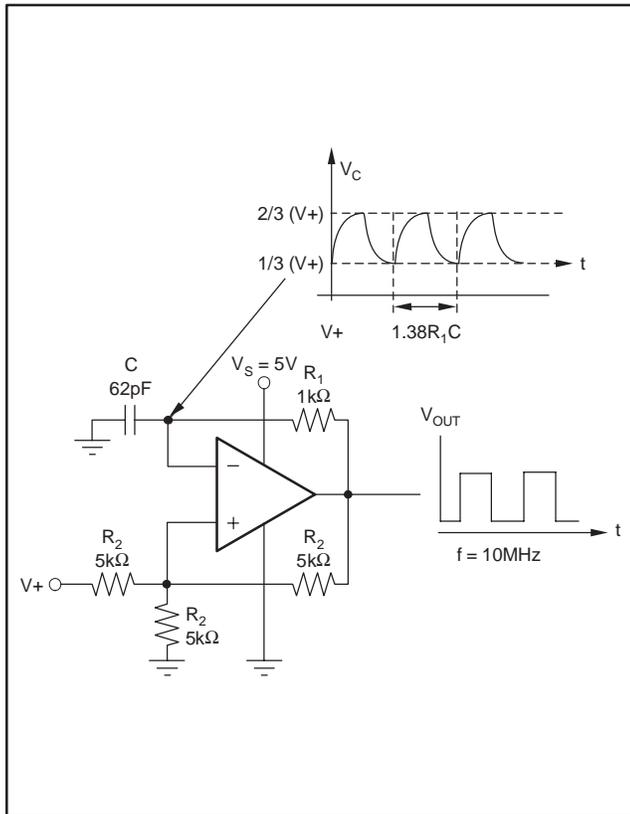


Figure 4. Relaxation Oscillator

### HIGH-SPEED WINDOW COMPARATOR

A window comparator circuit is used to determine when a signal is between two voltages. The TLV3502 can readily be used to create a high-speed window comparator.  $V_{HI}$  is the upper voltage threshold, and  $V_{LO}$  is the lower voltage threshold. When  $V_{IN}$  is between these two thresholds, the output in Figure 5 is high. Figure 6 shows a simple means of obtaining an active low output. Note that the reference levels are connected differently between Figure 5 and Figure 6. The operating voltage range of either circuit is 2.7V to 5.5V.

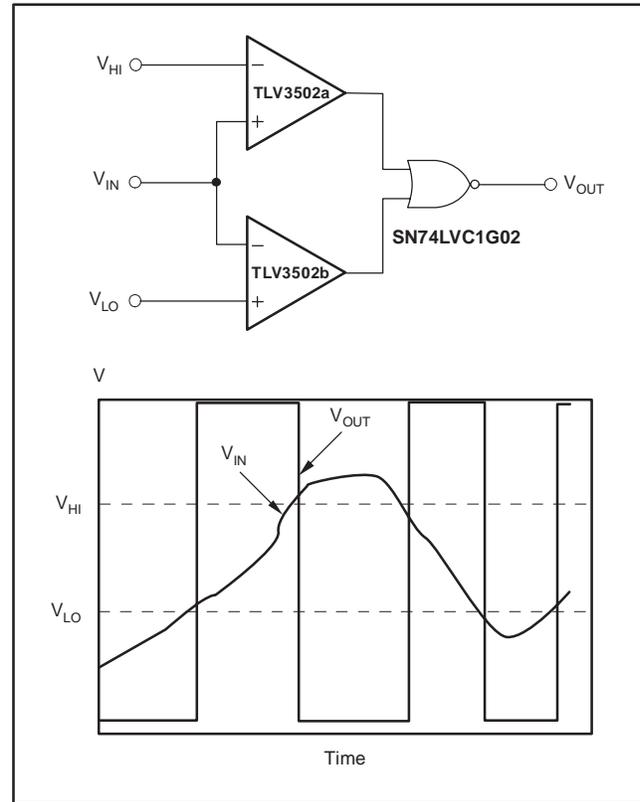


Figure 5. Window Comparator—Active High

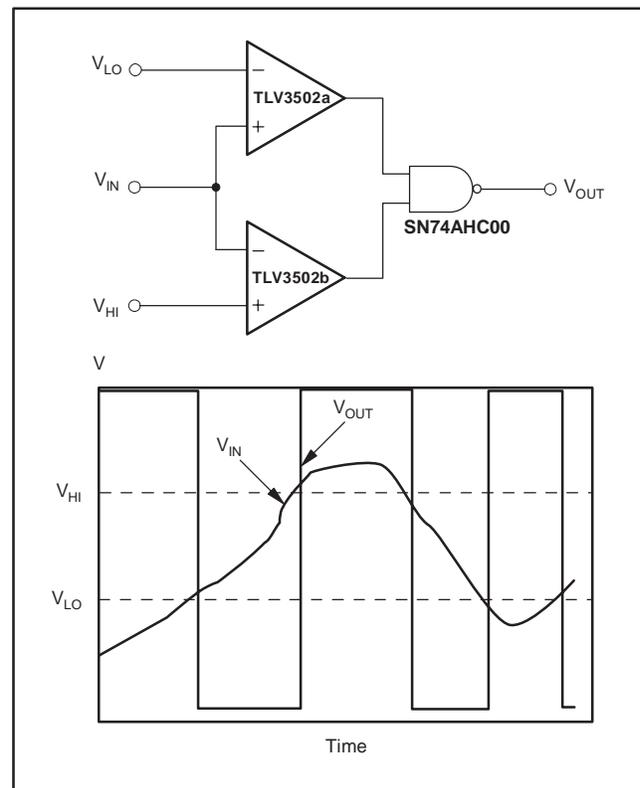


Figure 6. Window Comparator—Active Low

## PCB LAYOUT

For any high-speed comparator or amplifier, proper design and printed circuit board (PCB) layout are necessary for optimal performance. Excess stray capacitance on the active input, or improper grounding, can limit the maximum performance of high-speed circuitry.

Minimizing resistance from the signal source to the comparator input is necessary in order to minimize the propagation delay of the complete circuit. The source resistance along with input and stray capacitance creates an RC filter that delays voltage transitions at the input, and reduces the amplitude of high-frequency signals. The input capacitance of the TLV350x along with stray capacitance from an input pin to ground results in several picofarads of capacitance.

The location and type of capacitors used for power-supply bypassing are critical to high-speed comparators. The suggested 2.2 $\mu$ F tantalum capacitor do not need to be as close to the device as the 0.1 $\mu$ F capacitor, and may be shared with other devices. The 2.2 $\mu$ F capacitor buffers the power-supply line against ripple, and the 0.1 $\mu$ F capacitor provides a charge for the comparator during high-frequency switching.

In a high-speed circuit, fast rising and falling switching transients create voltage differences across lines that would be at the same potential at DC. To reduce this effect, a ground plane is often used to reduce difference in voltage potential within the circuit board. A ground plane has the advantage of minimizing the effect of stray capacitances on the circuit board by providing a more desirable path for the current to flow. With a signal trace over a ground plane, at high-frequency the return current (in the ground plane) tends to flow right under the signal trace. Breaks in the ground plane (as simple as through-hole leads and vias) increase the inductance of the plane, making it less effective at higher frequencies. Breaks in the ground plane for necessary vias should be spaced randomly.

Figure 7 shows an evaluation layout for the TLV3501 SO-8 package; Figure 8 is for the SOT23-5 package. They are shown with SMA connectors bringing signals on and off the board. RT1 and RT2 are termination resistors for + $V_{IN}$  and - $V_{IN}$ , respectively. C1 and C2 are power-supply bypass capacitors. Place the 0.1 $\mu$ F capacitor closest to the comparator. The ground plane is not shown, but the pads that the resistors and capacitors connect to are shown. Figure 9 shows a schematic of this circuit.

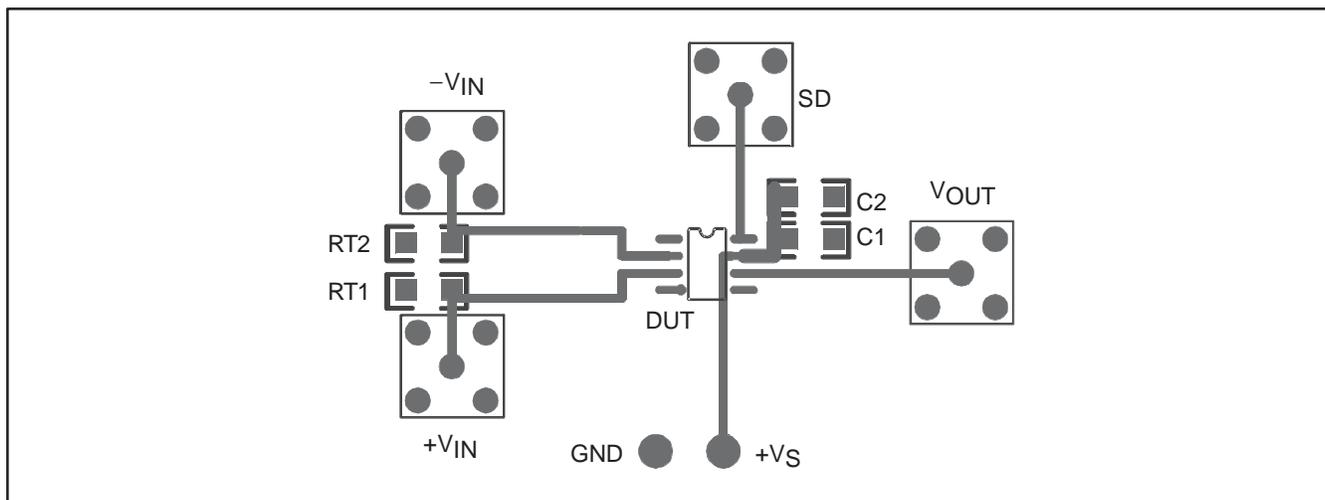


Figure 7. TLV3501D (SO-8) Sample Layout

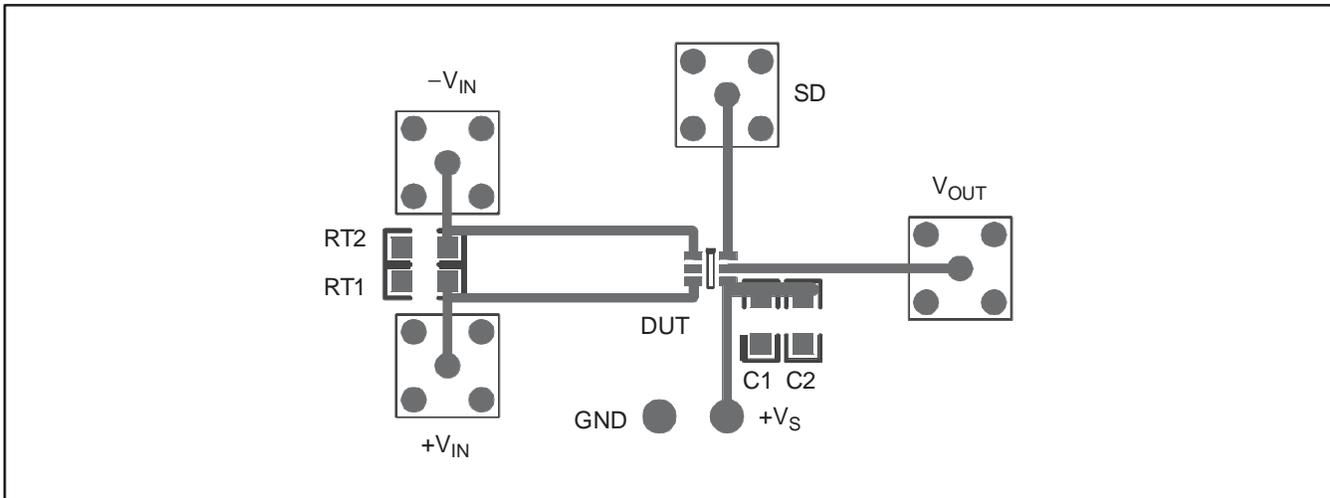


Figure 8. TLV3501DBV (SOT23) Sample Layout

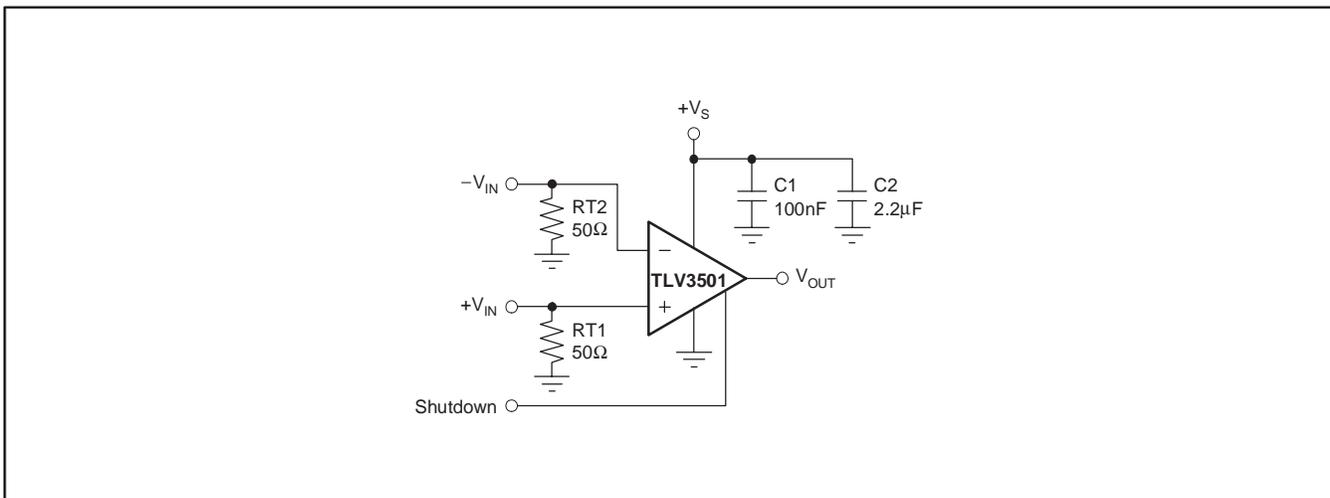


Figure 9. Schematic for Figure 7 and Figure 8

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TLV3501AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV3501AIDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV3501AIDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV3501AIDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV3501AIDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV3501AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV3501AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV3501AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV3502AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV3502AIDCNR	ACTIVE	SOT-23	DCN	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV3502AIDCNRG4	ACTIVE	SOT-23	DCN	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV3502AIDCNT	ACTIVE	SOT-23	DCN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV3502AIDCNTG4	ACTIVE	SOT-23	DCN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV3502AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV3502AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV3502AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

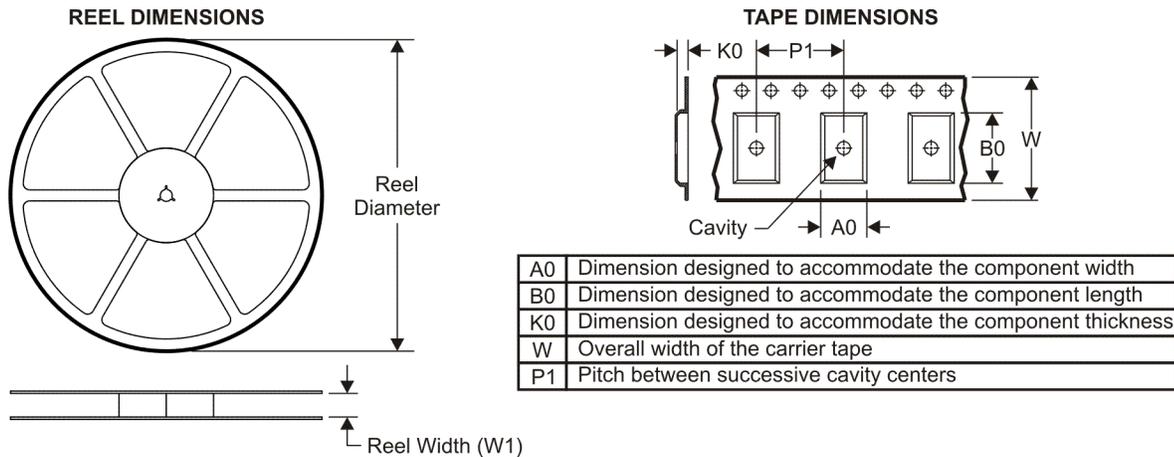
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

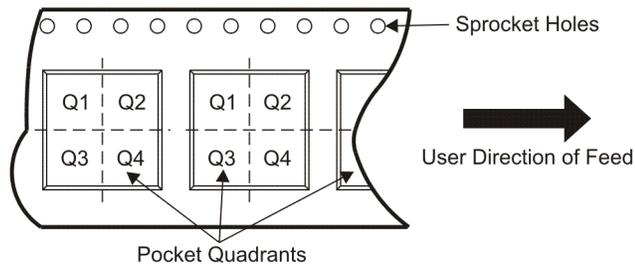
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**TAPE AND REEL INFORMATION**



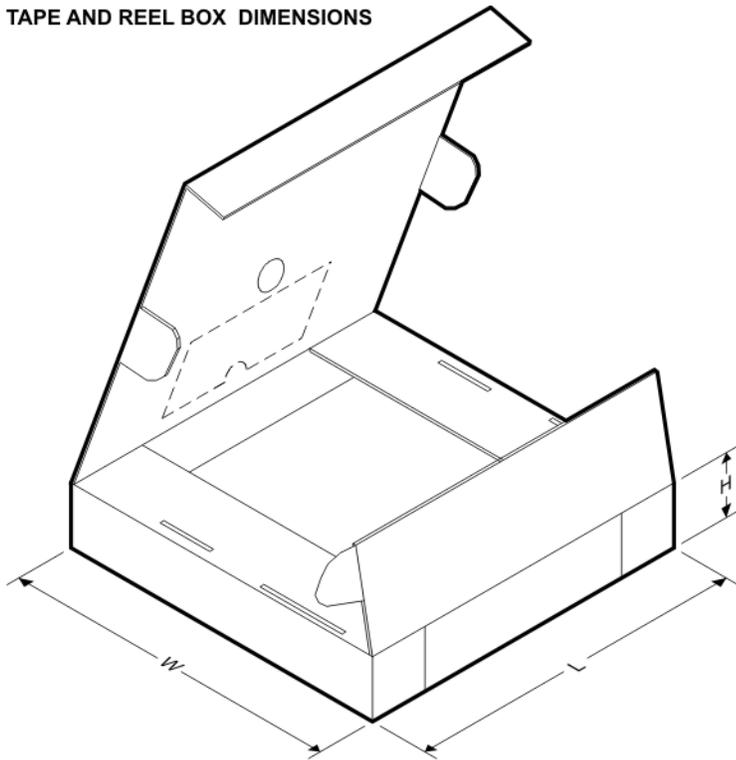
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3501AIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
TLV3501AIDBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
TLV3501AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV3502AIDCNR	SOT-23	DCN	8	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3502AIDCNT	SOT-23	DCN	8	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3502AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

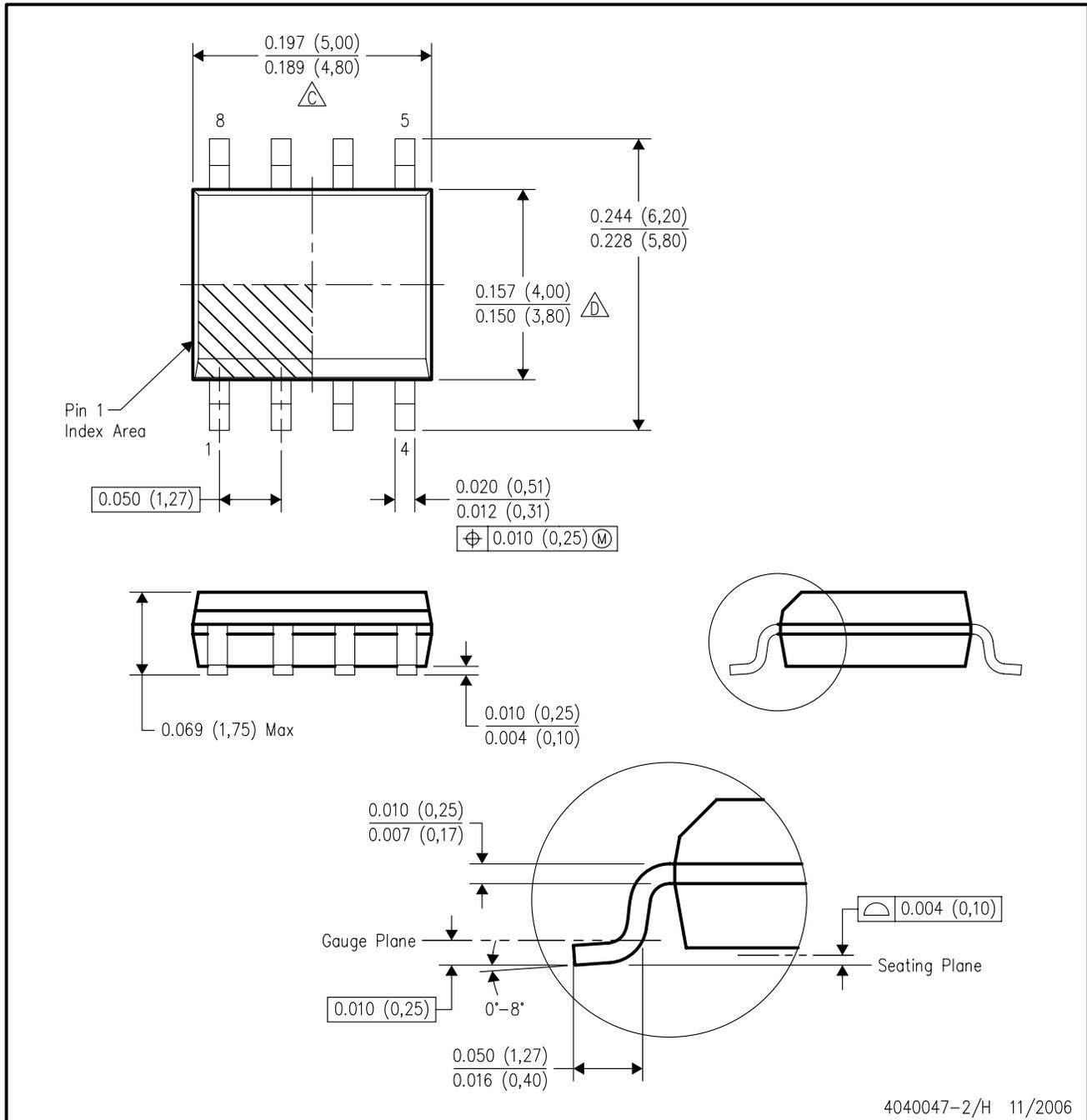


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3501AIDBVR	SOT-23	DBV	6	3000	184.0	184.0	50.0
TLV3501AIDBVT	SOT-23	DBV	6	250	190.5	212.7	31.8
TLV3501AIDR	SOIC	D	8	2500	346.0	346.0	29.0
TLV3502AIDCNR	SOT-23	DCN	8	3000	195.0	200.0	45.0
TLV3502AIDCNT	SOT-23	DCN	8	250	195.0	200.0	45.0
TLV3502AIDR	SOIC	D	8	2500	346.0	346.0	29.0

D (R-PDSO-G8)

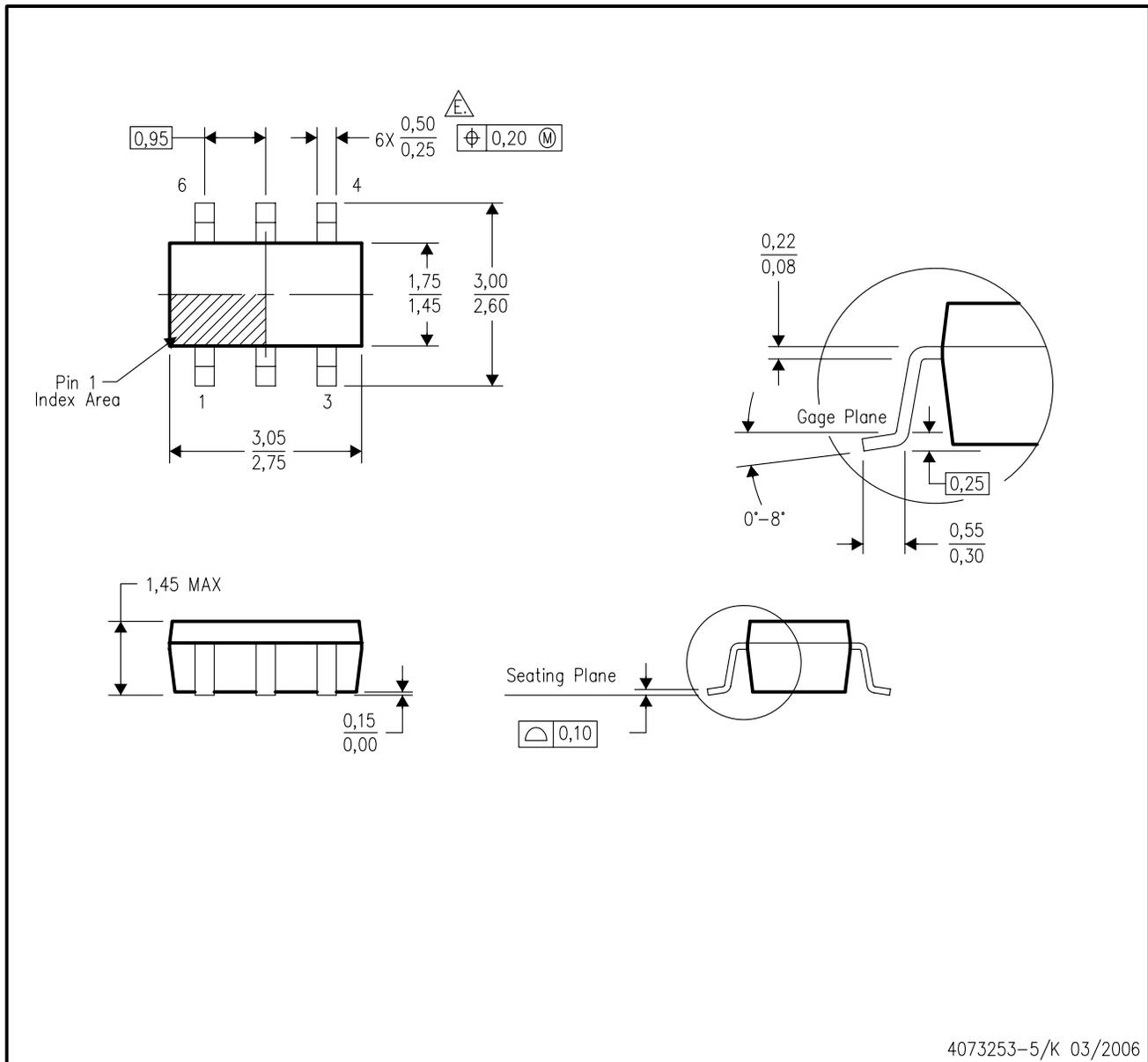
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AA.

DBV (R-PDSO-G6)

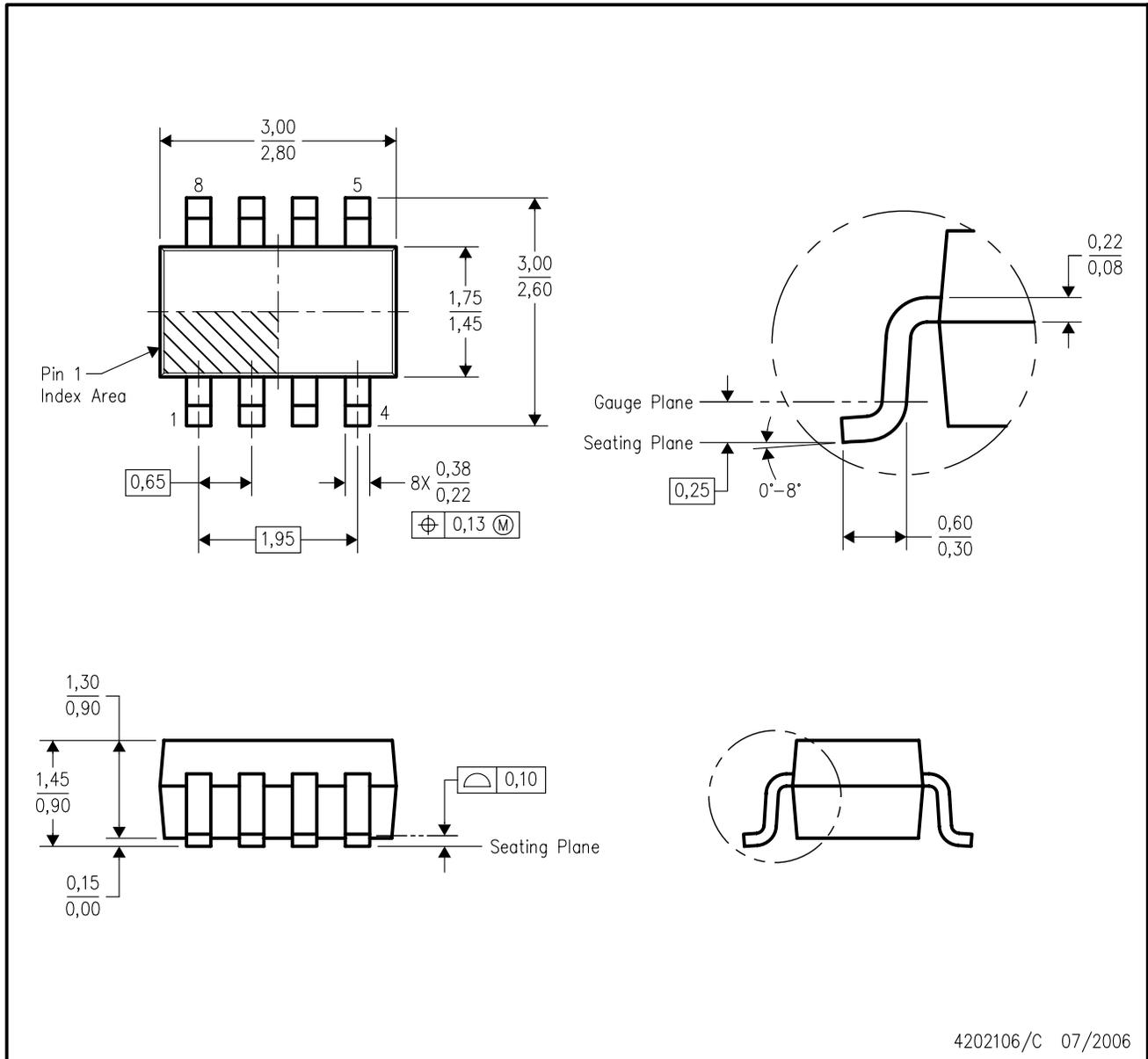
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- $\triangle E$  Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DCN (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Package outline exclusive of mold flash, metal burr & dambar protrusion/intrusion.
  - D. Package outline inclusive of solder plating.
  - E. A visual index feature must be located within the Pin 1 index area.
  - F. Falls within JEDEC MO-178 Variation BA.

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