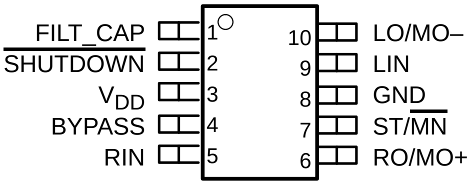
TPA0253
1-W MONO AUDIO POWER AMPLIFIER WITH HEADPHONE DRIVE

SLOS280D – JANUARY 2000 – REVISED NOVEMBER 2002

- **Ideal for Notebook Computers, PDAs, and Other Small Portable Audio Devices**
- **1 W Into 8-Ω From 5-V Supply**
- **0.3 W Into 8-Ω From 3-V Supply**
- **Stereo Head Phone Drive**
- **Mono (BTL) Signal Created by Summing Left and Right Signals Internally**
- **Wide Power Supply Compatibility**
  2.5 V to 5.5 V
- **Low Supply Current**
  - **3.2 mA Typical at 5 V**
  - **2.7 mA Typical at 3 V**
- **Shutdown Control . . . 1 μA Typical**
- **Shutdown Pin Is TTL Compatible**
- **–40°C to 85°C Operating Temperature Range**
- **Space-Saving, Thermally-Enhanced MSOP Packaging**

DGQ PACKAGE
(TOP VIEW)



description

The TPA0253 is a 1-W mono bridge-tied-load (BTL) amplifier designed to drive speakers with as low as 8-Ω impedance. The mono signal is created by summing left and right inputs internally. The amplifier can be reconfigured on the fly to drive two stereo single-ended (SE) signals into headphones. This makes the device ideal for use in small notebook computers, PDAs, digital personal audio players, anyplace a mono speaker and stereo headphones are required. From a 5-V supply, the TPA0253 can deliver 1-W of power into an 8-Ω speaker.

The gain of the input stage is set by the user-selected input resistor and a 50-kΩ internal feedback resistor ($A_V = -R_F/R_I$). The power stage is internally configured with a gain of –1.25 V/V in SE mode, and –2.5 V/V in BTL mode. Thus, the overall gain of the amplifier is 62.5 kΩ/R_I in SE mode and 125 kΩ/R_I in BTL mode. The input terminals are high-impedance CMOS inputs, and can be used as summing nodes.

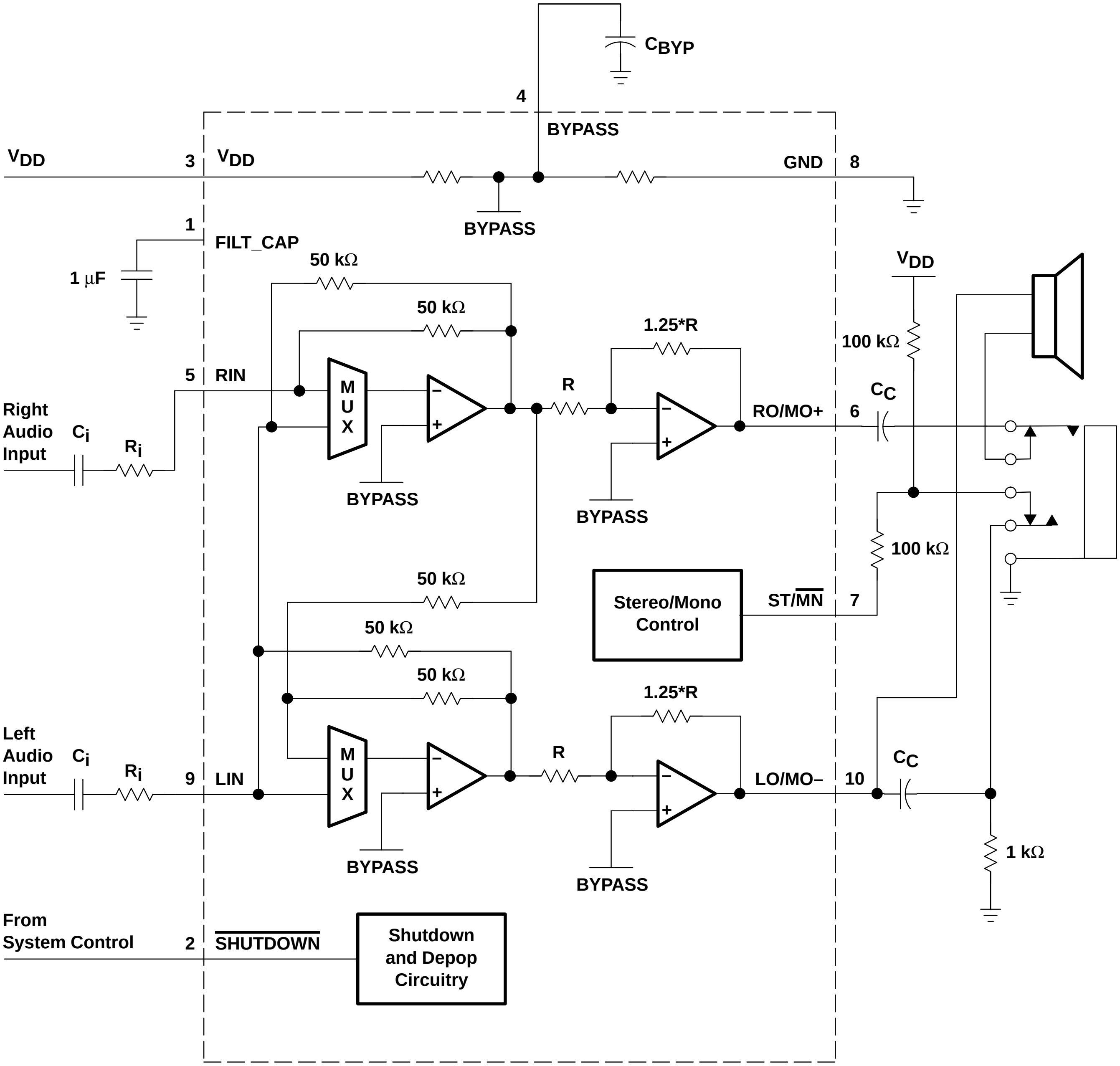
The TPA0253 is available in the 10-pin thermally-enhanced MSOP package (DGQ) and operates over an ambient temperature range of –40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	MSOP SYMBOLIZATION
	MSOP[†] (DGQ)	
–40°C to 85°C	TPA0253DGQ	AEL

[†] The DGQ package are available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0253DGQR).

schematic


C_{BYP}
4
BYPASS
V_{DD}
3
V_{DD}
GND
8
BYPASS
1
FILT_CAP
1 µF
50 kΩ
50 kΩ
1.25*R
V_{DD}
100 kΩ
5
RIN
M U X
R
C_C
RO/MO+
6
Right Audio Input
C_i
R_i
BYPASS
BYPASS
100 kΩ
50 kΩ
Stereo/Mono Control
ST/$\overline{MN}$
7
50 kΩ
50 kΩ
1.25*R
Left Audio Input
C_i
R_i
9
LIN
M U X
R
LO/MO–
10
C_C
1 kΩ
BYPASS
BYPASS
From System Control
2
$\overline{SHUTDOWN}$
Shutdown and Depop Circuitry

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	4	I	Midrail bias voltage
FILT_CAP	1		Terminal used to filter power supply
GND	8		Ground terminal
LIN	9	I	Left-channel input terminal
LO/MO–	10	O	Left-output in SE mode and mono negative output in BTL mode.
RIN	5	I	Right-channel input terminal
RO/MO+	6	O	Right-output in SE mode and mono positive output in BTL mode
$\overline{\text{SHUTDOWN}}$	2	I	TTL-compatible shutdown terminal
ST/$\overline{\text{MN}}$	7	I	Selects between stereo and mono mode. When held high, the amplifier is in SE stereo mode; while held low, the amplifier is in BTL mono mode.
V_{DD}	3	I	Positive power supply

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD}	6 V
Input voltage range, V_I	–0.3 V to V_{DD} +0.3 V
Continuous total power dissipation	internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A (see Table 3)	–40°C to 85°C
Operating junction temperature range, T_J	–40°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
DGQ	2.14 W§	17.1 mW/°C	1.37 W	1.11 W

‡ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (SLMA002), for more information on the PowerPAD™ package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of that document.

recommended operating conditions

			MIN	MAX	UNIT
Supply voltage, V_{DD}			2.5	5.5	V
High-level input voltage, V_{IH}	ST/$\overline{\text{MN}}$	V_{DD} = 3 V	2.7		V
		V_{DD} = 5 V	4.5		
	$\overline{\text{SHUTDOWN}}$		2		
Low-level input voltage, V_{IL}	ST/$\overline{\text{MN}}$	V_{DD} = 3 V		1.65	V
		V_{DD} = 5 V		2.75	
	$\overline{\text{SHUTDOWN}}$			0.8	
Operating free-air temperature, T_A			–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OO} \rvert$	Output offset voltage (measured differentially)	R_L = 4 Ω, ST/$\overline{\text{MN}}$ = 0 V, $\overline{\text{SHUTDOWN}}$ = 2 V			30	mV
PSRR	Power supply rejection ratio	V_{DD} = 2.9 V to 3.1 V, BTL mode		65		dB
$\lvert I_{IH} \rvert$	High-level input current	$\overline{\text{SHUTDOWN}}$, V_{DD} = 3.3 V, $V_I = V_{DD}$			1	µA
		ST/$\overline{\text{MN}}$, V_{DD} = 3.3 V, $V_I = V_{DD}$			1	
$\lvert I_{IL} \rvert$	Low-level input current	$\overline{\text{SHUTDOWN}}$, V_{DD} = 3.3 V, V_I = 0 V			1	µA
		ST/$\overline{\text{MN}}$, V_{DD} = 3.3 V, V_I = 0 V			1	
Z_I	Input impedance			50		kΩ
I_{DD}	Supply current	V_{DD} = 2.5 V, $\overline{\text{SHUTDOWN}}$ = 2 V		2.7	4	mA
$I_{DD(SD)}$	Supply current, shutdown mode	$\overline{\text{SHUTDOWN}}$ = 0 V		1	10	µA
R_F	Feedback resistor	V_{DD} = 2.5 V, R_L = 4 Ω, ST/$\overline{\text{MN}}$ = 1.375 V, $\overline{\text{SHUTDOWN}}$ = 2 V	47	50	57	kΩ

operating characteristics, V_{DD} = 3 V, T_A = 25°C, R_L = 8 Ω, f = 1 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power, see Note 1	THD = 0.1%,	BTL mode,	Gain = 14 dB		300		mW
		THD = 0.1% Gain = 1.9 dB	SE mode,	R_L = 32 Ω		30		
THD + N	Total harmonic distortion plus noise	P_O = 250 mW,	f = 20 Hz to 20 kHz			0.2%		
B_{OM}	Maximum output power bandwidth	Gain = 1.9 dB,	THD = 2%			20		kHz
	Supple ripple rejection ratio	f = 1 kHz,	$C_{(BYP)}$ = 0.47 µF	BTL mode		46		dB
				SE mode		68		
V_n	Noise output voltage	$C_{(BYP)}$ = 0.47 µF,	f = 20 Hz to 20 kHz	BTL mode		83		μV_{RMS}
				SE mode		33		

NOTE 1: Output power is measured at the output terminals of the device at f = 1 kHz.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OO} \rvert$	Output offset voltage (measured differentially)	R_L = 4 Ω, ST/$\overline{\text{MN}}$ = 0 V, $\overline{\text{SHUTDOWN}}$ = 2 V			30	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V, BTL mode		62		dB
$\lvert I_{IH} \rvert$	High-level input current	$\overline{\text{SHUTDOWN}}$, V_{DD} =5.5 V, $V_I = V_{DD}$			1	μA
		ST/$\overline{\text{MN}}$, V_{DD} = 5.5 V, $V_I = V_{DD}$			1	
$\lvert I_{IL} \rvert$	Low-level input current	$\overline{\text{SHUTDOWN}}$, V_{DD} = 5.5 V, V_I = 0 V			1	μA
		ST/$\overline{\text{MN}}$, V_{DD} = 5.5 V, V_I = 0 V			1	
Z_I	Input impedance			50		kΩ
I_{DD}	Supply current	$\overline{\text{SHUTDOWN}}$ = 2 V		3.2	4.8	mA
$I_{DD(SD)}$	Supply current, shutdown mode	$\overline{\text{SHUTDOWN}}$ = 0 V		1	10	μA

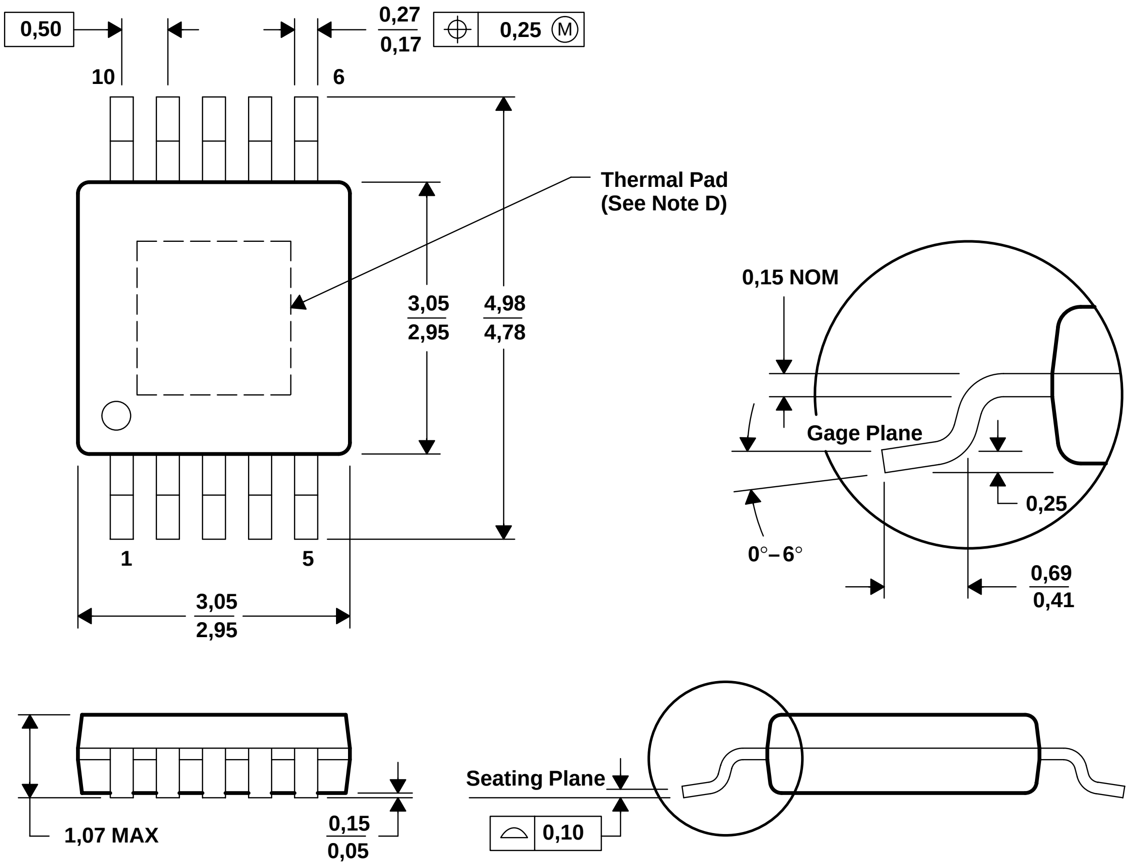
operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω, f = 1 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power (see Note 1)	THD = 0.1%,	BTL mode			1		W
		THD = 0.1%,	SE mode,	R_L = 32 Ω		85		mW
THD + N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 Hz to 20 kHz			0.33%		
B_{OM}	Maximum output power bandwidth	Gain = 8 dB,	THD = 2%			20		kHz
	Supple ripple rejection ratio	f = 1 kHz,	$C_{(BYP)}$ = 0.47 μF	BTL mode		46		dB
				SE mode		60		
V_n	Noise output voltage	$C_{(BYP)}$ = 0.47 μF,	f = 20 Hz to 20 kHz	BTL mode		85		μV_{RMS}
				SE mode		34		

NOTE 1: Output power is measured at the output terminals of the device at f = 1 kHz.

MECHANICAL DATA

DGQ (S-PDSO-G10) **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**



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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads. The dimension of the thermal pad is 1,40 mm (height as illustrated) × 1,80 (width as illustrated) mm (maximum). The pad is centered on the bottom of the package.

PowerPAD is a trademark of Texas Instruments.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPA0253DGQ	ACTIVE	MSOP-Power PAD	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPA0253DGQG4	ACTIVE	MSOP-Power PAD	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPA0253DGQR	ACTIVE	MSOP-Power PAD	DGQ	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPA0253DGQRG4	ACTIVE	MSOP-Power PAD	DGQ	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
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PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
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[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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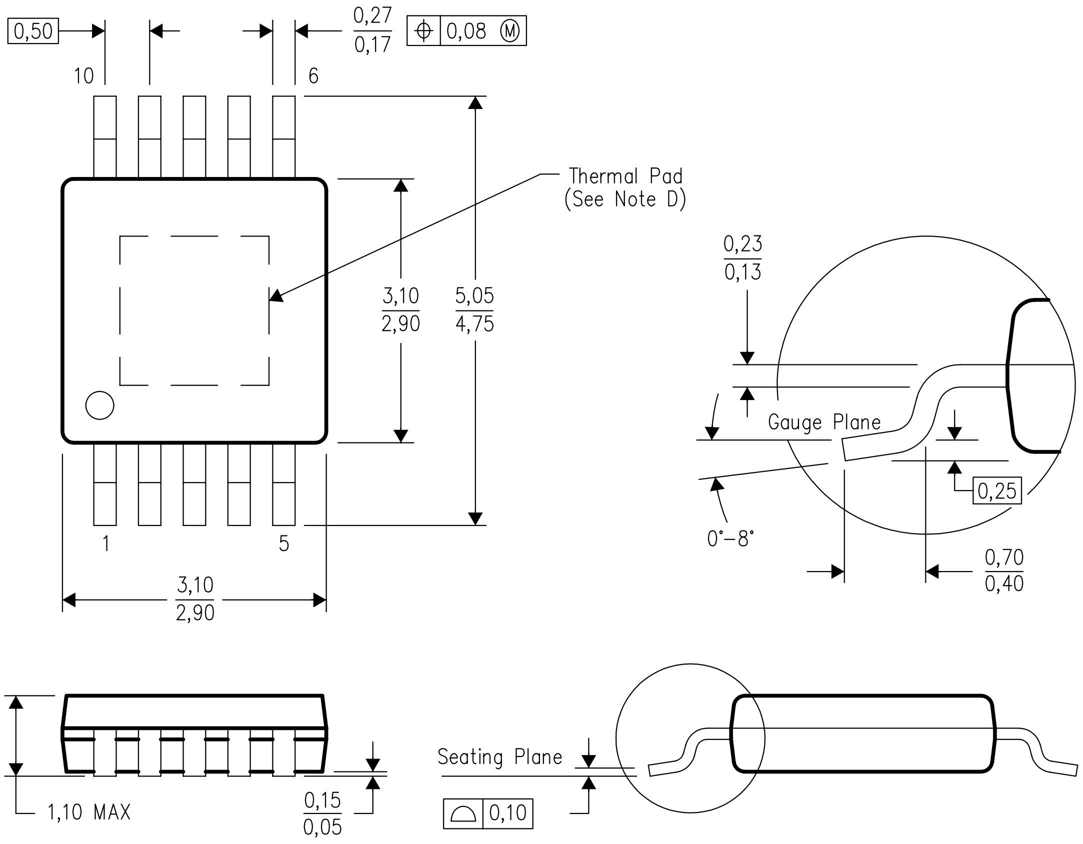
DGQ (S-PDSO-G10) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



4073273/D 02/04

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
- E. Falls within JEDEC MO-187 variation BA-T.

PowerPAD is a trademark of Texas Instruments.

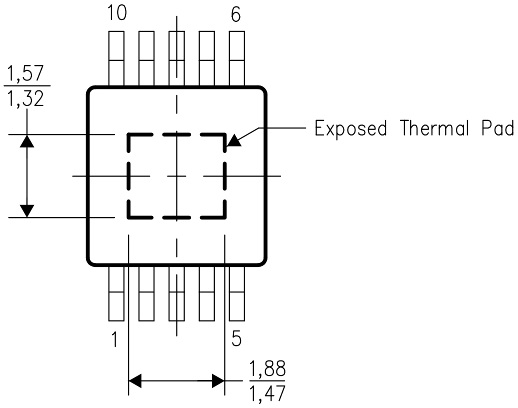
THERMAL PAD MECHANICAL DATA
DGQ (S-PDSO-G10)

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. When the thermal pad is soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



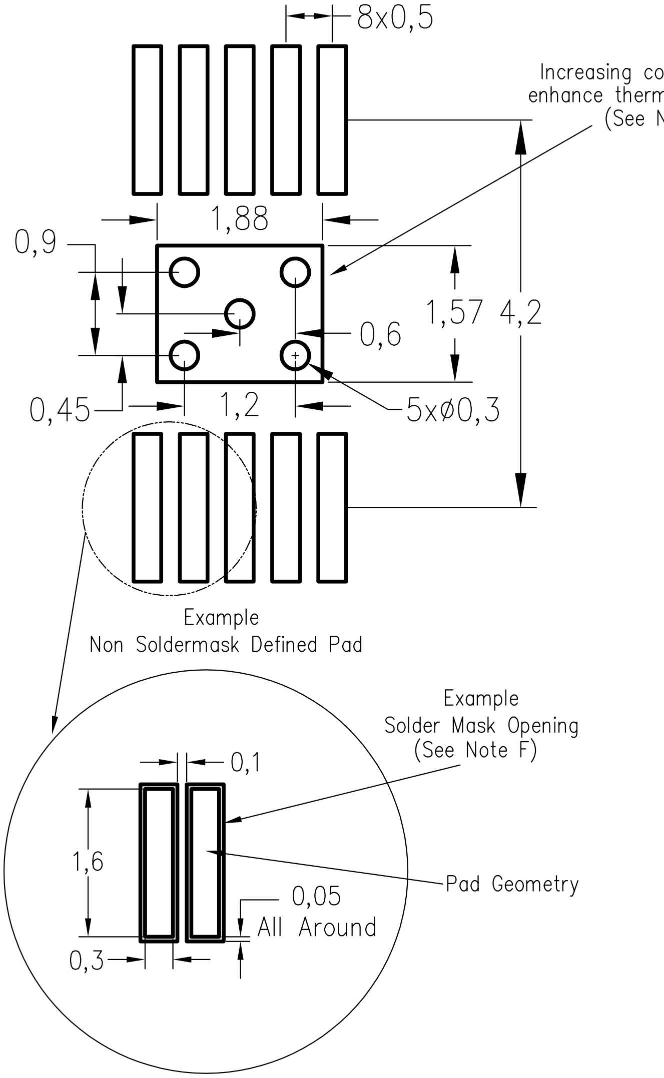
Top View

NOTE: All linear dimensions are in millimeters

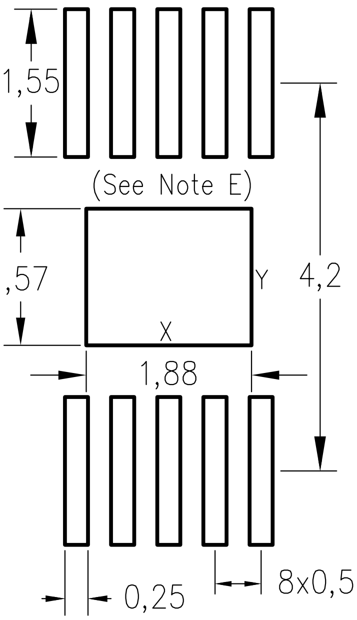
Exposed Thermal Pad Dimensions

DGQ (R–PDSO–G10) PowerPAD™

Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints



Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
Reference table below for other
solder stencil thicknesses



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.88	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207733/A 02/06

NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.

E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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PACKAGE OPTION ADDENDUM

18-Jul-2006

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[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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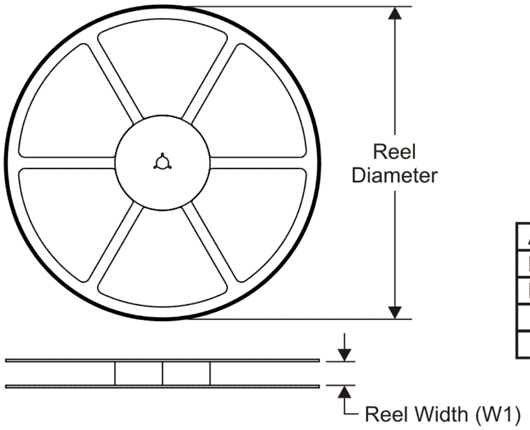
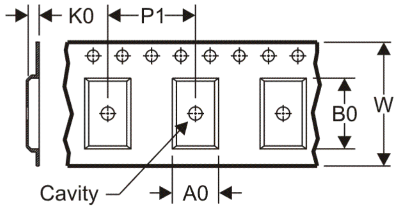
TAPE AND REEL INFORMATION

REEL DIMENSIONS

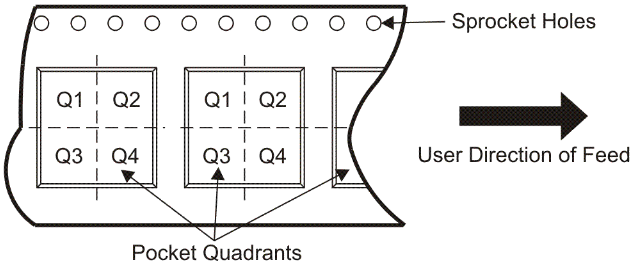


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

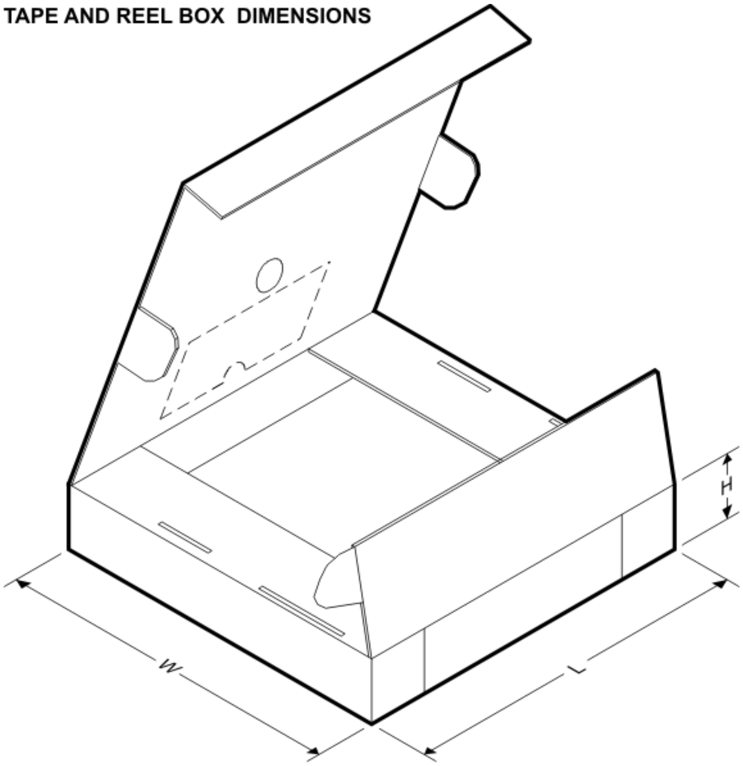
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA0253DGQR	MSOP-Power PAD	DGQ	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

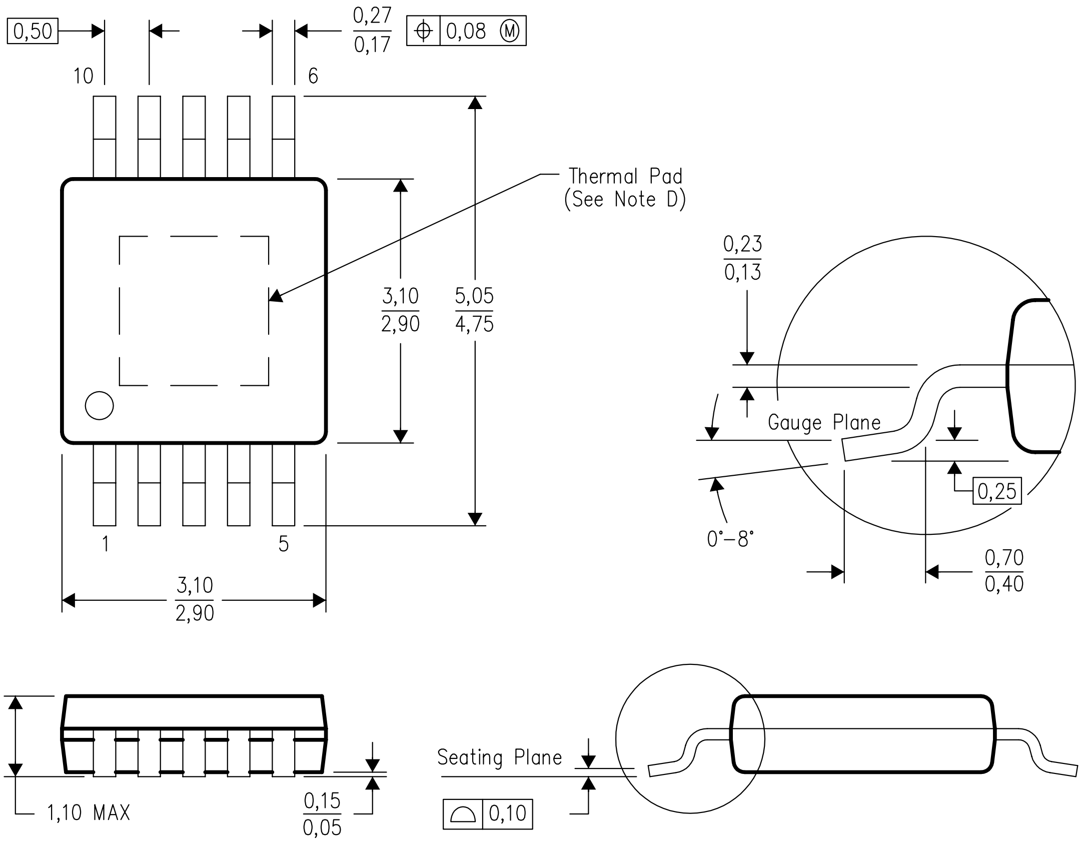
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA0253DGQR	MSOP-PowerPAD	DGQ	10	2500	358.0	335.0	35.0

DGQ (S-PDSO-G10) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
- E. Falls within JEDEC MO-187 variation BA-T.

THERMAL PAD MECHANICAL DATA

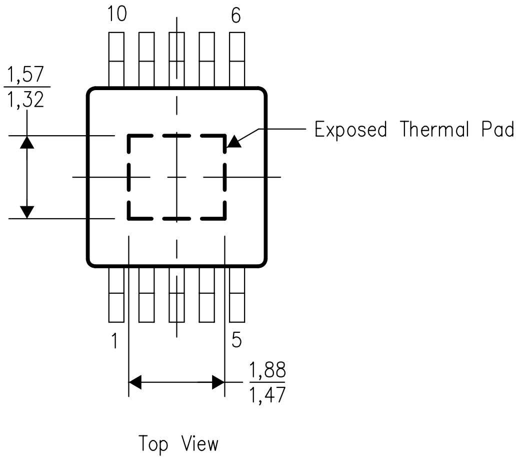
DGQ (S-PDSO-G10)

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

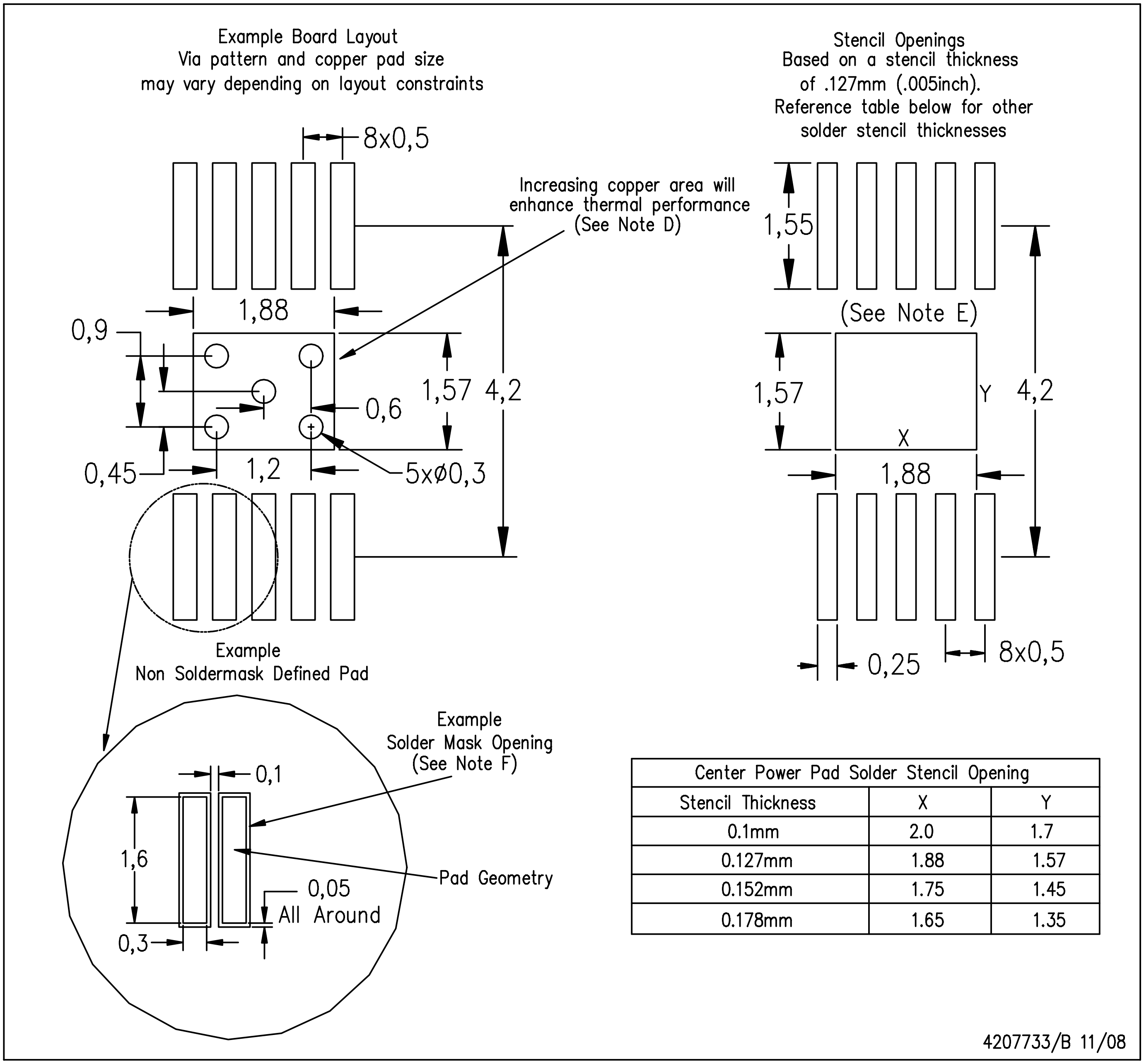
The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DGQ (R–PDSO–G10) PowerPAD™



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.88	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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