

## 2-BIT BIDIRECTIONAL VOLTAGE-LEVEL TRANSLATOR FOR OPEN-DRAIN AND PUSH-PULL APPLICATIONS

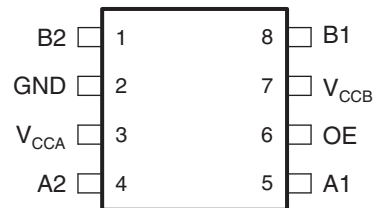
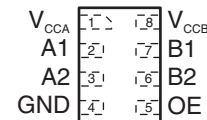
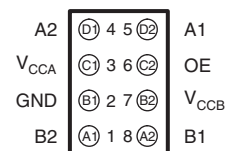
Check for Samples: [TXS0102](#)

### FEATURES

- No Direction-Control Signal Needed
- Max Data Rates
  - 24 Mbps (Push Pull)
  - 2 Mbps (Open Drain)
- Available in the Texas Instruments NanoStar™ Package
- 1.65 V to 3.6 V on A port and 2.3 V to 5.5 V on B port ( $V_{CCA} \leq V_{CCB}$ )
- $V_{CC}$  Isolation Feature – If Either  $V_{CC}$  Input Is at GND, Both Ports Are in the High-Impedance State
- No Power-Supply Sequencing Required – Either  $V_{CCA}$  or  $V_{CCB}$  Can Be Ramped First
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - A Port
    - 2500-V Human-Body Model (A114-B)
    - 250-V Machine Model (A115-A)
    - 1500-V Charged-Device Model (C101)
  - B Port
    - 8-kV Human-Body Model (A114-B)
    - 250-V Machine Model (A115-A)
    - 1500-V Charged-Device Model (C101)

### TYPICAL LEVEL-SHIFTER APPLICATIONS

- I<sup>2</sup>C/SMBus
- UART
- GPIO

DCT OR DCU PACKAGE  
(TOP VIEW)

DQE OR DQM PACKAGE  
(TOP VIEW)

YZP PACKAGE  
(BOTTOM VIEW)


### DESCRIPTION/ORDERING INFORMATION

This two-bit non-inverting translator is a bidirectional voltage-level translator and can be used to establish digital switching compatibility between mixed-voltage systems. It uses two separate configurable power-supply rails, with the A ports supporting operating voltages from 1.65 V to 3.6 V while it tracks the  $V_{CCA}$  supply, and the B ports supporting operating voltages from 2.3 V to 5.5 V while it tracks the  $V_{CCB}$  supply. This allows the support of both lower and higher logic signal levels while providing bidirectional translation capabilities between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

When the output-enable (OE) input is low, all I/Os are placed in the high-impedance state, which significantly reduces the power-supply quiescent current consumption.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.



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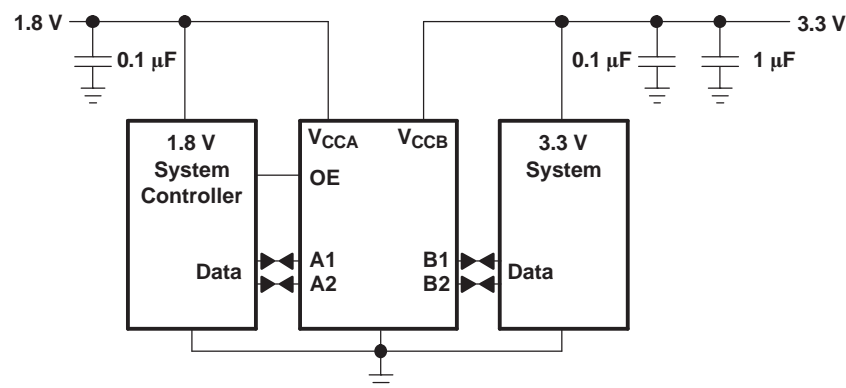
**ORDERING INFORMATION<sup>(1)</sup>**

T <sub>A</sub>	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(3)</sup>
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP	Reel of 3000	TXS0102YZPR	2H_
		Reel of 5000	TXS0102DQER	2H
	SON – DQE	Reel of 3000	TXS0102DQMR	2HR
	SSOP – DCT	Reel of 3000	TXS0102DCTR	NFE_ _ _
		Tube of 250	TXS0102DCTT	NFE_ _ _
	VSSOP – DCU	Reel of 3000	TXS0102DCUR	NFE_

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).
- (3) DCT: The actual top-side marking has three additional characters that designate the year, month, and wafer fab/assembly site.  
DCU: The actual top-side marking has one additional character that designates the wafer fab/assembly site.  
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

**PIN DESCRIPTION**

NO.			NAME	TYPE	FUNCTION
DCT, DCU	DQE, DQM	YZP			
1	6	A1	B2	I/O	Input/output B. Referenced to V <sub>CCB</sub> .
2	4	B1	GND	GND	Ground
3	1	C1	V <sub>CCA</sub>	Power	A-port supply voltage. $1.65\text{ V} \leq V_{CCA} \leq 3.6\text{ V}$ and $V_{CCA} \leq V_{CCB}$
4	3	D1	A2	I/O	Input/output A. Referenced to V <sub>CCA</sub> .
5	2	D2	A1	I/O	Input/output A. Referenced to V <sub>CCA</sub> .
6	5	C2	OE	Input	Output enable (active High). Pull OE low to place all outputs in 3-state mode. Referenced to V <sub>CCA</sub> .
7	8	B2	V <sub>CCB</sub>	Power	B-port supply voltage. $2.3\text{ V} \leq V_{CCB} \leq 5.5\text{ V}$
8	7	A2	B1	I/O	Input/output B. Referenced to V <sub>CCB</sub> .

**TYPICAL OPERATING CIRCUIT**

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage range		–0.5	4.6	V
V <sub>CCB</sub>	Supply voltage range		–0.5	6.5	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	A port	–0.5	4.6	V
		B port	–0.5	6.5	
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	A port	–0.5	4.6	V
		B port	–0.5	6.5	
V <sub>O</sub>	Voltage range applied to any output in the high or low state <sup>(2) (3)</sup>	A port	–0.5	V <sub>CCA</sub> + 0.5	V
		B port	–0.5	V <sub>CCB</sub> + 0.5	
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		–50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		–50	mA
I <sub>O</sub>	Continuous output current			±50	mA
	Continuous current through V <sub>CCA</sub> , V <sub>CCB</sub> , or GND			±100	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(4)</sup>	DCT package		220	°C/W
		DCU package		227	
		DQE package		261	
		DQM package		TBD	
		YZP package		102	
T <sub>stg</sub>	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CCA</sub> and V<sub>CCB</sub> are provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

## RECOMMENDED OPERATING CONDITIONS<sup>(1) (2)</sup>

		V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage <sup>(3)</sup>			1.65	3.6	V
V <sub>CCB</sub>	Supply voltage			2.3	5.5	V
V <sub>IH</sub>	High-level input voltage	A-port I/Os	1.65 V to 1.95 V	2.3 V to 5.5 V	V <sub>CCI</sub> – 0.2	V
			2.3 V to 3.6 V		V <sub>CCI</sub> – 0.4	
		B-port I/Os			V <sub>CCI</sub> – 0.4	
	OE input	1.65 V to 3.6 V	2.3 V to 5.5 V		V <sub>CCA</sub> × 0.65	5.5
V <sub>IL</sub> <sup>(4)</sup>	Low-level input voltage	A-port I/Os	1.65 V to 3.6 V	2.3 V to 5.5 V	0	V
		B-port I/Os			0	
		OE input			0	V <sub>CCA</sub> × 0.35
Δt/Δv	Input transition rise or fall rate	A-port I/Os, push-pull driving	1.65 V to 3.6 V	2.3 V to 5.5 V	10	ns/V
		B-port I/Os, push-pull driving			10	
		Control input			10	
T <sub>A</sub>	Operating free-air temperature			–40	85	°C

- (1) V<sub>CCI</sub> is the supply voltage associated with the input port.
- (2) V<sub>CCO</sub> is the supply voltage associated with the output port.
- (3) V<sub>CCA</sub> must be less than or equal to V<sub>CCB</sub>, and V<sub>CCA</sub> must not exceed 3.6 V.
- (4) The maximum V<sub>IL</sub> value is provided to ensure that a valid V<sub>OL</sub> is maintained. The V<sub>OL</sub> value is V<sub>IL</sub> plus the voltage drop across the pass-gate transistor.

**ELECTRICAL CHARACTERISTICS**<sup>(1) (2) (3)</sup>

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	T <sub>A</sub> = 25°C			–40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
V <sub>OHA</sub>		I <sub>OH</sub> = –20 μA, V <sub>IB</sub> ≥ V <sub>CCB</sub> – 0.4 V	1.65 V to 3.6 V	2.3 V to 5.5 V				V <sub>CCA</sub> × 0.67		V
V <sub>OLA</sub>		I <sub>OL</sub> = 1 mA, V <sub>IB</sub> ≤ 0.15 V	1.65 V to 3.6 V	2.3 V to 5.5 V				0.4		V
V <sub>OHB</sub>		I <sub>OH</sub> = –20 μA, V <sub>IA</sub> ≥ V <sub>CCA</sub> – 0.2 V	1.65 V to 3.6 V	2.3 V to 5.5 V				V <sub>CCB</sub> × 0.67		V
V <sub>OLB</sub>		I <sub>OL</sub> = 1 mA, V <sub>IA</sub> ≤ 0.15 V	1.65 V to 3.6 V	2.3 V to 5.5 V				0.4		V
I <sub>I</sub>	OE		1.65 V to 3.6 V	2.3 V to 5.5 V	±1			±2		μA
I <sub>off</sub>	A port		0 V	0 to 5.5 V	±1			±2		μA
	B port		0 to 3.6 V	0 V	±1			±2		μA
I <sub>OZ</sub>	A or B port		1.65 V to 3.6 V	2.3 V to 5.5 V	±1			±2		μA
I <sub>CCA</sub>		V <sub>I</sub> = V <sub>O</sub> = open, I <sub>O</sub> = 0	1.65 V to V <sub>CCB</sub>	2.3 V to 5.5 V				2.4		μA
			3.6 V	0 V				2.2		
			0 V	5.5 V				–1		
I <sub>CCB</sub>		V <sub>I</sub> = V <sub>O</sub> = open, I <sub>O</sub> = 0	1.65 V to V <sub>CCB</sub>	2.3 V to 5.5 V				12		μA
			3.6 V	0 V				–1		
			0 V	5.5 V				1		
I <sub>CCA</sub> + I <sub>CCB</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.65 V to V <sub>CCB</sub>	2.3 V to 5.5 V				14.4		μA
C <sub>I</sub>	OE		3.3 V	3.3 V	2.5			3.5		pF
C <sub>io</sub>	A or B port		3.3 V	3.3 V	10					pF
	A port				5			6		
	B port				6			7.5		

(1) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.(2) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.(3) V<sub>CCA</sub> must be less than or equal to V<sub>CCB</sub>, and V<sub>CCA</sub> must not exceed 3.6 V.

## TIMING REQUIREMENTS

over recommended operating free-air temperature range,  $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$  (unless otherwise noted)

				$V_{CCB} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 5\text{ V}$ $\pm 0.5\text{ V}$		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX		
Data rate		Push-pull driving		21		22		24		Mbps	
		Open-drain driving		2		2		2			
t <sub>w</sub>	Pulse duration	Push-pull driving		Data inputs	47		45		41		ns
		Open-drain driving			500		500		500		

## TIMING REQUIREMENTS

over recommended operating free-air temperature range,  $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (unless otherwise noted)

				$V_{CCB} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 5\text{ V}$ $\pm 0.5\text{ V}$		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX		
Data rate		Push-pull driving		20		22		24		Mbps	
		Open-drain driving		2		2		2			
t <sub>w</sub>	Pulse duration	Push-pull driving		Data inputs	50		45		41		ns
		Open-drain driving			500		500		500		

## TIMING REQUIREMENTS

over recommended operating free-air temperature range,  $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted)

				<b>V<sub>CC</sub> = 3.3 V ± 0.3 V</b>		<b>V<sub>CC</sub> = 5 V ± 0.5 V</b>		<b>UNIT</b>
				<b>MIN</b>	<b>MAX</b>	<b>MIN</b>	<b>MAX</b>	
Data rate	Push-pull driving			23		24		Mbps
	Open-drain driving			2		2		
t <sub>w</sub>	Pulse duration		Data inputs	43		41		ns
	Open-drain driving			500		500		

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PHL}$	A	B	Push-pull driving		5.3		5.4		6.8	ns
			Open-drain driving	2.3	8.8	2.4	9.6	2.6	10	
$t_{PLH}$			Push-pull driving		6.8		7.1		7.5	
			Open-drain driving	45	260	36	208	27	198	
$t_{PHL}$	B	A	Push-pull driving		4.4		4.5		4.7	ns
			Open-drain driving	1.9	5.3	1.1	4.4	1.2	4	
$t_{PLH}$			Push-pull driving		5.3		4.5		0.5	
			Open-drain driving	45	175	36	140	27	102	
$t_{en}$	OE	A or B			200		200		200	ns
$t_{dis}$	OE	A or B			50		40		35	ns
$t_{rA}$	A-port rise time		Push-pull driving	3.2	9.5	2.3	9.3	2	7.6	ns
			Open-drain driving	38	165	30	132	22	95	
$t_{rB}$	B-port rise time		Push-pull driving	4	10.8	2.7	9.1	2.7	7.6	ns
			Open-drain driving	34	145	23	106	10	58	
$t_{fA}$	A-port fall time		Push-pull driving	2	5.9	1.9	6	1.7	13.3	ns
			Open-drain driving	4.4	6.9	4.3	6.4	4.2	6.1	
$t_{fB}$	B-port fall time		Push-pull driving	2.9	13.8	2.8	16.2	2.8	16.2	
			Open-drain driving	6.9	13.8	7.5	16.2	7	16.2	
$t_{SK(O)}$	Channel-to-channel skew				0.7		0.7		0.7	ns
Max data rate			Push-pull driving	21		22		24		Mbps
			Open-drain driving	2		2		2		

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V <sub>CCB</sub> = 2.5 V ± 0.2 V		V <sub>CCB</sub> = 3.3 V ± 0.3 V		V <sub>CCB</sub> = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PHL</sub>	A	B	Push-pull driving	3.2		3.7		3.8		ns
t <sub>PLH</sub>			Open-drain driving	1.7	6.3	2	6	2.1	5.8	
			Push-pull driving	3.5		4.1		4.4		
			Open-drain driving	43	250	36	206	27	190	
t <sub>PHL</sub>	B	A	Push-pull driving	3		3.6		4.3		ns
t <sub>PLH</sub>			Open-drain driving	1.8	4.7	2.6	4.2	1.2	4	
			Push-pull driving	2.5		1.6		1		
			Open-drain driving	44	170	37	140	27	103	
t <sub>en</sub>	OE	A or B		200		200		200		ns
t <sub>dis</sub>	OE	A or B		50		40		35		ns
t <sub>rA</sub>	A-port rise time		Push-pull driving	2.8	7.4	2.6	6.6	1.8	5.6	ns
			Open-drain driving	34	149	28	121	24	89	
t <sub>rB</sub>	B-port rise time		Push-pull driving	3.2	8.3	2.9	7.2	2.4	6.1	ns
			Open-drain driving	35	151	24	112	12	64	
t <sub>fA</sub>	A-port fall time		Push-pull driving	1.9	5.7	1.9	5.5	1.8	5.3	ns
			Open-drain driving	4.4	6.9	4.3	6.2	4.2	5.8	
t <sub>fB</sub>	B-port fall time		Push-pull driving	2.2	7.8	2.4	6.7	2.6	6.6	ns
			Open-drain driving	5.1	8.8	5.4	9.4	5.4	10.4	
t <sub>SK(O)</sub>	Channel-to-channel skew			0.7		0.7		0.7		ns
Max data rate			Push-pull driving	20		22		24		Mbps
			Open-drain driving	2		2		2		

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
				MIN	MAX	MIN	MAX	
$t_{PHL}$	A	B	Push-pull driving	2.4		3.1		ns
			Open-drain driving	1.3	4.2	1.4	4.6	
$t_{PLH}$			Push-pull driving	4.2		4.4		
			Open-drain driving	36	204	28	165	
$t_{PHL}$	B	A	Push-pull driving	2.5		3.3		ns
			Open-drain driving	1	124	1	97	
$t_{PLH}$			Push-pull driving	2.5		2.6		
			Open-drain driving	3	139	3	105	
$t_{en}$	OE	A or B		200		200		ns
$t_{dis}$	OE	A or B		40		35		ns
$t_{rA}$	A-port rise time		Push-pull driving	2.3	5.6	1.9	4.8	ns
			Open-drain driving	25	116	19	85	
$t_{rB}$	B-port rise time		Push-pull driving	2.5	6.4	2.1	7.4	ns
			Open-drain driving	26	116	14	72	
$t_{fA}$	A-port fall time		Push-pull driving	2	5.4	1.9	5	ns
			Open-drain driving	4.3	6.1	4.2	5.7	
$t_{fB}$	B-port fall time		Push-pull driving	2.3	7.4	2.4	7.6	ns
			Open-drain driving	5	7.6	4.8	8.3	
$t_{SK(O)}$	Channel-to-channel skew			0.7		0.7		ns
Max data rate			Push-pull driving	23		24		Mbps
			Open-drain driving	2		2		



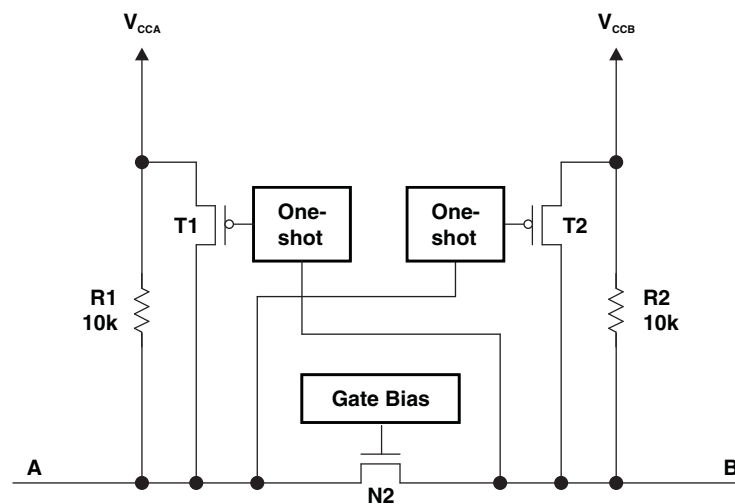
## PRINCIPLES OF OPERATION

### Applications

The TXS0102 can be used to bridge the digital-switching compatibility gap between two voltage nodes to successfully interface logic threshold levels found in electronic systems. It should be used in a point-to-point topology for interfacing devices or systems operating at different interface voltages with one another. Its primary target application use is for interfacing with open-drain drivers on the data I/Os such as I<sup>2</sup>C or 1-wire, where the data is bidirectional and no control signal is available. The TXS0102 can also be used in applications where a push-pull driver is connected to the data I/Os, but the TXB0102 might be a better option for such push-pull applications.

### Architecture

The TXS0102 architecture (see Figure 1) is an auto-direction-sensing based translator that does not require a direction-control signal to control the direction of data flow from A to B or from B to A.



**Figure 1. Architecture of a TXS01xx Cell**

These two bidirectional channels independently determine the direction of data flow without a direction-control signal. Each I/O pin can be automatically reconfigured as either an input or an output, which is how this auto-direction feature is realized.

The TXS0102 is part of TI's "Switch" type voltage translator family and employs two key circuits to enable this voltage translation:

- 1) An N-channel pass-gate transistor topology that ties the A-port to the B-port and
- 2) Output one-shot (O.S.) edge-rate accelerator circuitry to detect and accelerate rising edges on the A or B ports

For bidirectional voltage translation, pull-up resistors are included on the device for dc current sourcing capability. The  $V_{GATE}$  gate bias of the N-channel pass transistor is set at approximately one threshold voltage ( $V_T$ ) above the  $V_{CC}$  level of the low-voltage side. Data can flow in either direction without guidance from a control signal.

The O.S. rising-edge rate accelerator circuitry speeds up the output slew rate by monitoring the input edge for transitions, helping maintain the data rate through the device. During a low-to-high signal rising edge, the O.S. circuits turn on the PMOS transistors (T1, T2) to increase the current drive capability of the driver for approximately 30 ns or 95% of the input edge, whichever occurs first. This edge-rate acceleration provides high ac drive by bypassing the internal 10-k $\Omega$  pull-up resistors during the low-to-high transition to speed up the signal. The output resistance of the driver is decreased to approximately 50  $\Omega$  to 70  $\Omega$  during this acceleration phase. To minimize dynamic  $I_{CC}$  and the possibility of signal contention, the user should wait for the O.S. circuit to turn-off before applying a signal in the opposite direction. The worst-case duration is equal to the minimum pulse-width number provided in the *Timing Requirements* section of this data sheet.

## Input Driver Requirements

The continuous dc-current "sinking" capability is determined by the external system-level open-drain (or push-pull) drivers that are interfaced to the TXS0102 I/O pins. Since the high bandwidth of these bidirectional I/O circuits is used to facilitate this fast change from an input to an output and an output to an input, they have a modest dc-current "sourcing" capability of hundreds of micro-Amps, as determined by the internal 10-k $\Omega$  pullup resistors.

The fall time ( $t_{fA}$ ,  $t_{fB}$ ) of a signal depends on the edge-rate and output impedance of the external device driving TXS0102 data I/Os, as well as the capacitive loading on the data lines.

Similarly, the  $t_{pHL}$  and max data rates also depend on the output impedance of the external driver. The values for  $t_{fA}$ ,  $t_{fB}$ ,  $t_{pHL}$ , and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50  $\Omega$ .

## Output Load Considerations

TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper O.S. triggering takes place. PCB signal trace-lengths should be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The O.S. circuits have been designed to stay on for approximately 30 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic  $I_{CC}$ , load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the TXS0102 output sees, so it is recommended that this lumped-load capacitance be considered to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

## Power Up

During operation, ensure that  $V_{CCA} \leq V_{CCB}$  at all times. The sequencing of each power supply will not damage the device during the power up operation, so either power supply can be ramped up first.

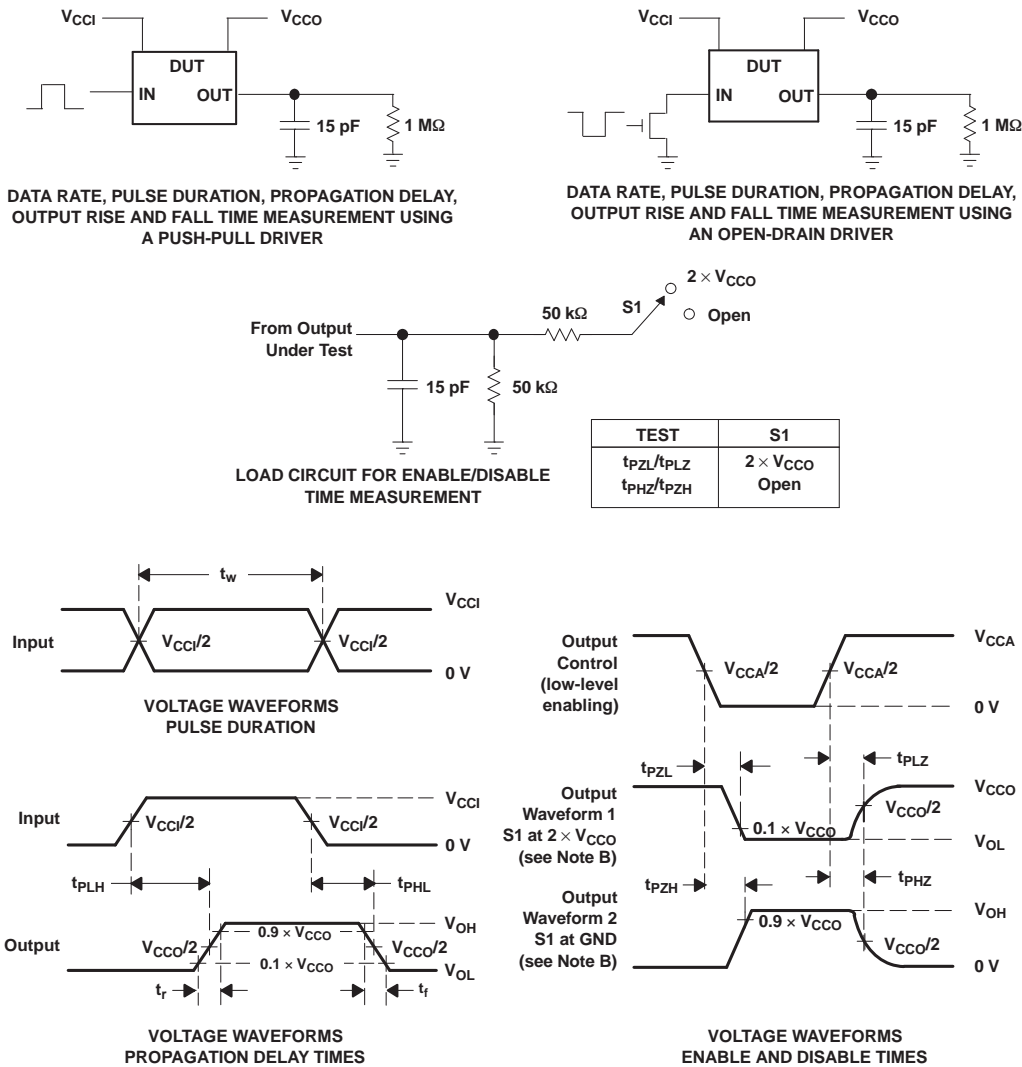
## Enable and Disable

The TXS0102 has an OE input that is used to disable the device by setting OE low, which places all I/Os in the Hi-Z state. The disable time ( $t_{dis}$ ) indicates the delay between the time when OE goes low and when the outputs are disabled (Hi-Z). The enable time ( $t_{en}$ ) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

## Pullup or Pulldown Resistors on I/O Lines

Each A-port I/O has an internal 10-k $\Omega$  pullup resistor to  $V_{CCA}$ , and each B-port I/O has an internal 10-k $\Omega$  pullup resistor to  $V_{CCB}$ . If a smaller value of pullup resistor is required, an external resistor must be added from the I/O to  $V_{CCA}$  or  $V_{CCB}$  (in parallel with the internal 10-k $\Omega$  resistors). Adding lower value pull-up resistors will effect  $V_{OL}$  levels, however. The internal pull-ups of the TXS0102 are disabled when the OE pin is low.

## PARAMETER MEASUREMENT INFORMATION



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $dv/dt \geq 1$  V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H.  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
- I.  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.
- J. All parameters and waveforms are not applicable to all devices.

**Figure 2. Load Circuit and Voltage Waveforms**

## REVISION HISTORY

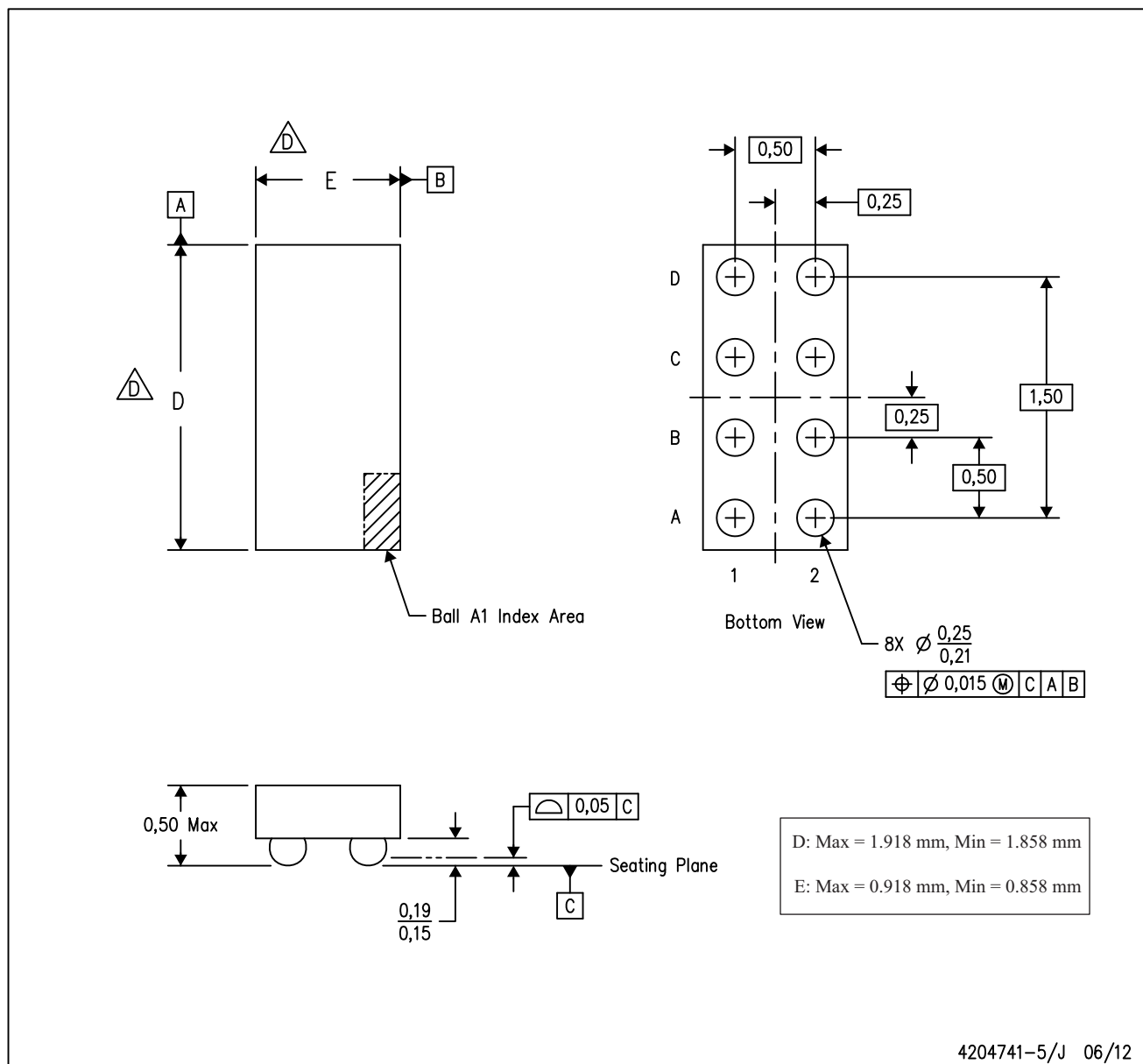
### Changes from Revision C (May 2009) to Revision D


### Page

- Added TOP-SIDE MARKING for SON - DQE and SON - DQM Packages in the ORDERING INFORMATION table. .... [2](#)

YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.
  -  The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
  - E. This package is a Pb-free solder ball design. Refer to the 8 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TXS0102DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TXS0102DCTRE4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TXS0102DCTT	ACTIVE	SM8	DCT	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TXS0102DCTTE4	ACTIVE	SM8	DCT	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TXS0102DCTTG4	ACTIVE	SM8	DCT	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TXS0102DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
TXS0102DCURG4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TXS0102DCUT	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TXS0102DCUTG4	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TXS0102DQER	ACTIVE	X2SON	DQE	8	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TXS0102DQMR	ACTIVE	X2SON	DQM	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TXS0102YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0102DCUR	US8	DCU	8	3000	180.0	9.0	2.05	3.3	1.0	4.0	8.0	Q3
TXS0102DCUR	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TXS0102DQER	X2SON	DQE	8	5000	180.0	8.4	1.17	1.67	0.73	4.0	8.0	Q1
TXS0102DQMR	X2SON	DQM	8	3000	180.0	9.5	1.4	2.0	0.5	4.0	8.0	Q1
TXS0102DQMR	X2SON	DQM	8	3000	180.0	8.4	1.57	2.21	0.59	4.0	8.0	Q1
TXS0102YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1
TXS0102YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1



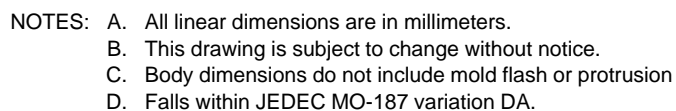
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

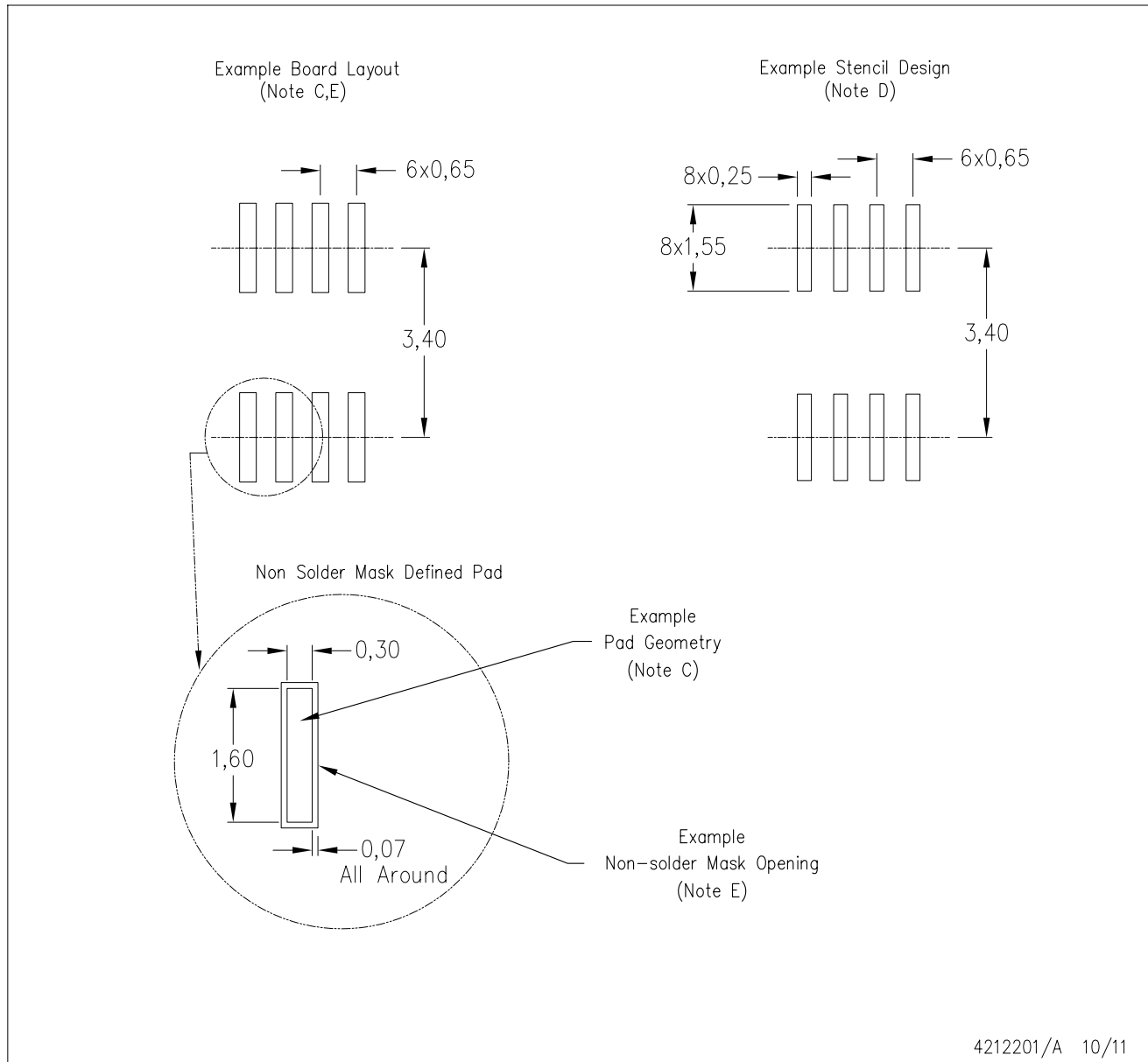
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0102DCUR	US8	DCU	8	3000	182.0	182.0	20.0
TXS0102DCUR	US8	DCU	8	3000	202.0	201.0	28.0
TXS0102DQER	X2SON	DQE	8	5000	202.0	201.0	28.0
TXS0102DQMR	X2SON	DQM	8	3000	180.0	180.0	30.0
TXS0102DQMR	X2SON	DQM	8	3000	202.0	201.0	28.0
TXS0102YZPR	DSBGA	YZP	8	3000	210.0	185.0	35.0
TXS0102YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

## PLASTIC SMALL-OUTLINE PACKAGE



DCT (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



## NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8)

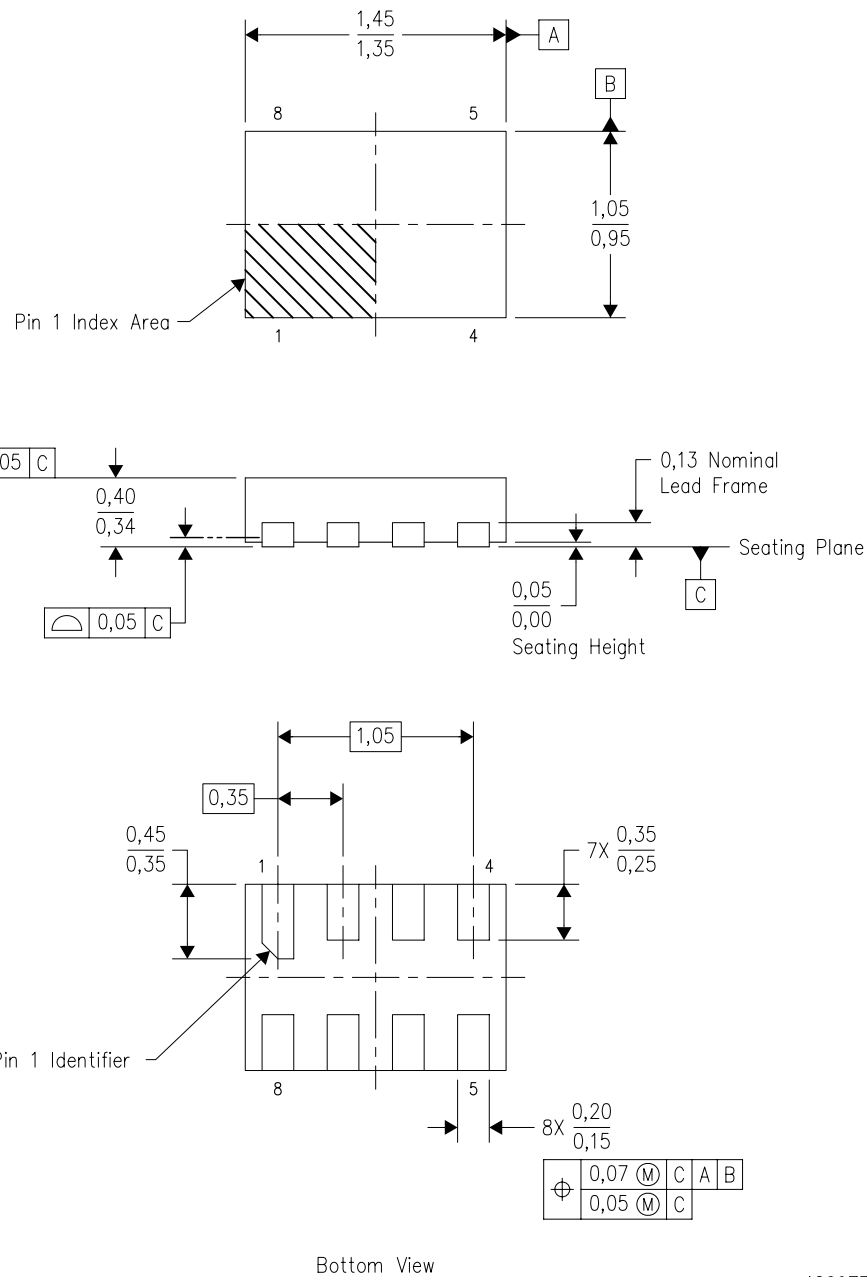
PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DQE (R-PX2SON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



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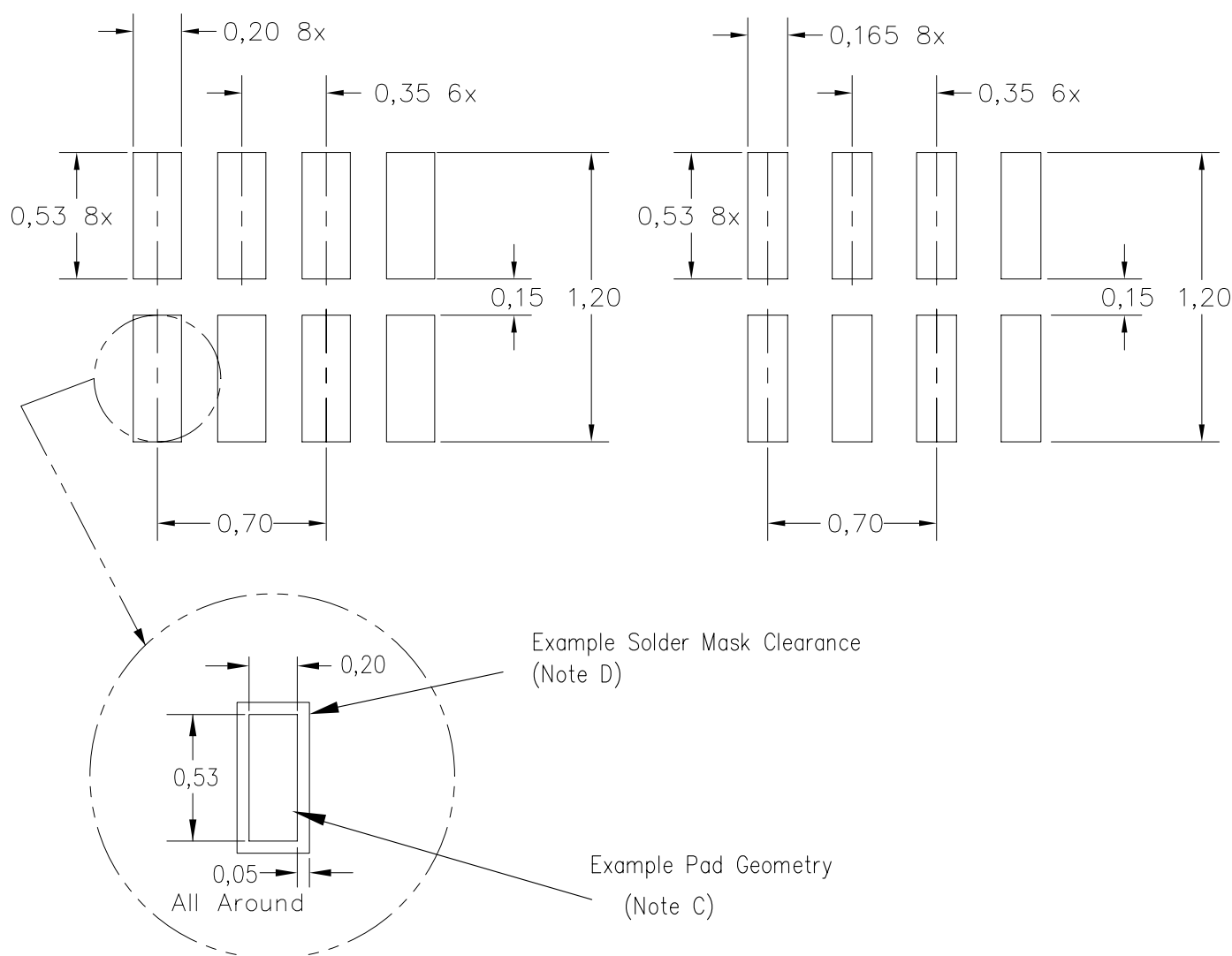
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. SON (Small Outline No-Lead) package configuration.
  - D. This package complies to JEDEC MO-287 variation X2EAF.

DQE (R-PX2SON-N8)

PLASTIC SMALL OUTLINE NO-LEAD

Example Board Layout

Example Stencil Design  
(Note E)

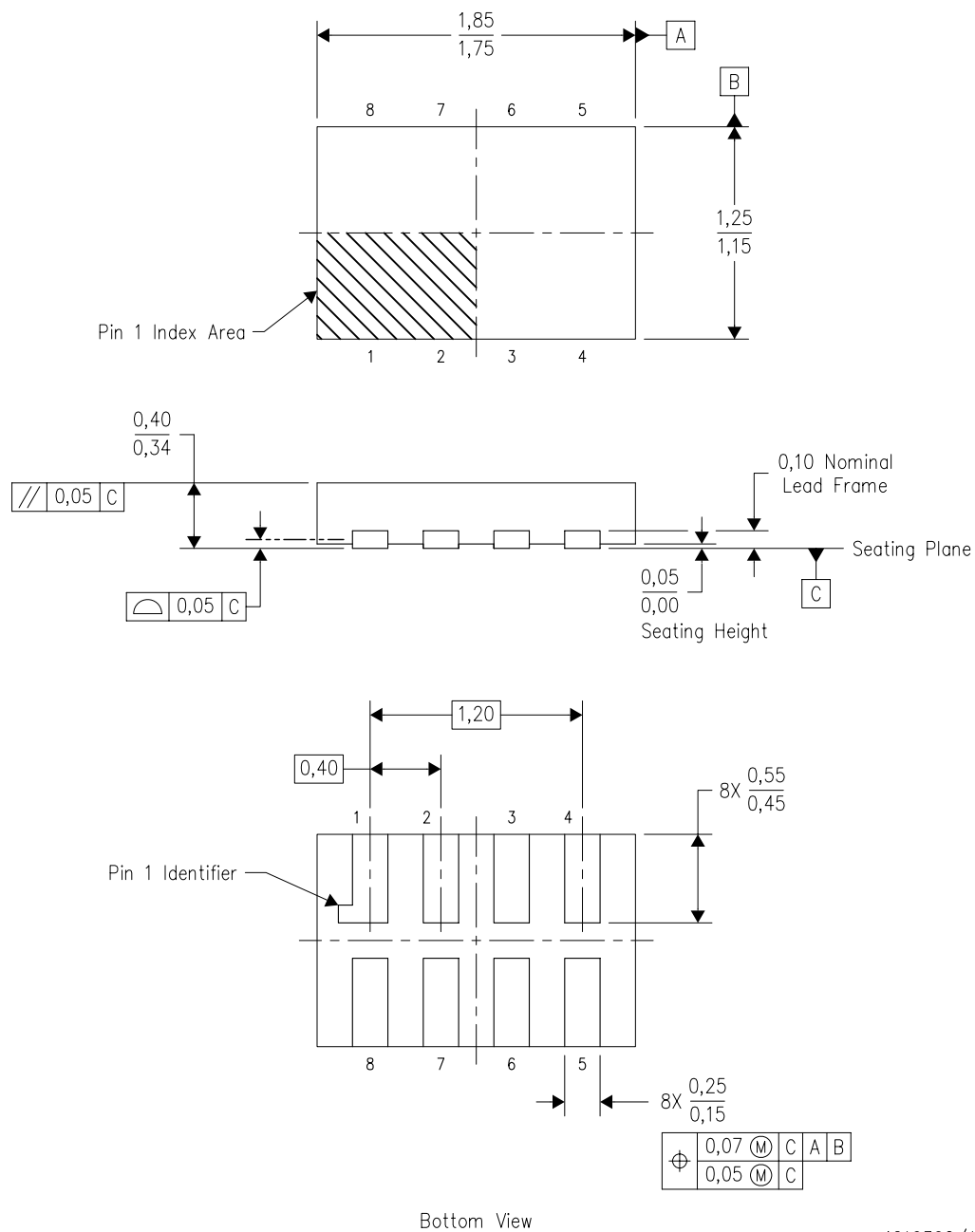


4211032/B 02/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
  - Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Over-printing land for acceptable area ratio is not viable due to land width and bridging potential. Customer may further reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.
  - Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
  - Component placement force should be minimized to prevent excessive paste block deformation.

DQM (R-PX2SON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



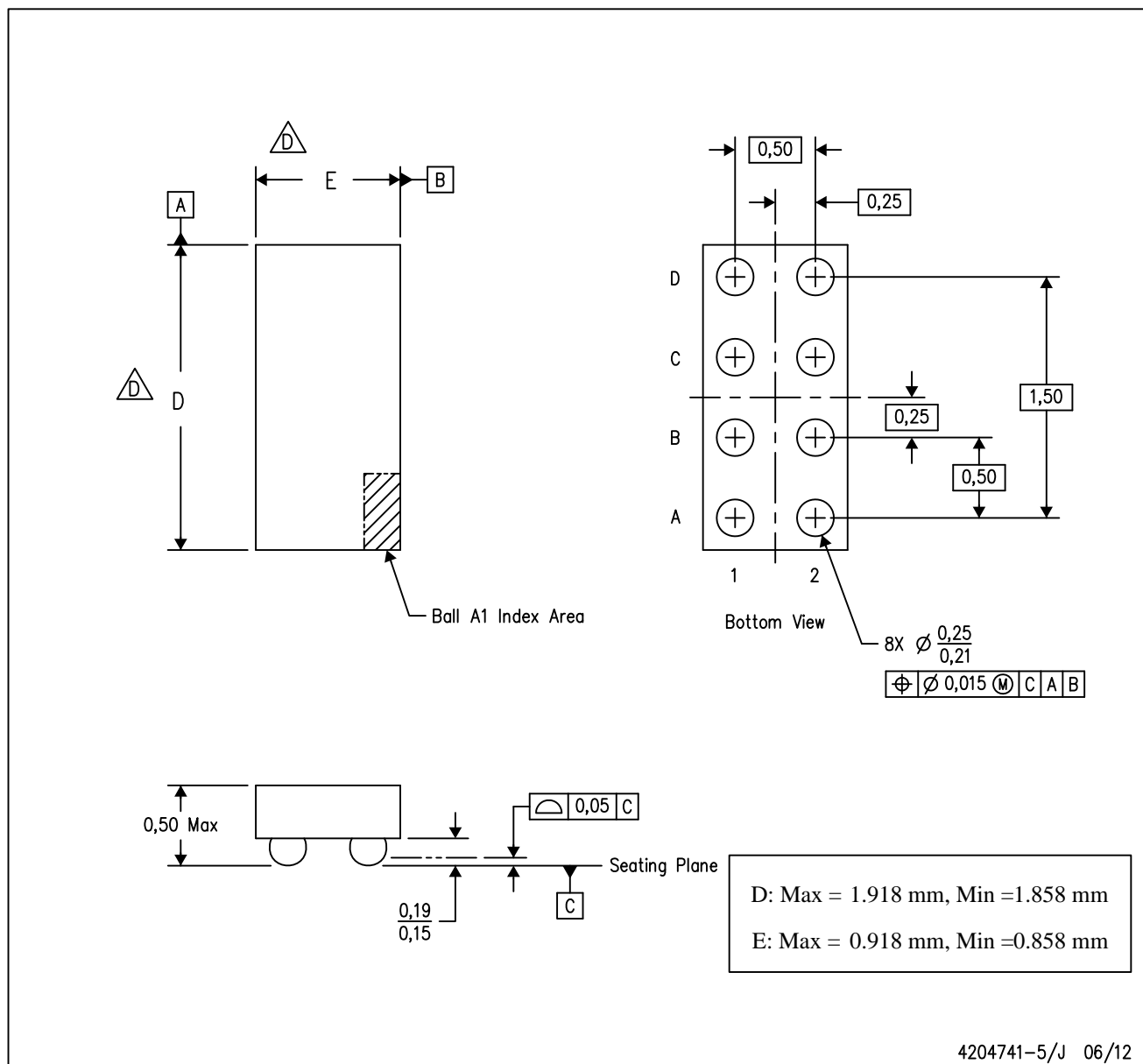
4210302/A 06/2009

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. SON (Small Outline No-Lead) package configuration.



YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



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  - C. NanoFree™ package configuration.
  - The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
  - E. This package is a Pb-free solder ball design. Refer to the 8 YEP package (drawing 4204725) for tin-lead (SnPb).

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