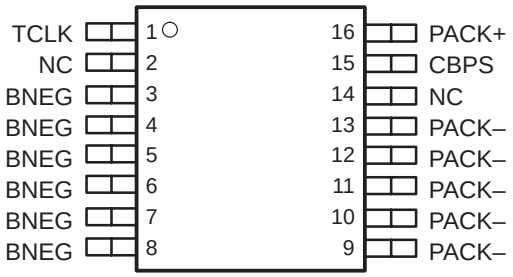
- **Protects Sensitive Lithium-Ion Cells From Overcharging and Over-Discharging**
- **Dedicated for One-Cell Applications**
- **Integrated Low-Impedance MOSFET Switch and Sense Resistor**
- **Precision Trimmed Overcharge and Overdischarge Voltage Limits**
- **Extremely Low Power Drain**
- **3-A Current Capacity**
- **Overcurrent and Short-Circuit Protection**
- **Reverse Charger Protection**
- **Thermal Protection**

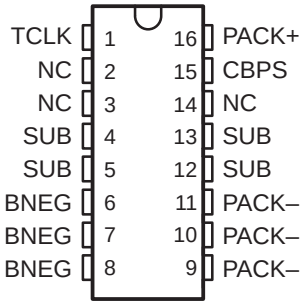
PW PACKAGE
(TOP VIEW)



description

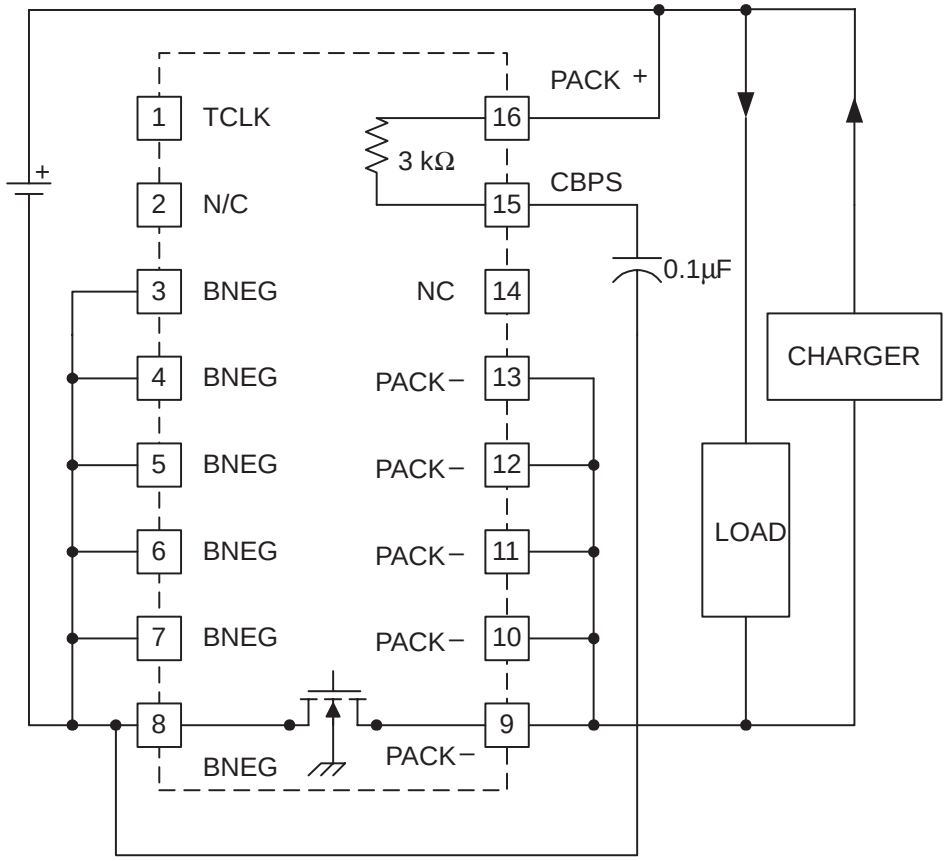
The UCC3952 monolithic BiCMOS lithium–ion battery protection circuit increases the useful operating life of a one-cell rechargeable battery pack. Cell protection features include internally trimmed charge and discharge voltage limits, discharge current limit with a delayed shutdown, and an ultra-low-current sleep mode state when the cell is discharged. Additional features include an on-chip MOSFET for reduced external component count and a charge pump for reduced power losses while charging or discharging a low-cell-voltage battery pack. This protection circuit requires one external capacitor and can operate and safely shut down in a short circuit condition.

DP PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

application diagram



AVAILABLE OPTIONS

T_A	PACKAGES	
	TSSOP–16 (PW)	SOIC–16 (DP)
–20°C to 70 °C	UCC3952PW–1	UCC3952DP–1
	UCC3952PW–2	UCC3952DP–2
	UCC3952PW–3	UCC3952DP–3
	UCC3952PW–4	UCC3952DP–4

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage (PACK+ to BNEG) . . . . . 7 V
Maximum forward voltage (PACK+ to PACK–) . . . . . 16 V
Maximum reverse voltage (where PACK+ to BNEG = 5V) . . . . . –8 V
Maximum cell continuous charge current . . . . . 3 A
Junction temperature, T_J . . . . . –55°C to 150°C
Storage Temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Data Book for thermal limitations and considerations of packages. All voltages are referenced to GND.

electrical characteristics, T_A = –20°C to 70°C, all voltages are with respect to BNEG (unless otherwise stated)

state transition threshold

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{(OV)}$	Normal to overcharge voltage	UCC3952–1		4.15	4.20	4.25	V
		UCC3952–2		4.20	4.25	4.30	
		UCC3952–3		4.25	4.30	4.35	
		UCC3952–4		4.30	4.35	4.40	
$V_{(OVR)}$	Overcharge to normal recovery voltage	UCC3952–1		3.85	3.90	3.95	V
		UCC3952–2		3.90	3.95	4.00	
		UCC3952–3		3.95	4.00	4.05	
		UCC3952–4		4.00	4.05	4.10	
$V_{(UV)}$	Normal to undercharge			2.25	2.35	2.45	V
$V_{(UVR)}$	Undercharge to normal recovery			2.55	2.65	2.75	V
$t_{d(OD)}$	Overcharge delay time			10	25	40	ms

short circuit protection

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{(THLD)}$	Discharge current limit	PACK+ = 3.7 V	3.0		6.0	A
$t_{d(DLY)}$	Discharge current delay	PACK+ = 3.7 V, I_I = 6 A	1		3.0	ms
$R_{(RESET)}$	Discharge current reset resistance	PACK+ = 3.7 V	7.5			MΩ

bias

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{DD}	Supply current	$V_{(UV)} < V_{(PACK)} < V_{(OV)}$		5	8	µA
$I_{DD(OV)}$	Operating supply current in overvoltage	$V_{(OV)} < V_{(PACK)}$		11	24	µA
$I_{(SD)}$	Shutdown current	$V_{(PACK)}$ = 2.0 V			2.5	µA
$V_{(min)}$	Minimum cell voltage when all circuits are fully functional				1.7	V
$t_d(OV)$	Overvoltage delay time		1		2	s

electrical characteristics, T_A = –20°C to 70°C, all voltages are with respect to BNEG (unless otherwise stated) (continued)

FET switch

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{(PACK–)}$	Voltage at PACK–	PACK+ > V_{OV} , $I_{(SWITCH)}$ = 1 mA to 2 A, Battery overcharged state switch permits discharge current only.		100	400	mV
		PACK+ = 2.5V, $I_{(SWITCH)}$ = –1 mA to –2 A, Battery overdischarged state switch permits charge current only.	–600	–100		mV
R_{ON}	Series resistance of the device	PACK+ = 2.5 V, In normal mode (when not in OV or UV). This value includes package and bondwire resistance.		50	75	mΩ

thermal shutdown

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$T_{(SD)}$	Thermal shutdown temperature (see Note 2)			135		°C

NOTE 2: This parameter is ensured by design and is not production tested.

detailed description

pin descriptions

BNEG

Connect the negative terminal of the battery to this pin.

PACK+

Connect to the positive terminal of the battery. This pin is available to the user.

CBPS

This power supply bypass pin is connected to PACK+ through an internal 3-kΩ resistor. An external 0.1-µF capacitor must be connected between this pin and BNEG.

PACK–

The negative terminal of the battery pack (negative terminal available to the user). The internal FET switch connects this terminal to the BNEG terminal to give the battery pack user appropriate access to the battery. In an overcharged state, only discharge current is permitted. In an overdischarged state, only charge current is permitted.

SUB (DP Package Only)

Do not connect. These pins must be electrically isolated from all other pins. The SUB pins may be soldered to an isolated copper pad for heatsinking. However, most applications do not require heatsinking.

TCLK

Production test mode pin. This pin is used to provide a high-frequency clock to the IC during production testing. In an application, this pin is left unconnected or tied to BNEG.

APPLICATION INFORMATION

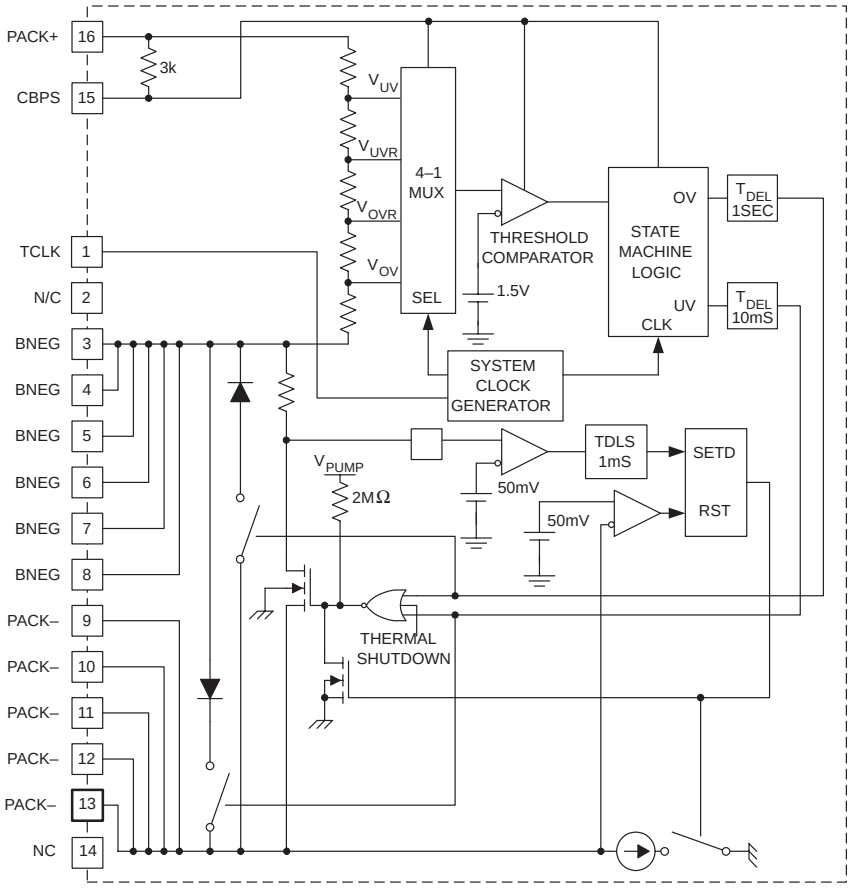


Figure 1. Detailed Block Diagram

battery voltage monitoring

The battery cell voltage is sampled every 8 ms by connecting a resistor divider across it and comparing the resulting voltage to a precision internal reference voltage. Under normal conditions (cell voltage is below overvoltage threshold and above undervoltage threshold), the UCC3952 consumes less than 10 μA of current and the internal MOSFET is fully turned on with the aid of a charge pump.

When the cell voltage falls below the undervoltage threshold for two consecutive samples, the IC disconnects the load from the battery pack and enters a super-low-power mode. The pack remains in this state until it detects the application of a charger, at which point charging is enabled. The requirement of two consecutive readings below the undervoltage threshold filters out momentary drops in cell voltage due to load transients, preventing nuisance trips.

If the cell voltage exceeds the overvoltage threshold for 1 second, charging is disabled; however, discharge current is still allowed. This feature of the IC is explained further in the *controlled charge/discharge mode* section of this document.

APPLICATION INFORMATION

overcurrent monitoring and protection

Discharge current is continuously monitored via an internal sense resistor. In the event of excessive current, an overcurrent condition is declared if the high current (over 3 A) persists for over 1 ms. This delay allows for charging of the system bypass capacitors without tripping the overcurrent protection. A 0.1-μF capacitor on the CBPS pin provides momentary holdup for the IC to assure proper operation in the event that a hard short suddenly pulls the cell voltage below the minimum operating voltage.

Once an overcurrent condition has been declared, the internal MOSFET turns off. To return the device to normal operation, the UCC3952 requires a load impedance greater than 7.5 MΩ across PACK+ to PACK–. This impedance is typically achieved by removing the battery pack from the system. At this point, the pack returns to its normal state of operation.

controlled charge/discharge mode

When the chip senses an overvoltage condition, it prevents any additional charging, but allows discharge. This is accomplished by activating a linear control loop, which controls the gate of the MOSFET based on the differential voltage across its drain-to-source terminals. The linear loop attempts to regulate the differential voltage across the MOSFET to 100 mV. When a light load is applied to the part, the loop adjusts the impedance of the MOSFET to maintain 100 mV across it. As the load increases, the impedance of the MOSFET is decreased to maintain the 100-mV control. At heavy loads (still below the overcurrent limit), the loop does not maintain regulation and drives the gate of the MOSFET to the battery voltage (not the charge-pump output voltage). The MOSFET $R_{DS(on)}$ in the overvoltage state is higher than RDS(on) during normal operation. The voltage drop (and associated power loss) across the internal MOSFET in this mode of operation is still significantly lower than the typical solution of two external back-to-back MOSFETs, where the body diode is conducting.

When the chip senses an undervoltage condition, it disconnects the load from the battery pack and shuts itself down to minimize current drain from the battery. Several circuits remain powered and detect placement of the battery pack into a charger. Once the charger presence is detected, the linear loop is activated and the chip allows charging current into the battery. This linear control mode of operation is in effect until the battery voltage reaches a level of V_{UVR} , at which time normal operation is resumed.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UCC3952DP-1	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3952DP-1G4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3952DP-2	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3952DP-2G4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3952DP-3	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3952DP-3G4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3952DP-4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3952DP-4G4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3952PW-1	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3952PW-1G4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3952PW-2	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3952PW-2G4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3952PW-3	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3952PW-3G4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3952PW-4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3952PW-4G4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3952PWTR-2	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3952PWTR-2G4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3952PWTR-3	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3952PWTR-3G4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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