TOSHIBA BI-DIRECTIONAL TRIODE THYRISTOR SILICON PLANAR TYPE

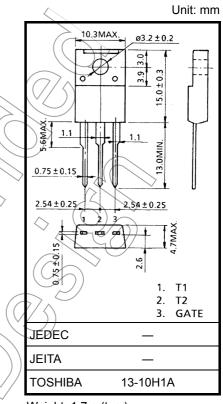
# SM8GZ47, SM8JZ47, SM8GZ47A, SM8JZ47A

# AC POWER CONTROL APPLICATIONS

- Repetitive Peak Off-State Voltage: VDRM = 400V, 600V
- R.M.S On-State Current: I<sub>T</sub> (RMS) = 8A
- High Commutating (dv / dt)
- Isolation Voltage: VISOL = 1500V AC

## **ABSOLUTE MAXIMUM RATINGS**

CHARACTERI	STIC	SYMBOL	RATING	UNIT
Repetitive Peak Off-State Voltage	SM8GZ47 SM8GZ47A	VDRM	400	
	SM8JZ47 SM8JZ47A	V DRM	600	
R.M.S On-State Curren (Full Sine Waveform Tc	•	I <sub>T (RMS)</sub>	8	> A
Peak One Cycle Surge ( Current (Non-Repetitive		ITSM	80 (50Hz) 88 (60Hz)	A
I <sup>2</sup> t Limit Value		l <sup>2</sup> t	32	(A <sup>2</sup> s
Critical Rate of Rise of C Current	0n−State (Note 1)	di / dt	50	A/µs
Peak Gate Power Dissip	ation	Рсм	5 <	w
Average Gate Power Dis	ssipation	PG(AV)	0.5	W
Peak Gate Voltage	6	Удм	10	V
Peak Gate Current		Úы	2	$\sim_{A}$
Junction Temperature		) Tj	-40~125))	°C
Storage Temperature Ra	ange	T <sub>stg</sub>	-40~125	°C
Isolation Voltage (AC, t =	= 1min.)	VISOL	1500	V



Weight: 1.7 g (typ.)

Note 1: di / dt Test Condition V<sub>DRM</sub> = 0.5×Rated

 $I_{TM} \leq 12A$   $t_{gw} \geq 10\mu s$   $t_{gr} \leq 250ns$   $i_{GP} = I_{GT} \times 2.0$ 

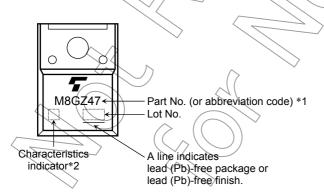
Note 2: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

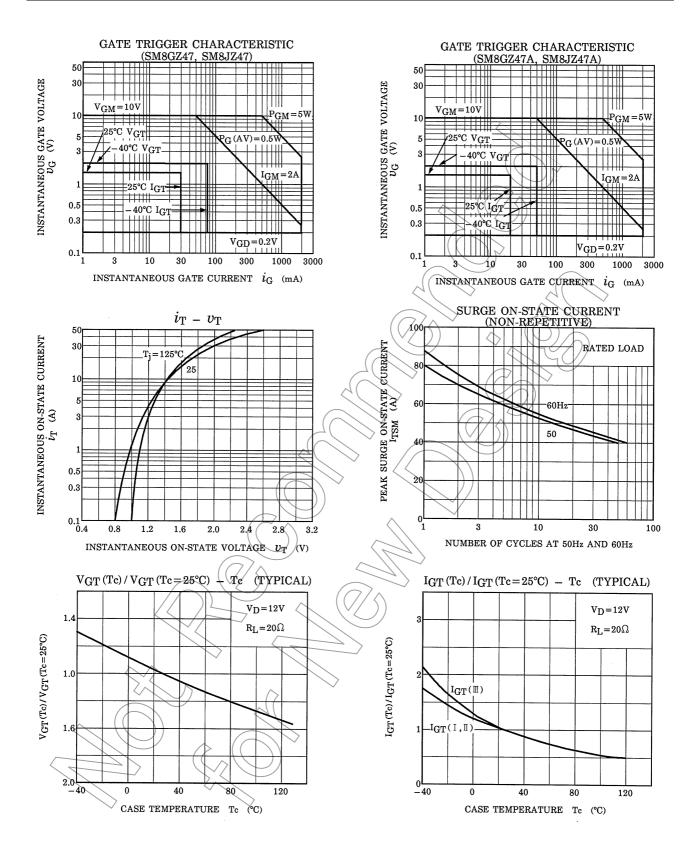
# ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION		MIN	TYP.	MAX	UNIT			
Repetitive Peak C Current	petitive Peak Off-State I <sub>DRM</sub> V <sub>DRM</sub> = Rated			_	_	20	μΑ				
			Ι			T2 (+), Gate (+)	1	_	1.5		
		П	V <sub>GT</sub> V <sub>D</sub> RL	V <sub>D</sub> = 12V	T2 (+), Gate (-)	X	—	1.5	v		
		III		$R_L = 20\Omega$	T2 (−), Gate (−)	(-)	4	1.5			
			IV			T2 (-), Gate (+)		2 –	_		
			Ι			T2 (+), Gate (+)	$\langle \uparrow \rangle$	—	30		
Gate Trigger Current	SM8GZ4		П	I <sub>GT</sub>	V <sub>D</sub> = 12V R <sub>L</sub> = 20Ω	T2 (+), Gate (-)		_	30	- mA	
	SM8JZ4	7	Ш			T2 (-), Gate (-)	- -	_	30		
			IV			T2 (-), Gate (+)					
			Ι			T2 (+), Gate (+)		$\mathcal{A}$	20		
	SM8GZ4		П			T2 (+), Gate (−)	- (	$\geq$	20		
	SM8JZ4	7A	III			(T2 (⁻), Gate (−)	+()	)	20	20	
			IV			T2 (-), Gate (+)	Ľ	K <del>(</del> )	/		
Peak On-State Voltage		V <sub>TM</sub>	ITM = 12A		1(		1.5	V			
Gate Non-Trigger Voltage		V <sub>GD</sub>	V <sub>D</sub> = Rated, Tc = 125°C		0.2	_		V			
Holding Current		IΗ	$V_{\rm D} = 12V_{\rm v} I_{\rm TM} = 1A$		Ŋ	_	50	mA			
Thermal Resistance		R <sub>th (j-c)</sub>	Junction to Case, AC		) —	—	3.6	°C / W			
Critical Rate of SMR Rise of Off-State SMR Voltage SMR		SM8GZ SM8JZ		dv Ldt	V <sub>DRM</sub> = Rated, T <sub>j</sub> = 125°C Exponential Rise		_	300		V / µs	
		SM8GZ SM8JZ					_	200			
Rise of Off-State SM8 Voltage at SM8		SM8GZ SM8JZ	(	(dv) dt) c	V <sub>DRM</sub> = 400V, 1 = 125°C		10	—	_	·V/µs	
		SM8G2 SM8JZ	/			Ă/ms	4	_	_		

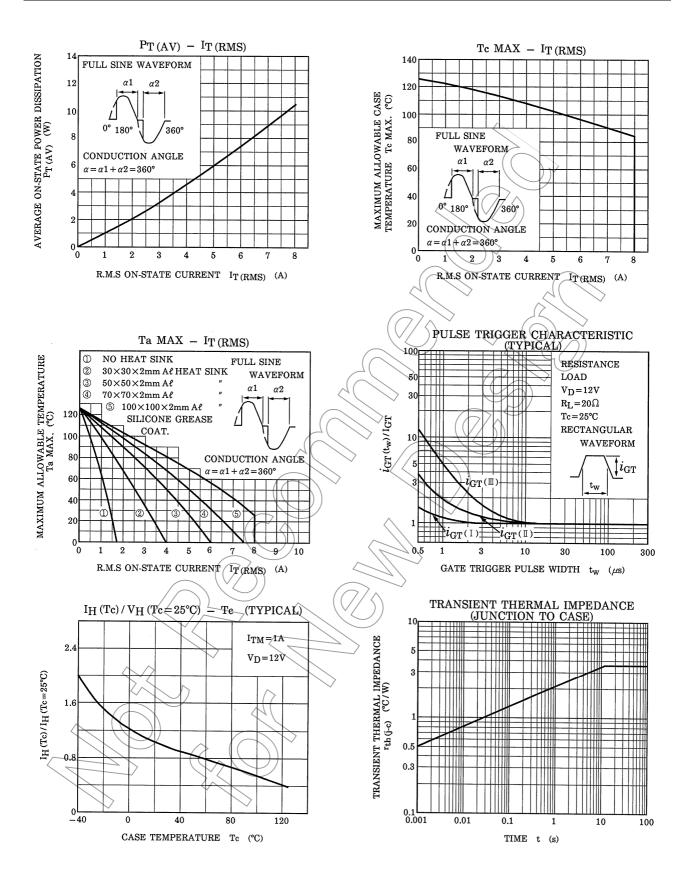
### MARKING



	Part No. (or abbreviation code)	Part No.
*1	M8GZ47	SM8GZ47, SM8GZ47A
	M8JZ47	SM8JZ47, SM8JZ47A
*2	Nothing	SM8GZ47, SM8JZ47
	А	SM8GZ47A, SM8JZ47A



# TOSHIBA



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