

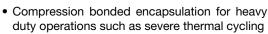
Phase Control Thyristors (Stud Version), 110 A



PRIMARY CHARACTERISTICS				
I _{T(AV)}	110 A			
V_{DRM}/V_{RRM}	400 V, 800 V, 1200 V, 1600 V			
V_{TM}	1.52 V			
I _{GT}	150 mA			
T_J	-40 °C to +125 °C			
Package	TO-94 (TO-209AC)			
Circuit configuration	Single SCR			

FEATURES

- · Center gate
- International standard case TO-94 (TO-209AC)





- Hermetic glass-metal case with ceramic insulator (Glass-metal seal over 1200 V)
- · Designed and qualified for industrial level
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

TYPICAL APPLICATIONS

- DC motor controls
- Controlled DC power supplies
- AC controllers

MAJOR RATINGS AND CHARACTERISTICS					
PARAMETER	TEST CONDITIONS	VALUES	UNITS		
1		110	A		
$I_{T(AV)}$	T _C	90	°C		
I _{T(RMS)}		175			
Ітѕм	50 Hz	2700	A		
	60 Hz	2830			
I ² t	50 Hz	36.4	kA ² s		
1-1	60 Hz	33.2	KA-S		
V _{DRM} /V _{RRM}		400 to 1600	V		
tq	Typical	100	μs		
T _J		-40 to +125	°C		

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS							
TYPE NUMBER	VOLTAGE CODE	V _{DRM} /V _{RRM} , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V _{RSM} , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	$\begin{aligned} I_{DRM}/I_{RRM} & \text{MAXIMUM AT} \\ & T_J = T_J & \text{MAXIMUM} \\ & \text{mA} \end{aligned}$			
	04	400	500				
VS-ST110S	08	800	900	20			
VS-511105	12	1200	1300	20			
	16	1600	1700				



ABSOLUTE MAXIMUM RATINGS						
PARAMETER	SYMBOL		TEST CON	IDITIONS	VALUES	UNITS
Maximum average on-state current at case temperature	I _{T(AV)}	180° conduction, half sine wave		110 90	A °C	
Maximum RMS on-state current	I _{T(RMS)}	DC at 85 °C	case temperat	ure	175	
	,	t = 10 ms	No voltage		2700	
Maximum peak, one-cycle		t = 8.3 ms	reapplied		2830	Α
non-repetitive surge current	I _{TSM}	t = 10 ms	100 % V _{RRM}		2270	
		t = 8.3 ms	reapplied	Sinusoidal half wave,	2380	
Maximum I ² t for fusing		t = 10 ms	No voltage	initial T _J = T _J maximum	36.4	kA ² s
	I ² t	t = 8.3 ms	reapplied		33.2	
Waxiiiluiiii Lioi lusiiig		t = 10 ms	100 % V _{RRM}		25.8	
		t = 8.3 ms	reapplied		23.5	
Maximum I ² √t for fusing	I ² √t	t = 0.1 to 10 ms, no voltage reapplied		364	kA²√s	
Low level value of threshold voltage	V _{T(TO)1}	(16.7 % x π	$x \ I_{T(AV)} < I < \pi \ x$	$I_{T(AV)}$), $T_J = T_J$ maximum	0.90	V
High level value of threshold voltage	V _{T(TO)2}	$(I > \pi \times I_{T(AV)}), T_J = T_J \text{ maximum}$		0.92	٧	
Low level value of on-state slope resistance	r _{t1}	(16.7 % x π x $I_{T(AV)} < I < \pi$ x $I_{T(AV)}$), $T_J = T_J$ maximum		1.79	mΩ	
High level value of on-state slope resistance	r _{t2}	$(I > \pi \times I_{T(AV)}), T_J = T_J \text{ maximum}$		1.81	1115.2	
Maximum on-state voltage	V_{TM}	$I_{pk} = 350 \text{ A}, T_J = T_J \text{ maximum}, t_p = 10 \text{ ms sine pulse}$		1.52	V	
Maximum holding current	I _H	T. = 25 °C	anada supply 1	2 V resistive lead	600	mA
Typical latching current	lι	T _J = 25 °C, anode supply 12 V resistive load		1000	111/4	

SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS	
Maximum non-repetitive rate of rise of turned-on current	dl/dt	Gate drive 20 V, 20 Ω , $t_r \le 1~\mu s$ $T_J = T_J$ maximum, anode voltage $\le 80~\%~V_{DRM}$	500	A/μs	
Typical delay time	t _d	Gate current 1 A, $dl_g/dt = 1 A/\mu s$ $V_d = 0.67 \% V_{DRM}$, $T_J = 25 °C$	2.0		
Typical turn-off time	t _q	I_{TM} = 100 A, T_J = T_J maximum, dI/dt = 10 A/ μ s, V_R = 50 V, dV/dt = 20 V/ μ s, gate 0 V 100 Ω , t_p = 500 μ s	100	μs	

BLOCKING					
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS	
Maximum critical rate of rise of off-state voltage	dV/dt	T _J = T _J maximum linear to 80 % rated V _{DRM}	500	V/µs	
Maximum peak reverse and off-state leakage current	I _{RRM} , I _{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	20	mA	



TRIGGERING						
PARAMETER	SYMBOL	TEST COMPLIANS		VALUES		
PARAMETER	STWIBUL	l Es	ST CONDITIONS	TYP.	MAX.	UNITS
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum,	$t_p \le 5 \text{ ms}$,	5	W
Maximum average gate power	P _{G(AV)}	$T_J = T_J$ maximum,	f = 50 Hz, d% = 50		1	VV
Maximum peak positive gate current	I _{GM}			2	.0	Α
Maximum peak positive gate voltage	+ V _{GM}	$T_J = T_J$ maximum,	$T_J = T_J$ maximum, $t_p \le 5$ ms		20	
Maximum peak negative gate voltage	- V _{GM}			5.0		V
		T _J = -40 °C		180	-	
DC gate current required to trigger	I _{GT}	T _J = 25 °C	Maximum required gate trigger/ current/voltage are the lowest	90	150	mA
		T _J = 125 °C		40	-	
		T _J = -40 °C	value which will trigger all units	2.9	-	
DC gate voltage required to trigger	V_{GT}	T _J = 25 °C	6 V anode to cathode applied	1.8	3.0	V
		T _J = 125 °C		1.2	-	
DC gate current not to trigger	I_{GD}		Maximum gate current/voltage	10		mA
DC gate voltage not to trigger	V _{GD}	$T_J = T_J \text{ maximum}$	not to trigger is the maximum value which will not trigger any unit with rated V _{DRM} anode to cathode applied	0.25		V

THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS	
Maximum operating junction temperature range	TJ		-40 to 125	°C	
Maximum storage temperature range	T _{Stg}		-40 to 150		
Maximum thermal resistance, junction to case	R _{thJC}	nJC DC operation		K/W	
Maximum thermal resistance, case to heatsink	R _{thCS}	Mounting surface, smooth, flat and greased	0.08	rv vv	
Mounting torque, ± 10 %		Non-lubricated threads	15.5 (137)	Nm	
Wounting torque, ± 10 %		Lubricated threads	14 (120)	(lbf \cdot in)	
Approximate weight			130	g	
Case style		See dimensions - link at the end of datasheet TO-94 (TO-209AC)		O-209AC)	

△R _{thJC} CONDUCTIO	N			
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDITIONS	UNITS
180°	0.035	0.025		
120°	0.041	0.042		
90°	0.052	0.056	$T_J = T_J$ maximum	K/W
60°	0.076	0.079		
30°	0.126	0.127		

Note

• The table above shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

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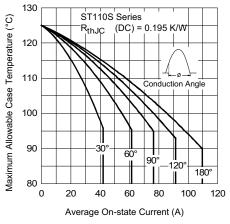


Fig. 1 - Current Ratings Characteristics

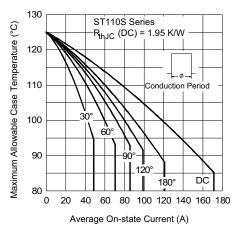


Fig. 2 - Current Ratings Characteristics

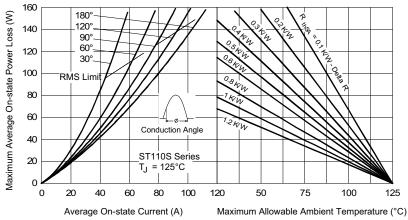


Fig. 3 - On-State Power Loss Characteristics

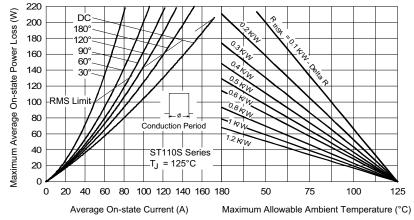


Fig. 4 - On-State Power Loss Characteristics



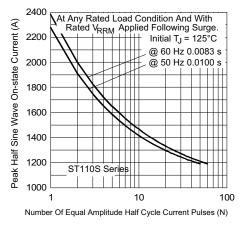


Fig. 5 - Maximum Non-Repetitive Surge Current

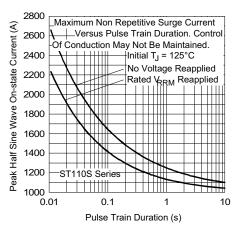


Fig. 6 - Maximum Non-Repetitive Surge Current

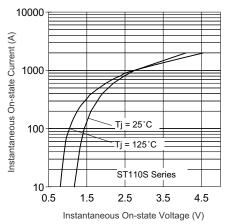


Fig. 7 - On-State Voltage Drop Characteristics

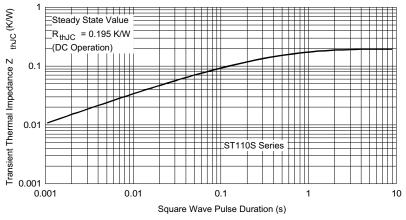


Fig. 8 - Thermal Impedance Z_{thJC} Characteristic

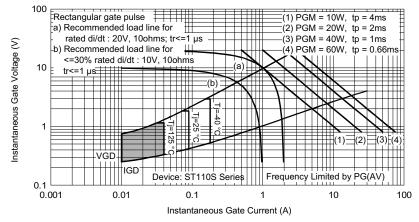
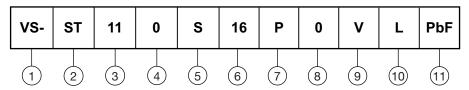


Fig. 9 - Gate Characteristics

ORDERING INFORMATION TABLE

Device code



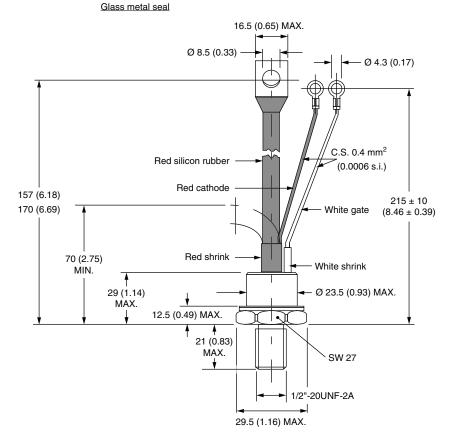
- Vishay Semiconductors product
- **Thyristor**
- Essential part marking
- 0 = converter grade
- S = compression bonding stud
- 3 4 5 6 Voltage code x 100 = V_{RRM} (see Voltage Ratings table)
- P = stud base 20UNF threads
- 0 = eyelet terminals (gate and auxiliary cathode leads)
 - 1 = fast-on terminals (gate and auxiliary cathode leads)
 - 2 = flag terminals (for cathode and gate terminals)
- 9 • V = glass-metal seal (only up to 1200 V)
 - None = ceramic housing (over 1200 V)
- 10 Critical dV/dt:
 - None = 500 V/µs (standard value)
 - L = 1000 V/µs (special selection)
- 11 None = standard production
 - PbF = lead (Pb)-free

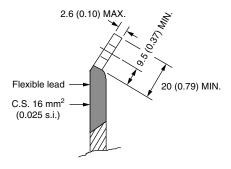
LINKS TO RELAT	TED DOCUMENTS
Dimensions	www.vishay.com/doc?95078

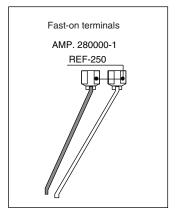


TO-209AC (TO-94) for ST110S Series

DIMENSIONS in millimeters (inches)







Document Number: 95078 Revision: 23-Sep-08

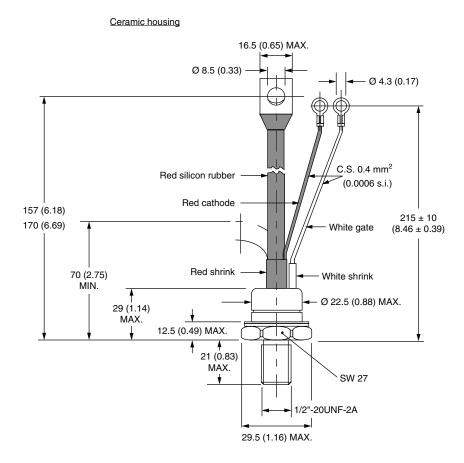
Outline Dimensions

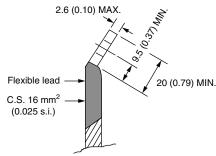
Vishay Semiconductors

TO-209AC (TO-94) for ST110S Series



DIMENSIONS in millimeters (inches)





Document Number: 95078 Revision: 23-Sep-08

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