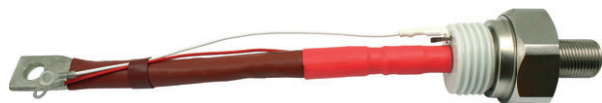


Inverter Grade Thyristors (Stud Version), 330 A


TO-118 (TO-209AE)

RoHS
COMPLIANT

FEATURES

- Center amplifying gate
- High surge current capability
- Low thermal impedance
- High speed performance
- Compression bonding
- Designed and qualified for industrial level
- Material categorization: for definitions of compliance please see www.vishay.com/doc?999912

TYPICAL APPLICATIONS

- Inverters
- Choppers
- Induction heating
- All types of force-commutated converters

PRIMARY CHARACTERISTICS	
$I_{T(AV)}$	330 A
V_{DRM}/V_{RRM}	400 V, 800 V
V_{TM}	1.96 V
I_{TSM} at 50 Hz	11 000 A
I_{TSM} at 60 Hz	11 520 A
I_{GT}	200 mA
T_J	-40 °C to +125 °C
T_C	75 °C
Package	TO-118 (TO-209AE)
Circuit configuration	Single SCR

MAJOR RATINGS AND CHARACTERISTICS			
PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		330	A
	T_C	75	°C
$I_{T(RMS)}$		518	A
I_{TSM}	50 Hz	11 000	
	60 Hz	11 520	
I^2t	50 Hz	605	kA ² s
	60 Hz	550	
V_{DRM}/V_{RRM}		400 to 800	V
t_q		15	μs
T_J		-40 to +125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM} , MAXIMUM REPETITIVE PEAK VOLTAGE V	V_{RSM} , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I_{DRM}/I_{RRM} MAXIMUM AT $T_J = T_J$ MAXIMUM mA
VS-ST333S	04	400	500	50
	08	800	900	

**CURRENT CARRYING CAPABILITY**

FREQUENCY							UNITS
50 Hz	840	600	1280	1040	5430	4350	A
400 Hz	650	450	1280	910	2150	1560	
1000 Hz	430	230	1090	730	1080	720	
2500 Hz	140	60	490	250	400	190	
Recovery voltage V _R	50		50		50		V
Voltage before turn-on V _D	V _{DRM}		V _{DRM}		V _{DRM}		
Rise of on-state current di/dt	50		-		-		A/μs
Case temperature	50	75	50	75	50	75	°C
Equivalent values for RC circuit	10/0.47		10/0.47		10/0.47		Ω/μF

ON-STATE CONDUCTION

PARAMETER	SYMBOL	TEST CONDITIONS				VALUES	UNITS
Maximum average on-state current at case temperature	I _{T(AV)}	180° conduction, half sine wave				330	A
						75	°C
Maximum RMS on-state current	I _{T(RMS)}	DC at 63 °C case temperature				518	A
Maximum peak, one half cycle, non-repetitive surge current	I _{TSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial T _J = T _J maximum	11 000		
		t = 8.3 ms			11 520		
		t = 10 ms	100 % V _{RRM} reapplied		9250		
		t = 8.3 ms			9700		
Maximum I ² t for fusing	I ² t	t = 10 ms	No voltage reapplied			605	kA ² s
		t = 8.3 ms				550	
		t = 10 ms	100 % V _{RRM} reapplied			430	
		t = 8.3 ms				390	
Maximum I ² √t for fusing	I ² √t	t = 0.1 ms to 10 ms, no voltage reapplied				6050	kA ² √s
Maximum peak on-state voltage	V _{TM}	I _{TM} = 1810 A, T _J = T _J maximum, t _p = 10 ms sine wave pulse				1.96	V
Low level value of threshold voltage	V _{T(TO)1}	(16.7 % × π × I _{T(AV)}) < I < π × I _{T(AV)} , T _J = T _J maximum				0.91	
High level value of threshold voltage	V _{T(TO)2}	(I > π × I _{T(AV)}), T _J = T _J maximum				0.92	
Low level value of forward slope resistance	r _{t1}	(16.7 % × π × I _{T(AV)}) < I < π × I _{T(AV)} , T _J = T _J maximum				0.58	mΩ
High level value of forward slope resistance	r _{t2}	(I > π × I _{T(AV)}), T _J = T _J maximum				0.58	
Maximum holding current	I _H	T _J = 25 °C, I _T > 30 A				600	mA
Typical latching current	I _L	T _J = 25 °C, V _A = 12 V, R _a = 6 Ω, I _G = 1 A				1000	

SWITCHING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	di/dt	$T_J = T_J$ maximum, $V_{DRM} = \text{Rated } V_{DRM}$ $I_{TM} = 2 \times di/dt$	1000	A/μs
Typical delay time	t_d	$T_J = 25$ °C, $V_{DM} = \text{Rated } V_{DRM}$, $I_{TM} = 50$ A DC, $t_p = 1$ μs Resistive load, gate pulse: 10 V, 5 Ω source	1.0	μs
Maximum turn-off time	t_q	$T_J = T_J$ maximum, $I_{TM} = 550$ A, commutating $di/dt = 40$ A/μs $V_R = 50$ V, $t_p = 500$ μs, $dV/dt = 200$ V/μs	15	

**BLOCKING**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, linear to 80 % V_{DRM} , higher value available on request	500	V/ μ s
Maximum peak reverse and off-state leakage current	I_{RRM} , I_{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	50	mA

TRIGGERING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $f = 50$ Hz, $d\% = 50$	60	W
Maximum average gate power	$P_{G(AV)}$		10	
Maximum peak positive gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms	10	A
Maximum peak positive gate voltage	$+V_{GM}$		20	V
Maximum peak negative gate voltage	$-V_{GM}$		5	
Maximum DC gate current required to trigger	I_{GT}	$T_J = 25$ °C, $V_A = 12$ V, $R_a = 6$ Ω	200	mA
Maximum DC gate voltage required to trigger	V_{GT}		3	V
Maximum DC gate current not to trigger	I_{GD}	$T_J = T_J$ maximum, rated V_{DRM} applied	20	mA
Maximum DC gate voltage not to trigger	V_{GD}		0.25	V

THERMAL AND MECHANICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum operating junction temperature range	T_J		-40 to +125	°C
Maximum storage temperature range	T_{Stg}		-40 to +150	
Maximum thermal resistance, junction to case	R_{thJC}	DC operation	0.10	K/W
Maximum thermal resistance, case to heatsink	R_{thCS}	Mounting surface, smooth, flat and greased	0.03	
Mounting torque, ± 10 %		Non-lubricated threads	48.5 (425)	N · m (lbf · in)
Approximate weight			535	g
Case style		See dimensions - link at the end of datasheet	TO-118 (TO-209AE)	

 ΔR_{thJ-hs} CONDUCTION

CONDUCTION ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDITIONS	UNITS
180°	0.011	0.008	$T_J = T_J$ maximum	K/W
120°	0.013	0.014		
90°	0.017	0.018		
60°	0.025	0.026		
30°	0.041	0.042		

Note

- The table above shows the increment of thermal resistance R_{thJ-hs} when devices operate at different conduction angles than DC

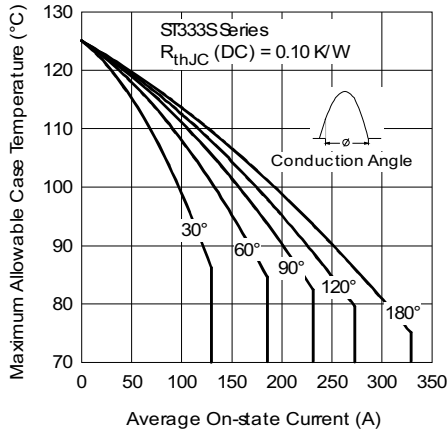


Fig. 1 - Current Ratings Characteristics

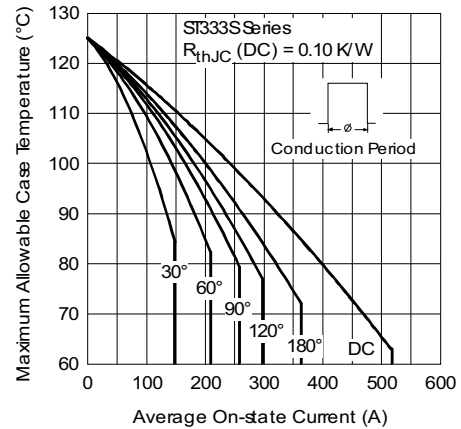


Fig. 2 - Current Ratings Characteristics

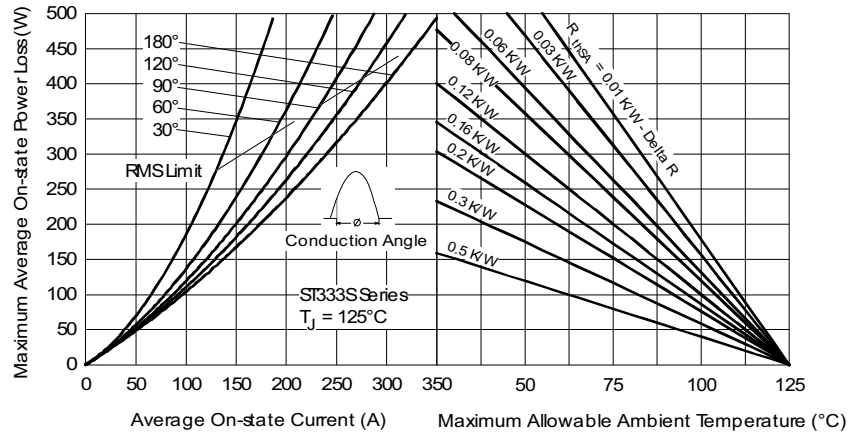


Fig. 3 - On-State Power Loss Characteristics

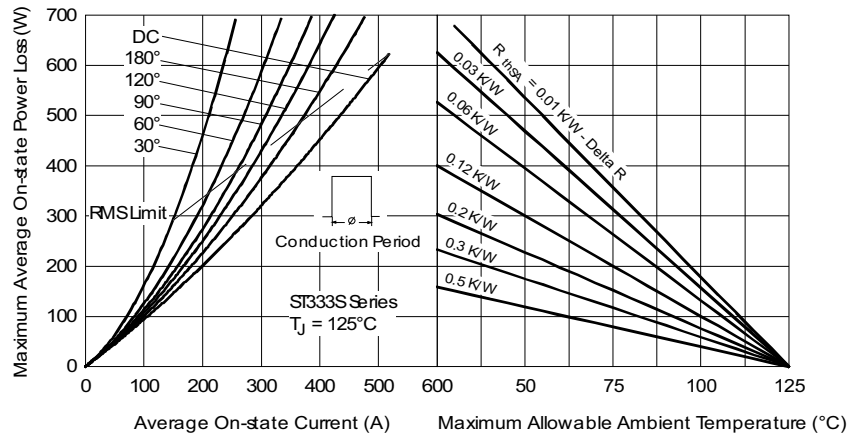


Fig. 4 - On-State Power Loss Characteristics

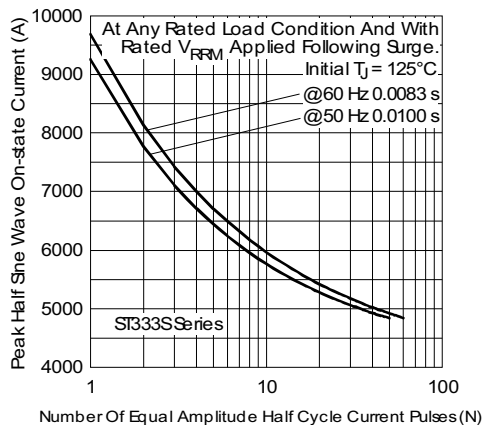


Fig. 5 - Maximum Non-Repetitive Surge Current

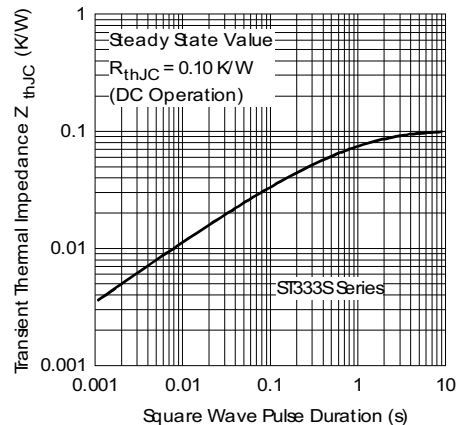


Fig. 8 - Thermal Impedance Z_{thJC} Characteristics

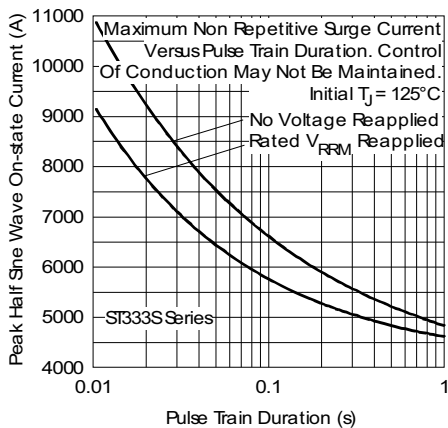


Fig. 6 - Maximum Non-Repetitive Surge Current

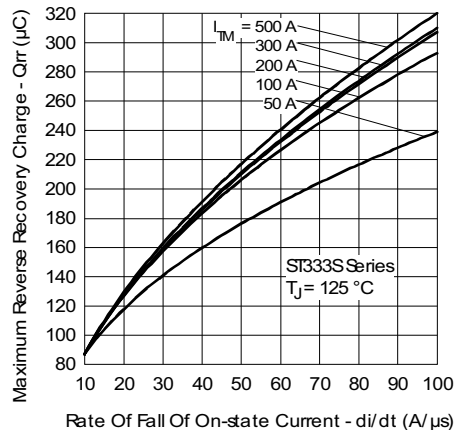


Fig. 9 - Reverse Recovered Charge Characteristics

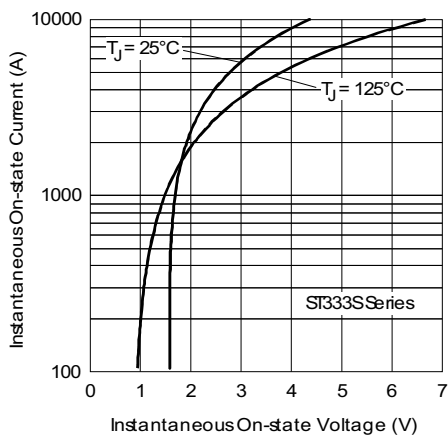


Fig. 7 - On-State Voltage Drop Characteristics

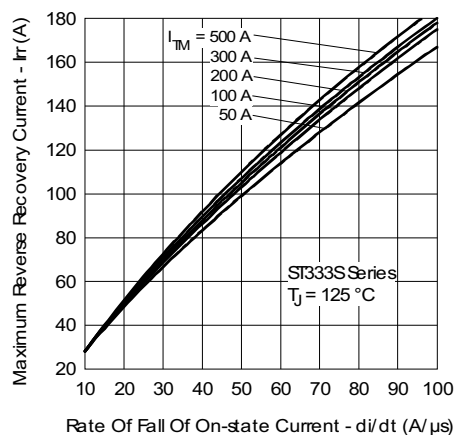


Fig. 10 - Reverse Recovery Current Characteristics

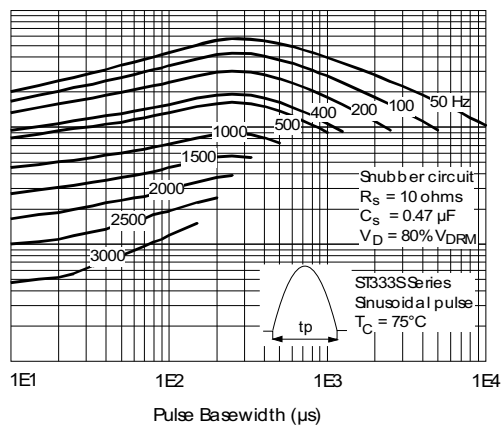
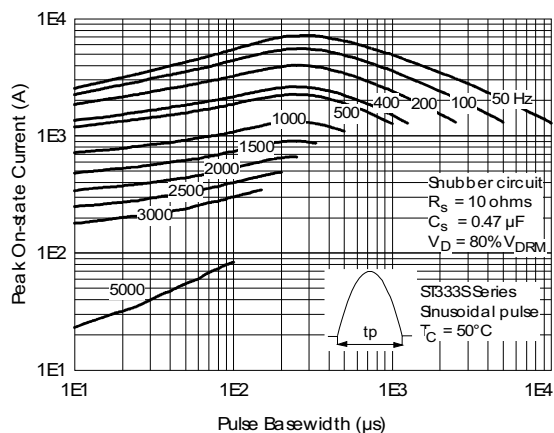


Fig. 11 - Frequency Characteristics

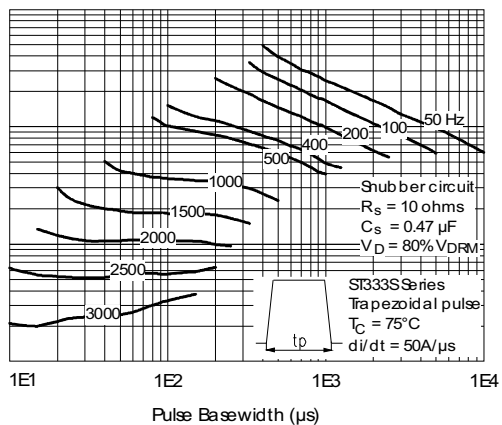
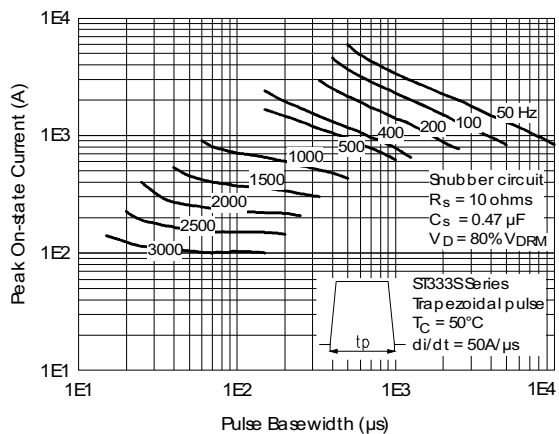


Fig. 12 - Frequency Characteristics

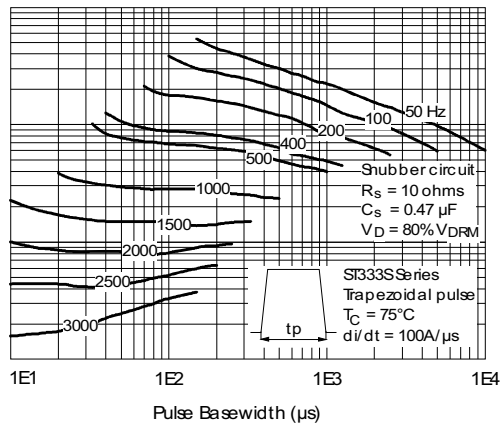
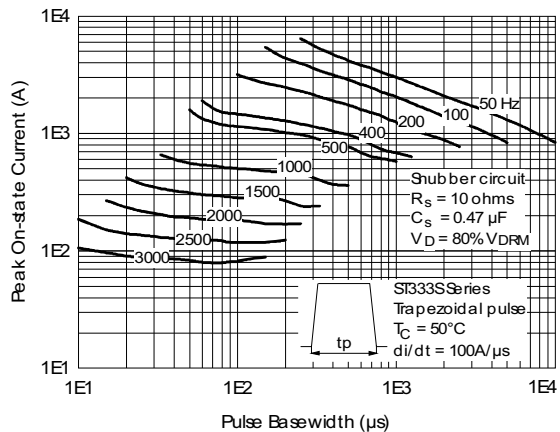


Fig. 13 - Frequency Characteristics

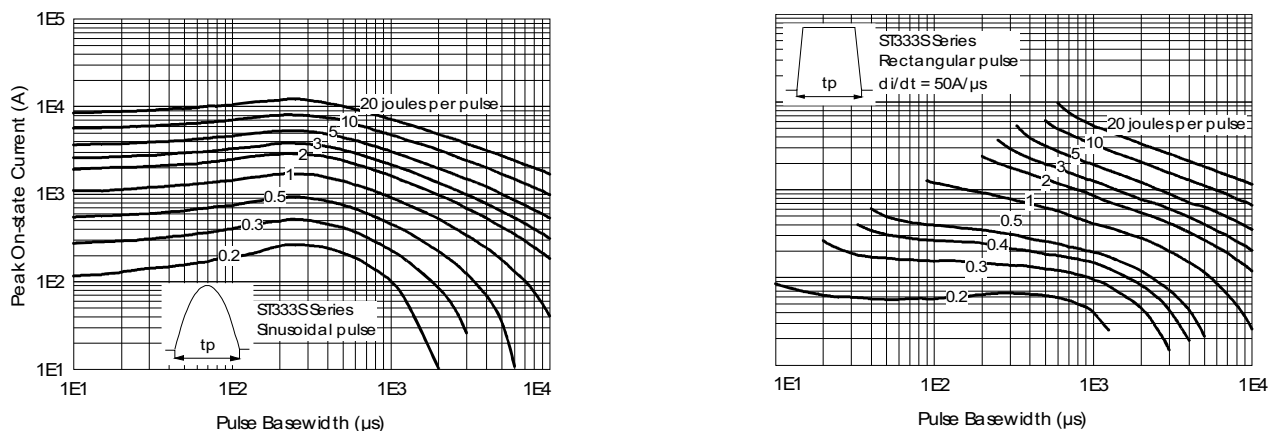


Fig. 14 - Maximum On-State Energy Power Loss Characteristics

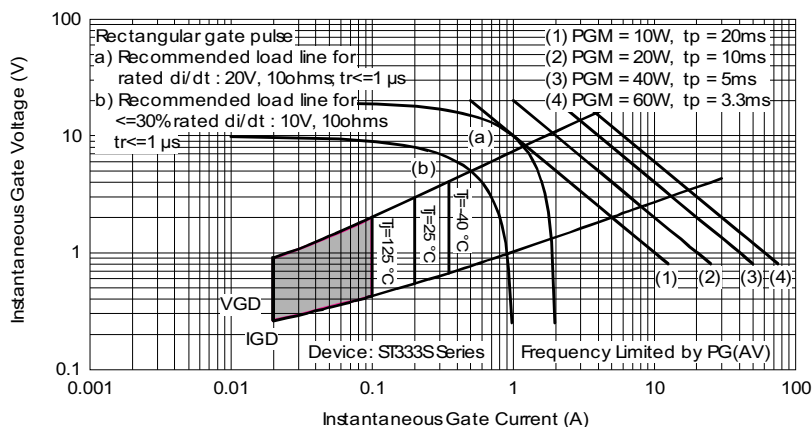


Fig. 15 - Gate Characteristics



ORDERING INFORMATION TABLE

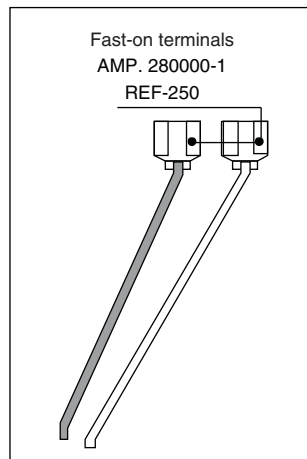
Device code	VS-	ST	33	3	S	08	P	F	L	0	P
	1	2	3	4	5	6	7	8	9	10	11

- 1** - Vishay Semiconductors product
- 2** - Thyristor
- 3** - Essential part number
- 4** - 3 = fast turn-off
- 5** - S = compression bonding stud
- 6** - Voltage code x 100 = V_{RRM}
(see Voltage Ratings table)
- 7** - P = stud base 3/4" 16UNF-2A / M = metric device
- 8** - Reapplied dV/dt code (for t_q test condition) F = 200 V/ μ s
- 9** - t_q code (L = 15 μ s) M = 12 μ s
- 10** - 0 = eyelet terminals
(gate and auxiliary cathode leads)
1 = fast-on terminals
(gate and auxiliary cathode leads)
- 11** - None = standard production
P = lead (Pb)-free

Note: For metric device M24 x 1.5 contact factory

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95080

DIMENSIONS in millimeters (inches)



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