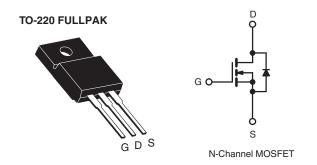


Vishay Siliconix

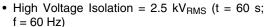
### **Power MOSFET**

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	60			
$R_{DS(on)}\left(\Omega\right)$	V <sub>GS</sub> = 5.0 V	0.050		
Q <sub>g</sub> (Max.) (nC)	35			
Q <sub>gs</sub> (nC)	7.1			
Q <sub>gd</sub> (nC)	25			
Configuration	Single			



#### **FEATURES**

· Isolated Package





- Sink to Lead Creepage Distance 4.8 mm
- · Logic-Level Gate Drive
- R<sub>DS(on)</sub> Specified at V<sub>GS</sub> = 4 V and 5 V
- · Fast Switching
- · Ease of paralleling
- · Lead (Pb)-free

#### **DESCRIPTION**

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 FULLPAK eliminates the need for additional insulating hardware in commercial-industrial applications. The molding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The FULLPAK is mounted to a heatsink using a single clip or by a single screw fixing.

ORDERING INFORMATION			
Package	TO-220 FULLPAK		
Lead (Pb)-free	IRLIZ34GPbF		
	SiHLIZ34G-E3		
SnPb	IRLIZ34G		
	SiHLIZ34G		

<b>ABSOLUTE MAXIMUM RATINGS</b> $T_C = 25$ °C, unless otherwise noted						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			$V_{DS}$	60	V	
Gate-Source Voltage			$V_{GS}$	± 10	\ \ \	
Continuous Drain Current	$V_{GS}$ at 5.0 V $\frac{T_C}{T_C}$	T <sub>C</sub> = 25 °C	- I <sub>D</sub>	20	А	
		T <sub>C</sub> = 100 °C		14		
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	80		
Linear Derating Factor				0.28	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	200	mJ	
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		$P_{D}$	42	W	
Peak Diode Recovery dV/dt <sup>c</sup>			dV/dt	4.5	V/ns	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 175	°C		
Soldering Recommendations (Peak Temperature)	for 10 s			300 <sup>d</sup>	1	
Mounting Torque	6 22 or l	6-32 or M3 screw		10	lbf ⋅ in	
	0-32 OF MIS SCIEW			1.1	N⋅m	

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b.  $V_{DD} = 25 \text{ V}$ , starting  $T_J = 25 \,^{\circ}\text{C}$ ,  $L = 583 \, \mu\text{H}$ ,  $R_G = 25 \, \Omega$ ,  $I_{AS} = 20 \, \text{A}$  (see fig. 12c). c.  $I_{SD} \le 30 \, \text{A}$ ,  $dI/dt \le 200 \, \text{A}/\mu\text{s}$ ,  $V_{DD} \le V_{DS}$ ,  $T_J \le 175 \,^{\circ}\text{C}$ .
- d. 1.6 mm from case.

<sup>\*</sup> Pb containing terminations are not RoHS compliant, exemptions may apply

# IRLIZ34G, SiHLIZ34G

# Vishay Siliconix



THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R <sub>thJA</sub>	-	65	°C/W	
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	-	3.6	C/VV	

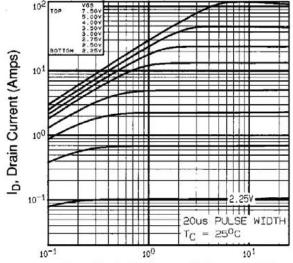
PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> =	60	-	-	V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Referenc	e to 25 °C, I <sub>D</sub> = 1 mA	-	0.070	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$		-	2.0	٧
Gate-Source Leakage	I <sub>GSS</sub>	,	V <sub>GS</sub> = ± 10 V		-	± 100	nA
Zero Gate Voltage Drain Current	1	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V		-	-	25	μΑ
Zero Gate Voltage Drain Gunerit	I <sub>DSS</sub>	V <sub>DS</sub> = 48 V,	V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C			250	μΑ
Drain-Source On-State Resistance	_	V <sub>GS</sub> = 5.0 V	I <sub>D</sub> = 12 A <sup>b</sup>	-	-	0.050	Ω
	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.0 V	$I_D = 10 A^b$	-	-	0.070	
Forward Transconductance	9 <sub>fs</sub>	V <sub>DS</sub> = 25 V, I <sub>D</sub> = 12 A <sup>b</sup>		12	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	$V_{GS} = 0 \text{ V},$ $V_{DS} = 25 \text{ V},$ $f = 1.0 \text{ MHz, see fig. 5}$ $f = 1 \text{ MHz}$		-	1600	-	pF
Output Capacitance	C <sub>oss</sub>			-	660	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	170	-	
Drain to Sink Capacitance	С			-	12	-	
Total Gate Charge	Qg			-	-	35	nC
Gate-Source Charge	Q <sub>gs</sub>	V <sub>GS</sub> = 5.0 V	$I_D = 30 \text{ A}, V_{DS} = 48 \text{ V},$ see fig. 6 and 13 <sup>b</sup>	-	-	7.1	
Gate-Drain Charge	$Q_{gd}$		goo ng. o ana 10	-	-	25	
Turn-On Delay Time	t <sub>d(on)</sub>		'		14	-	ns ns
Rise Time	t <sub>r</sub>	$V_{DD} = 30 \text{ V}, I_{D} = 30 \text{ A},$ $R_{G} = 6.0 \Omega, R_{D} = 1.0 \Omega,$ see fig. $10^{b}$		-	170	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	30	-	
Fall Time	t <sub>f</sub>			-	56	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	
Internal Source Inductance	L <sub>S</sub>			-	7.5	-	- nH
Drain-Source Body Diode Characteristic	s	•		•			
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	20	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	80	A
Body Diode Voltage	$V_{SD}$	$T_J = 25$ °C, $I_S = 20$ A, $V_{GS} = 0$ V <sup>b</sup>		-	-	1.6	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T 25 °C 1	= 30 A dl/dt = 100 A/v-ah	-	90	180	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	$T_J = 25  ^{\circ}\text{C}, I_F = 30  \text{A}, dI/dt = 100  \text{A}/\mu \text{s}^{\text{b}}$		-	0.65	1.3	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic tu	-on is don	ninated by	l a and l	-1	

### Notes

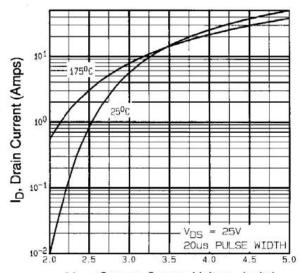
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq$  300  $\mu$ s; duty cycle  $\leq$  2 %.



### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



V<sub>DS</sub>, Drain-to-Source Voltage (volts) Fig. 1 - Typical Output Characteristics, T<sub>C</sub> = 25 °C



V<sub>GS</sub>, Gate-to-Source Voltage (volts) Fig. 3 - Typical Transfer Characteristics

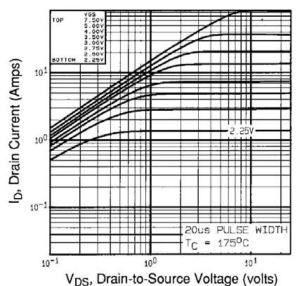


Fig. 2 - Typical Output Characteristics, T<sub>C</sub> = 175 °C

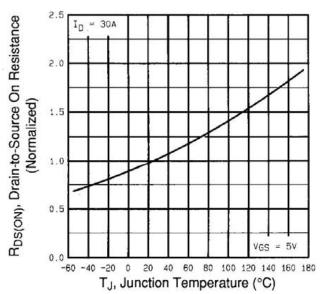


Fig. 4 - Normalized On-Resistance vs. Temperature

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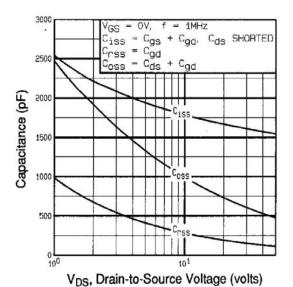


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

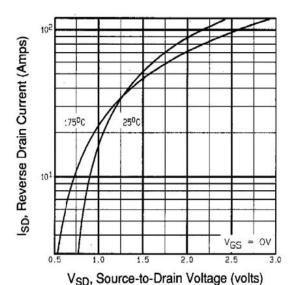


Fig. 7 - Typical Source-Drain Diode Forward Voltage

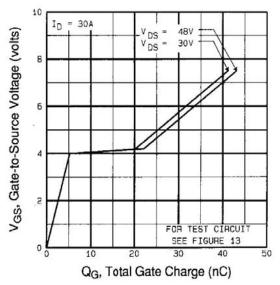


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

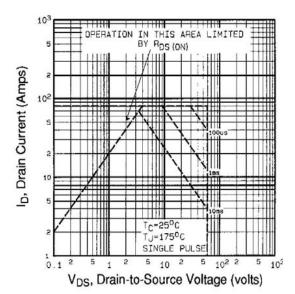


Fig. 8 - Maximum Safe Operating Area



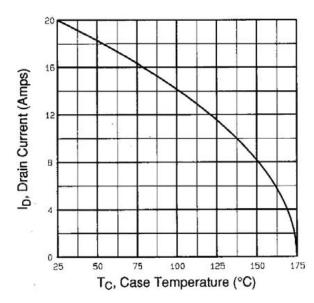


Fig. 9 - Maximum Drain Current vs. Case Temperature

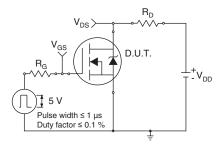


Fig. 10a - Switching Time Test Circuit

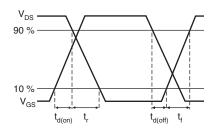


Fig. 10b - Switching Time Waveforms

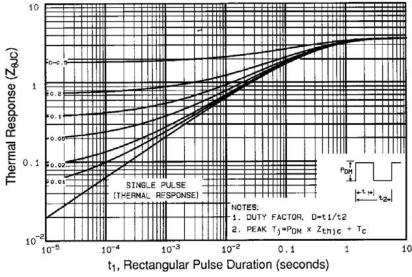


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

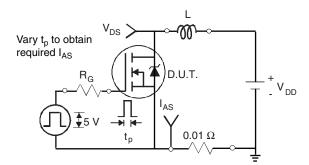


Fig. 12a - Unclamped Inductive Test Circuit

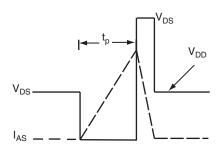
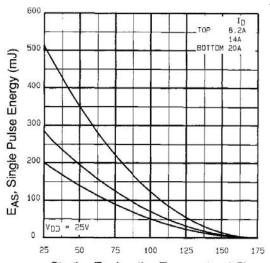


Fig. 12b - Unclamped Inductive Waveforms

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Starting T<sub>J</sub>, Junction Temperature(°C)
Fig. 12c - Maximum Avalanche Energy vs. Drain Current

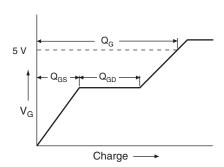


Fig. 13a - Basic Gate Charge Waveform

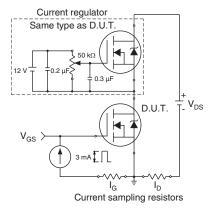
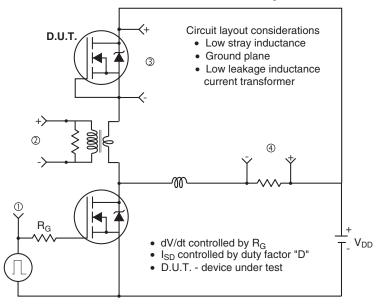
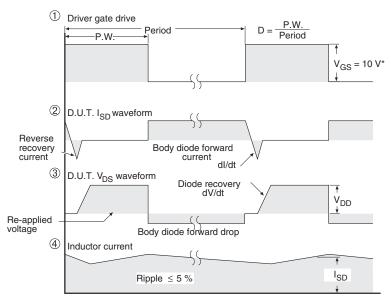


Fig. 13b - Gate Charge Test Circuit



## Peak Diode Recovery dV/dt Test Circuit





\* V<sub>GS</sub> = 5 V for logic level devices and 3 V drive devices

Fig. 14 - For N-Channel

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