

P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
- 20	0.019 at $V_{GS} = - 4.5$ V	- 11.4
	0.025 at $V_{GS} = - 2.5$ V	- 9.9
	0.034 at $V_{GS} = - 1.8$ V	- 8.5

FEATURES

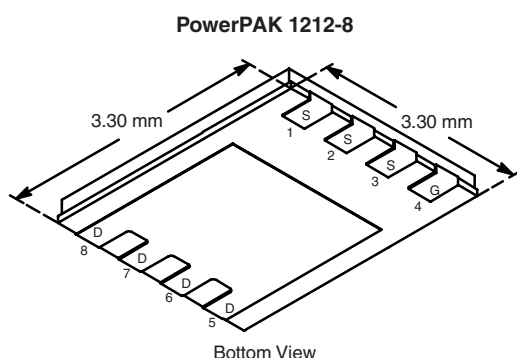
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFET: 1.8 V Rated
- New PowerPAK® Package
 - Low Thermal Resistance, R_{thJC}
 - Low 1.07 mm Profile



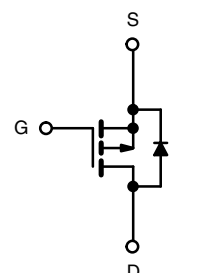
RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Load Switch



Ordering Information: Si7411DN-T1-E3 (Lead (Pb)-free)
Si7411DN-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

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Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V _{DS}	- 20		V
Gate-Source Voltage		V _{GS}	± 8		
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	- 11.4	- 7.5	A
	T _A = 85 °C		- 8.2	- 5.4	
Pulsed Drain Current		I _{DM}	- 30		
Continuous Source Current (Diode Conduction) ^a		I _S	- 3	- 1.3	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	3.6	1.5	W
	T _A = 85 °C		1.9	0.8	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{b, c}			260		

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	28	35	$^\circ\text{C/W}$
		65	81	
Maximum Junction-to-Case	R_{thJC}	2.9	3.8	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

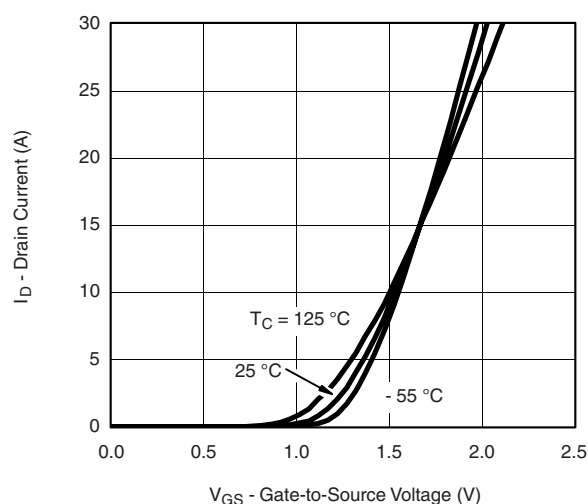
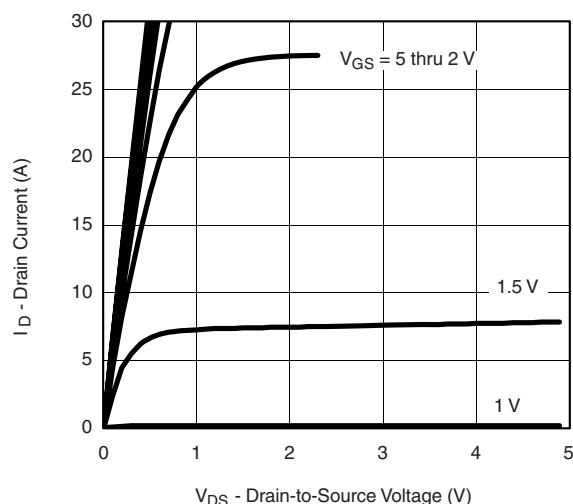
SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -300\ \mu\text{A}$	-0.4		-1.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 8\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\ \text{V}$, $V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -20\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 85^\circ\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\ \text{V}$, $V_{GS} = -4.5\ \text{V}$	-30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\ \text{V}$, $I_D = -11.4\ \text{A}$		0.015	0.019	Ω
		$V_{GS} = -2.5\ \text{V}$, $I_D = -9.9\ \text{A}$		0.020	0.025	
		$V_{GS} = -1.8\ \text{V}$, $I_D = -2.9\ \text{A}$		0.027	0.034	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\ \text{V}$, $I_D = -11.4\ \text{A}$		35		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -3.0\ \text{A}$, $V_{GS} = 0\ \text{V}$		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -10\ \text{V}$, $V_{GS} = -4.5\ \text{V}$, $I_D = -11.4\ \text{A}$		27	41	nC
Gate-Source Charge	Q_{gs}			3.9		
Gate-Drain Charge	Q_{gd}			7		
Gate Resistance	R_g	$f = 1\ \text{MHz}$		5		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\ \text{V}$, $R_L = 10\ \Omega$ $I_D \approx -1\ \text{A}$, $V_{GEN} = -4.5\ \text{V}$, $R_g = 6\ \Omega$		23	35	ns
Rise Time	t_r			45	70	
Turn-Off Delay Time	$t_{d(off)}$			135	200	
Fall Time	t_f			70	105	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -3.2\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		29	50	

Notes:

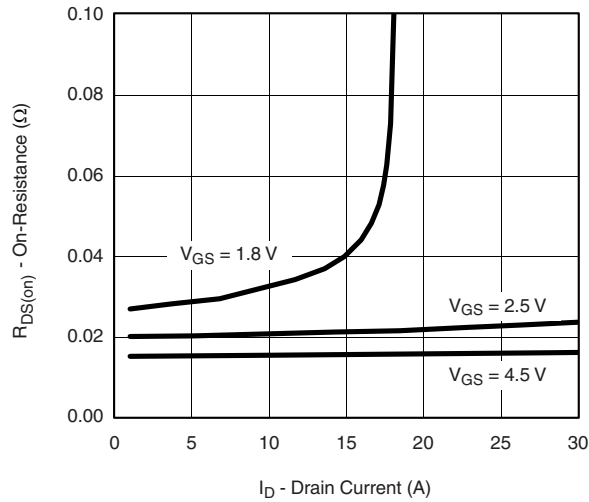
a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

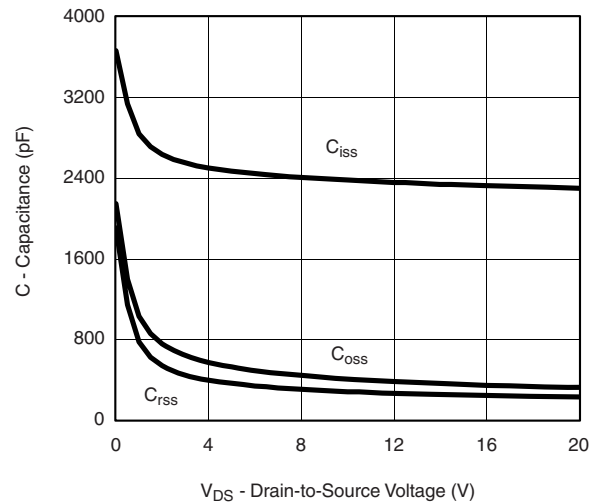
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25°C , unless otherwise noted

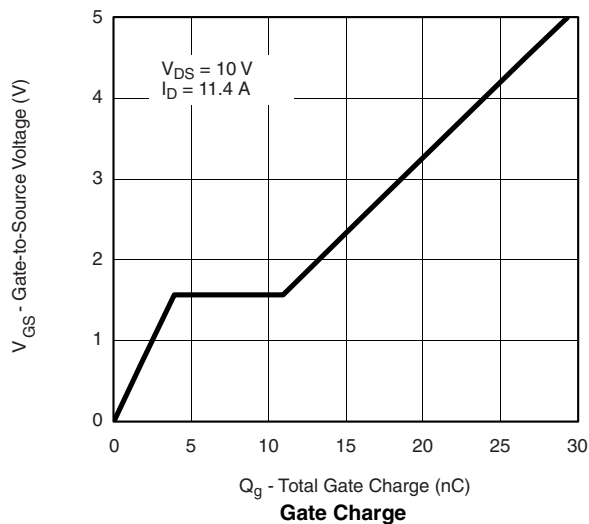
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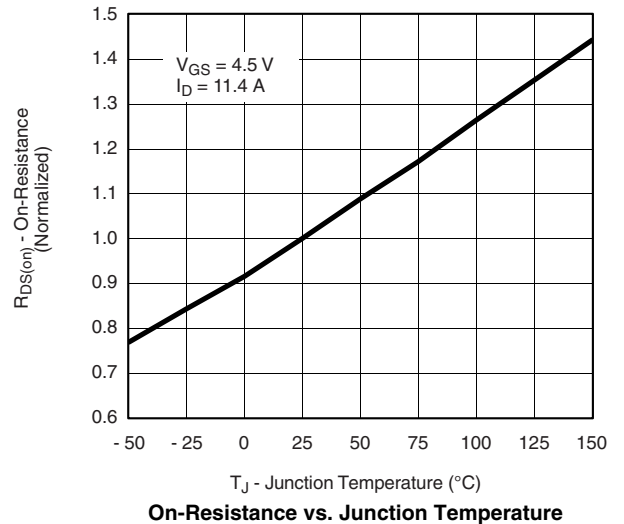
On-Resistance vs. Drain Current



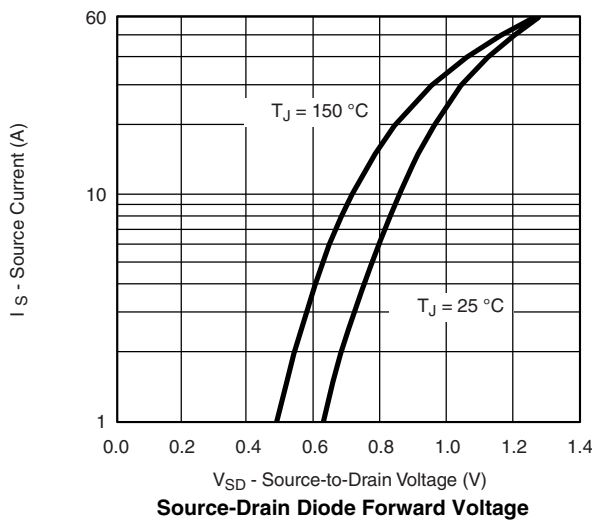
Capacitance



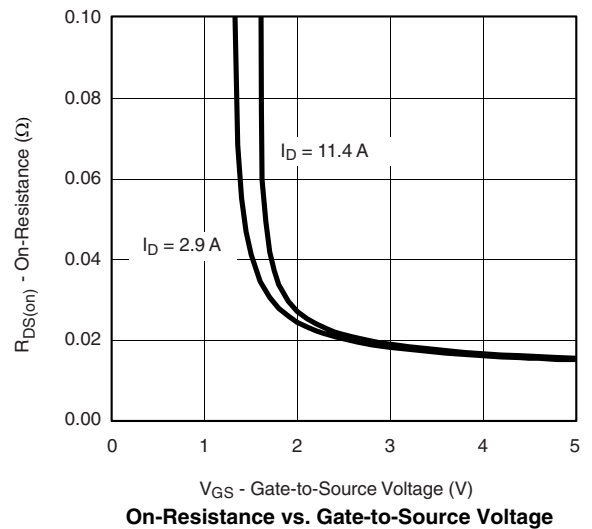
Gate Charge



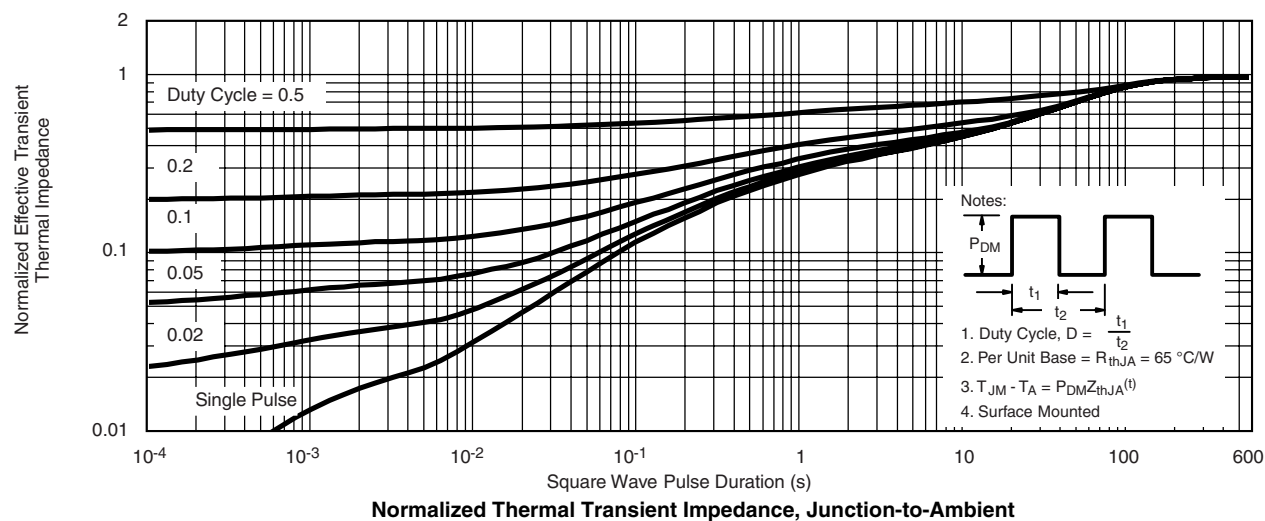
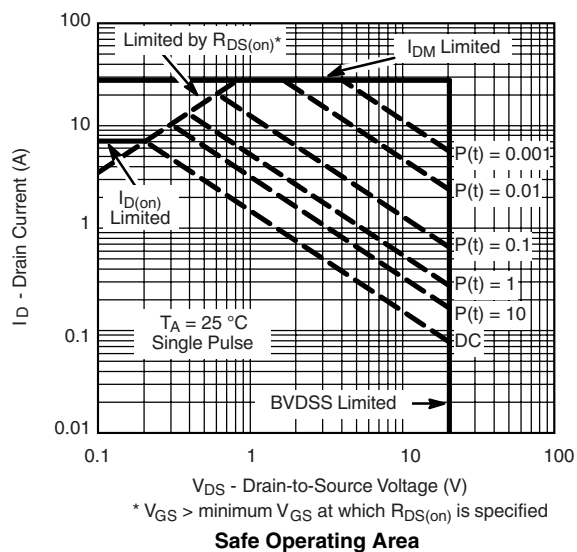
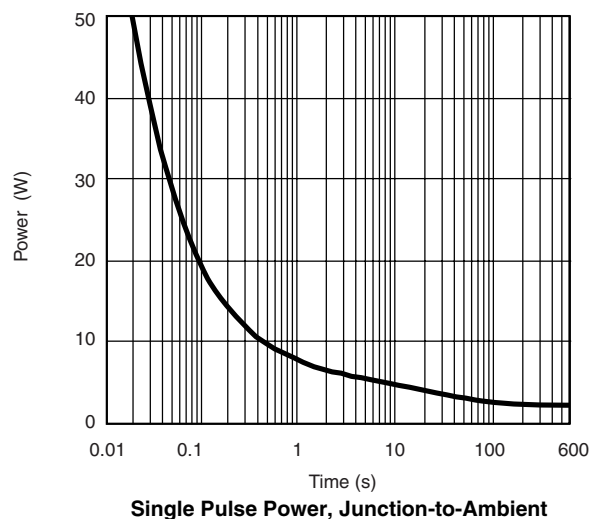
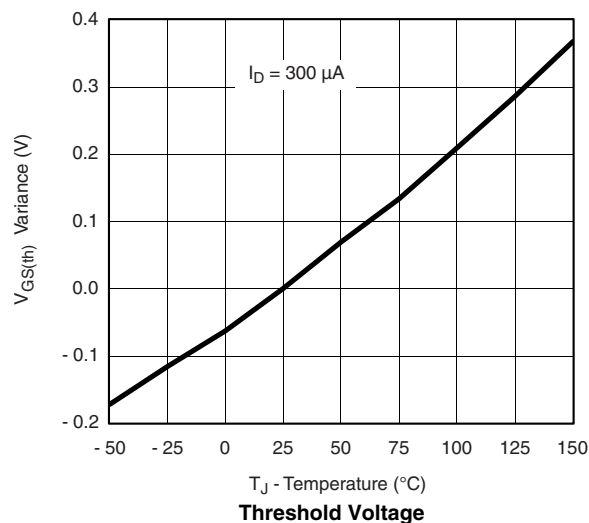
On-Resistance vs. Junction Temperature



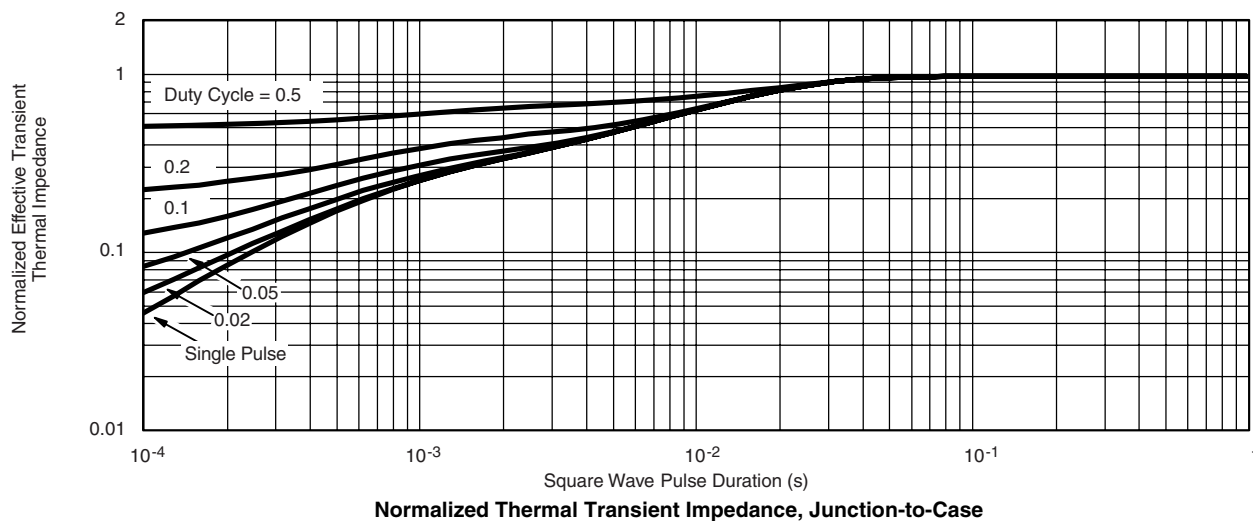
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

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