

Bi-Directional N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY

V_{S1S2} (V)	$R_{S1S2(on)}$ (Ω)	I_{S1S2} (A)
30	0.045 at $V_{GS} = 4.5$ V	4.9
	0.060 at $V_{GS} = 2.5$ V	4.2

FEATURES

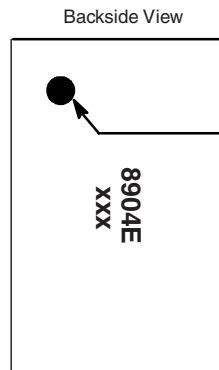
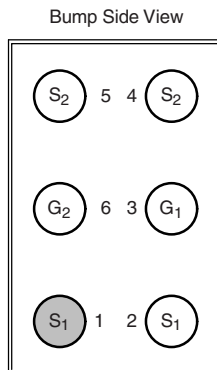
- TrenchFET® Power MOSFET
- Ultra-Low $R_{SS(on)}$ and 22.5 m Ω Maximum Effective On-Resistance
- ESD Protected: 4000 V
- MICRO FOOT® Chipscale Packaging Reduces Footprint Area, Profile (0.65 mm) and On-Resistance Per Footprint Area


RoHS
COMPLIANT

APPLICATIONS

- Battery Protection Circuit
- 1-2 Cell Li+/LiP Battery Pack for Portable Devices

MICRO FOOT



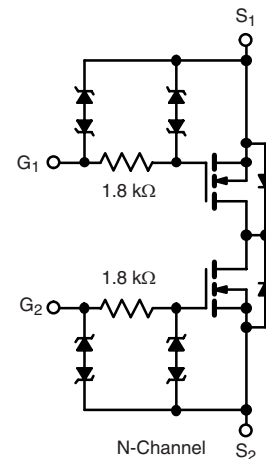
Pin 1 Identifier

Device Marking:

8904E = P/N Code
xxx = Date/Lot Traceability Code

Ordering Information:

Si8904EDB-T2-E1 (Lead (Pb)-free)



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	5 s	Steady State	Unit
Source1- Source2 Voltage	V_{S1S2}	30		V
Gate-Source Voltage	V_{GS}	± 12		
Continuous Source1- Source2 Current ($T_J = 150^\circ\text{C}$) ^a	I_{S1S2}	4.9	3.8	A
		3.5	2.7	
Pulsed Source1- Source2 Current	I_{SM}	25		
Maximum Power Dissipation ^a	P_D	1.7	1	W
		0.8	0.5	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150		$^\circ\text{C}$
Package Reflow Conditions ^c	IR/Convection	260		

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	60	75	$^\circ\text{C/W}$
		95	120	
Maximum Junction-to-Foot ^b	R_{thJF}	18	22	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. The foot is defined as the top surface of the package.

c. Refer to IPC/JEDEC (J-STD-020C), no manual or hand soldering.

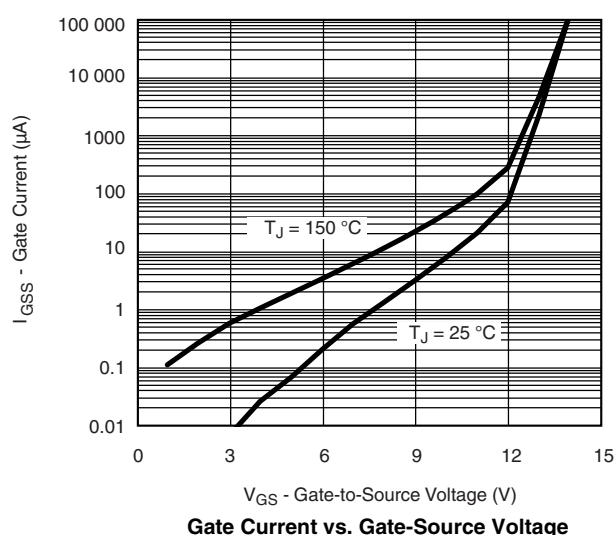
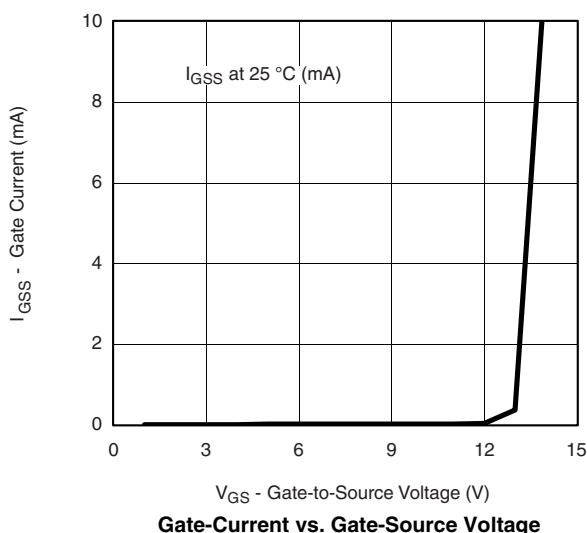
SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{SS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	0.6		1.6	V
Gate-Body Leakage	I_{GSS}	$V_{SS} = 0\text{ V}$, $V_{GS} = \pm 4.5\text{ V}$			± 4	μA
		$V_{SS} = 0\text{ V}$, $V_{GS} = \pm 12\text{ V}$			± 10	mA
Zero Gate Voltage Source Current	I_{S1S2}	$V_{SS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
		$V_{SS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 85\text{ }^{\circ}\text{C}$			5	
On-State Source Current ^a	$I_{S(on)}$	$V_{SS} = 5\text{ V}$, $V_{GS} = 4.5\text{ V}$	5			A
Source1- Source2 On-State Resistance ^a	$R_{S1S2(on)}$	$V_{GS} = 4.5\text{ V}$, $I_{SS} = 1\text{ A}$		0.037	0.045	Ω
		$V_{GS} = 2.5\text{ V}$, $I_{SS} = 1\text{ A}$		0.048	0.060	
Forward Transconductance ^a	g_{fs}	$V_{SS} = 10\text{ V}$, $I_{SS} = 1\text{ A}$		12		S
Dynamic^b						
Turn-On Delay Time	$t_{d(on)}$	$V_{SS} = 10\text{ V}$, $R_L = 10\text{ }\Omega$ $I_{SS} \cong 1\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 6\text{ }\Omega$		1.6	2.4	μs
Rise Time	t_r			2	3	
Turn-Off Delay Time	$t_{d(off)}$			1.5	2.3	
Fall Time	t_f			3.7	5.6	

Notes:

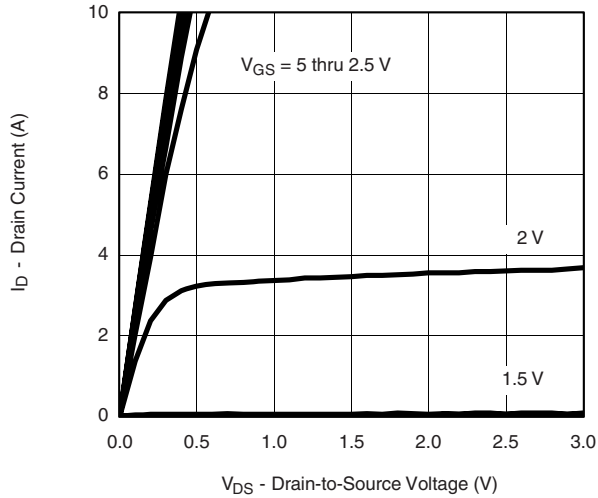
a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

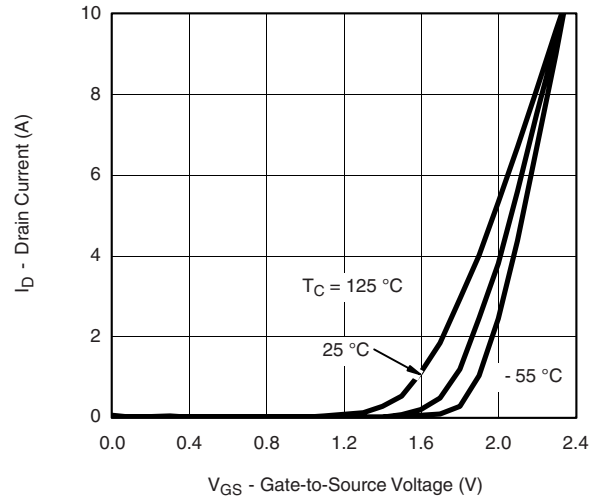
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS $25\text{ }^{\circ}\text{C}$, unless otherwise noted

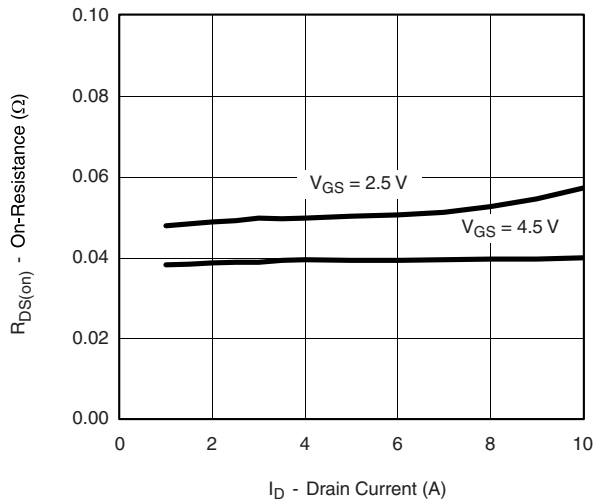
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



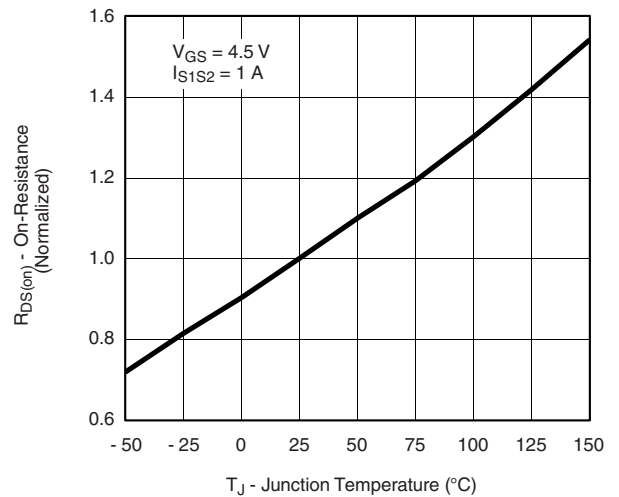
Output Characteristics



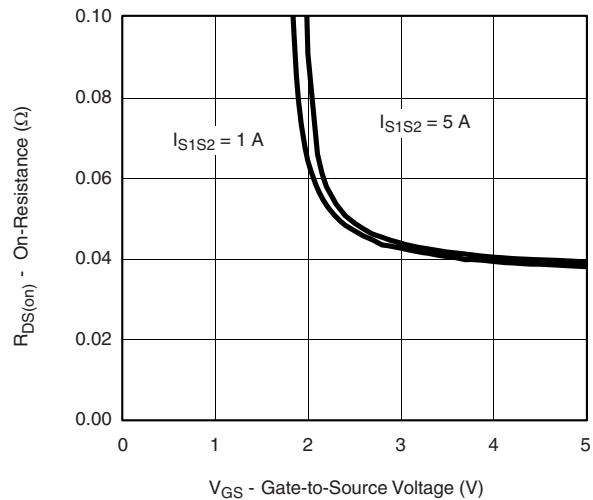
Transfer Characteristics



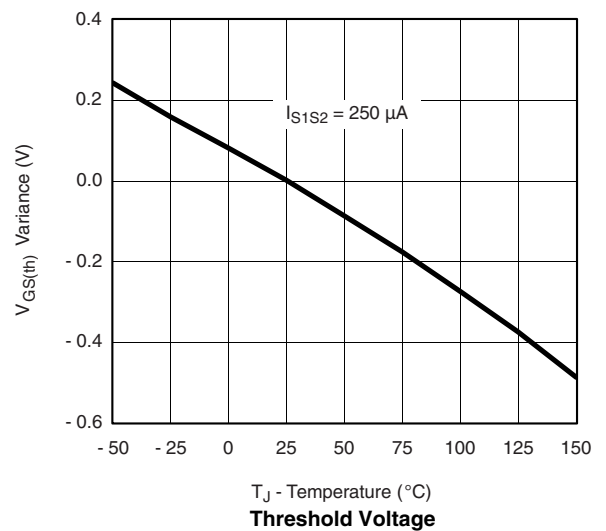
On-Resistance vs. Drain Current



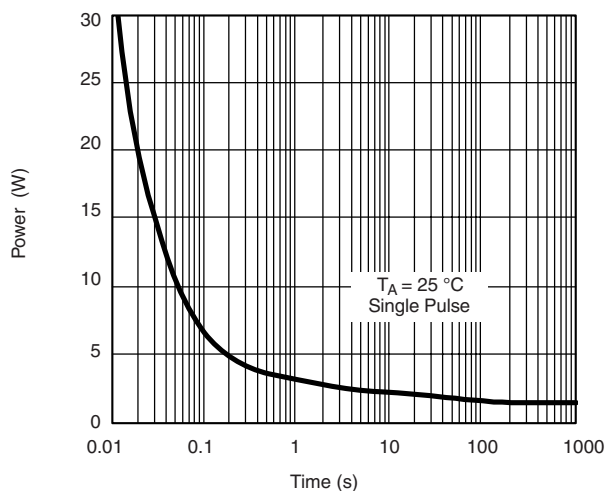
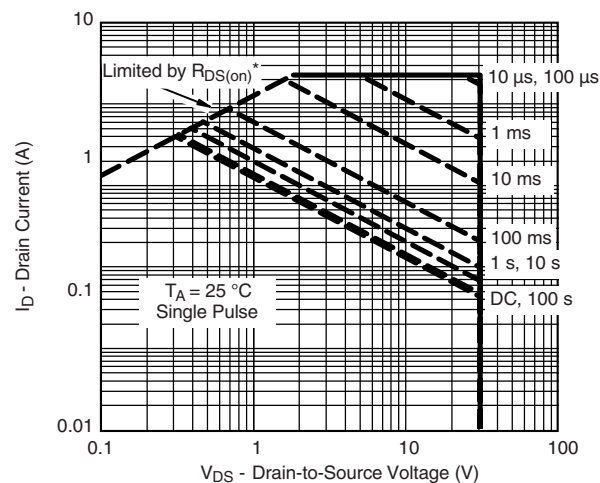
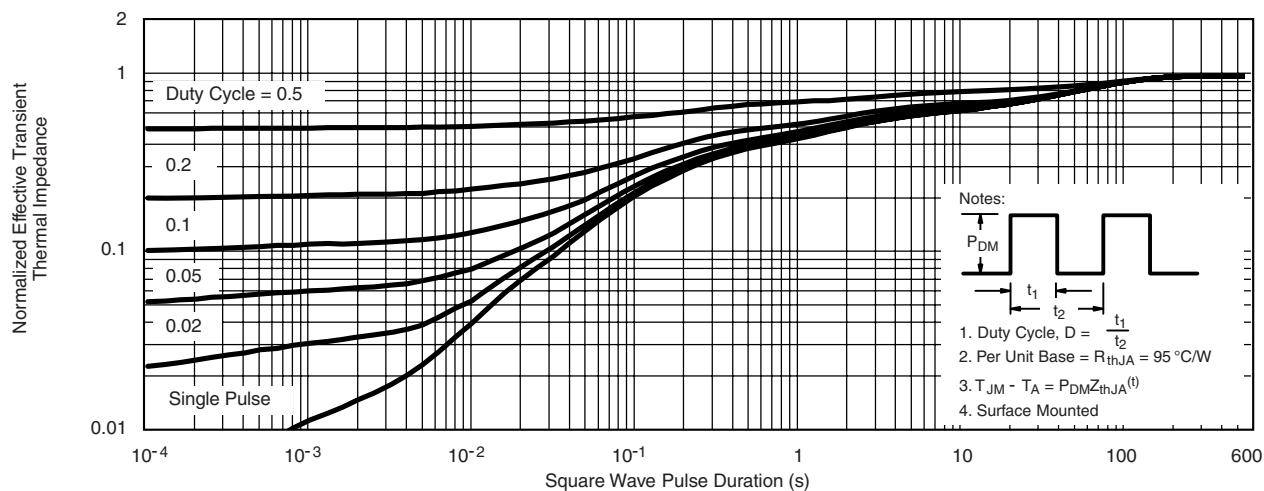
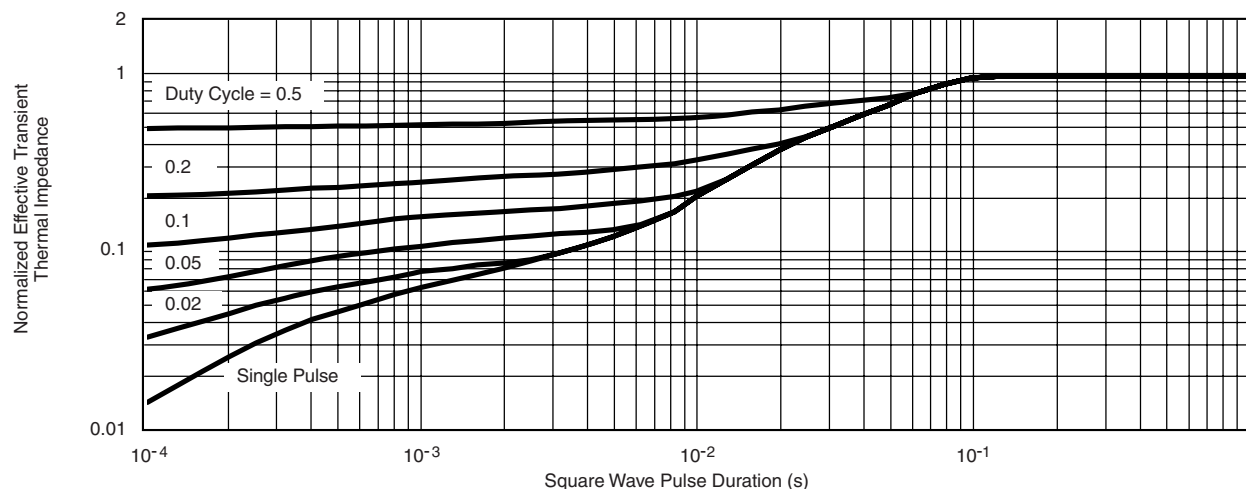
On-Resistance vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage

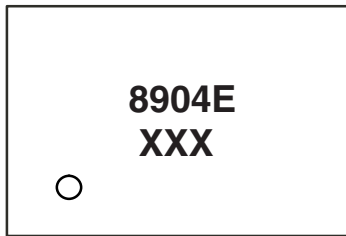
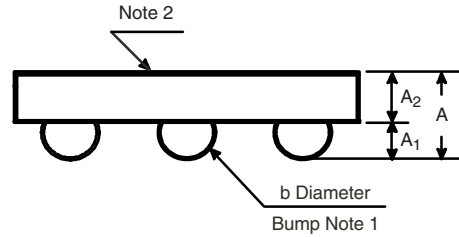
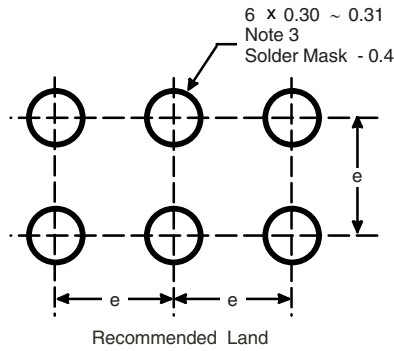


Threshold Voltage

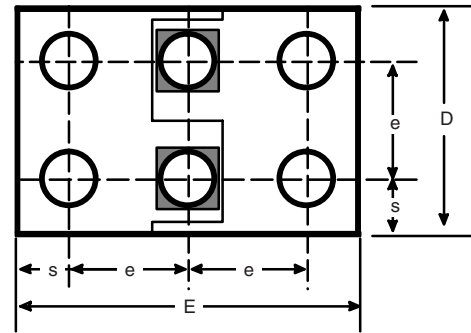
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Single Pulse Power, Junction-to-Ambient*** $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area****Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Foot**

PACKAGE OUTLINE

MICRO FOOT: 6-BUMP (2 x 3, 0.8 mm PITCH)



Mark on Backside of Die



Notes (Unless Otherwise Specified):

1. 6 solder bumps are 95.5/3.8/0.7 Sn/Ag/Cu.
2. Backside surface is coated with a Ag/Ni/Ti layer.
3. Non-solder mask defined copper landing pad.
4. Laser marks on the silicon die back.

Dim.	Millimeters ^a		Inches	
	Min.	Max.	Min.	Max.
A	0.600	0.650	0.0236	0.0256
A ₁	0.260	0.290	0.102	0.114
A ₂	0.340	0.360	0.0134	0.0142
b	0.370	0.410	0.0146	0.0161
D	1.520	1.600	0.0598	0.0630
E	2.320	2.400	0.0913	0.0945
e	0.750	0.850	0.0295	0.0335
s	0.380	0.400	0.0150	0.0157

Notes:

- a. Use millimeters as the primary measurement.

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