Si9926CDY

Vishay Siliconix

SO-8 Dual D_2 D_2 5 D1 6 D_1 8 S₁ Top View

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PRODUCT SUMMARY					
V _{DS} (V)	20				
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.018				
$R_{DS(on)}$ max. (Ω) at V_{GS} = 2.5 V	0.022				
Q _g typ. (nC)	10				
I _D (A) ^a	8				
Configuration	Dual				

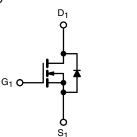
FEATURES

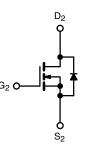
Dual N-Channel 20 V (D-S) MOSFET

- TrenchFET[®] power MOSFET
- 100 % UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- DC/DC converter - Game machine
- PC





N-Channel MOSFET

N-Channel MOSFET

ORDERING INFORMATION			
Package	SO-8		
Lead (Pb)-free	Si9926CDY-T1-E3		
Lead (Pb)-free and halogen-free	Si9926CDY-T1-GE3		

ABSOLUTE MAXIMUM RATINGS ($T_A = 25 \text{ °C}$, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	20	V	
Gate-source voltage		V _{GS}	± 12	v	
Continuous drain current (T _J = 150 °C)	T _C = 25 °C		8 ^a		
	T _C = 70 °C	1 . [8 ^a		
	T _A = 25 °C	I _D	8 a, b, c		
	T _A = 70 °C		6.7 ^{b, c}	•	
Pulsed drain current		I _{DM}	30	A	
Continuous source-drain diode current	T _C = 25 °C		2.6		
	T _A = 25 °C	- I _S	1.7 ^{b, c}		
Single pulse avalanche current		I _{AS}	5		
Single pulse avalanche energy	L = 0.1 mH	E _{AS}	1.25	mJ	
Maximum power dissipation	T _C = 25 °C		3.1		
	T _C = 70 °C		2	10/	
	T _A = 25 °C	P _D	2 ^{b, c}	W	
	T _A = 70 °C	1 [1.3 ^{b, c}		
Operating junction and storage temperature range		T _J , T _{stq}	-55 to +150	°C	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient a, c, d	$t \le 10 s$	R _{thJA}	50	62.5	°C/W	
Maximum junction-to-foot (drain)	Steady state	R _{thJF}	32	40	°C/W	

Notes

a. Package limited, T_C = 25 °C

b. Surface mounted on 1" x 1" FR4 board

c. t = 10 s

d. Maximum under steady state conditions is 110 °C/W

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static			•				
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	20	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	AVps/Ti		25	-		
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	-	-4	-	mV/°C	
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	0.6	-	1.5	V	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 12 V$	-	-	± 100	nA	
		$V_{DS} = 20 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	1	μΑ	
Zero gate voltage drain current	IDSS	$V_{DS} = 20 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 55 ^{\circ}\text{C}$	-	-	10		
On-state drain current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	30	-	-	Α	
		$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 8.3 \text{ A}$	-	0.015	0.018		
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = 2.5 \text{ V}, \text{ I}_{D} = 4.5 \text{ A}$	-	0.017	0.022	Ω	
Forward transconductance a	9 _{fs}	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 8.3 \text{ A}$	-	45	-	S	
Dynamic ^b							
Input capacitance	C _{iss}		-	1200	-	pF	
Output capacitance	C _{oss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	220	-		
Reverse transfer capacitance	C _{rss}		-	100	-		
Total gate charge	Qg	$V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 8.3 \text{ A}$	-	22	33		
			-	10	15		
Gate-source charge	Q _{qs}	$V_{DS} = 10 \text{ V}, \text{ V}_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 8.3 \text{ A}$	-	2.5	-	nC	
Gate-drain charge	Q _{gd}		-	1.7	-		
Gate resistance	R _g	f = 1 MHz	-	2.4	-	Ω	
Turn-on delay time	t _{d(on)}		-	15	25		
Rise time	t _r	$V_{DD} = 10 \text{ V}, \text{ R}_1 = 1.5 \Omega$	-	10	15		
Turn-off delay time	t _{d(off)}	$I_D \cong 6.7 \text{ A}, V_{GEN} = 4.5 \text{ V}, \text{ R}_{g} = 1 \ \Omega$	-	35	55		
Fall time	t _f		-	12	20		
Turn-on delay time	t _{d(on)}		-	10	15	ns	
Rise time	t _r	$V_{DD} = 10 \text{ V}, \text{ R}_{\text{I}} = 1.5 \Omega$	-	12	20	-	
Turn-off delay time	t _{d(off)}	$I_D \cong 6.7$ Å, $V_{GEN} = 10$ V, $R_g = 1$ Ω	-	25	40		
Fall time	t _f		-	10	15		
Drain-Source Body Diode Characteristi	cs						
Continuous source-drain diode current	IS	T _C = 25 °C	-	-	2.6		
Pulse diode forward current	I _{SM}		-	-	30	A	
Body diode voltage	V _{SD}	$I_{\rm S} = 6.7$ A, $V_{\rm GS} = 0$ V	-	0.8	1.2	V	
Body diode reverse recovery time	t _{rr}		-	20	40	ns	
Body diode reverse recovery charge	Q _{rr}	I _F = 6.7 A, di/dt = 100 A/μs,	-	10	20	nC	
Reverse recovery fall time	ta	$T_J = 25 \text{ °C}$	-	10	-		
Reverse recovery rise time	t _b		-	10	-	ns	

Notes

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %

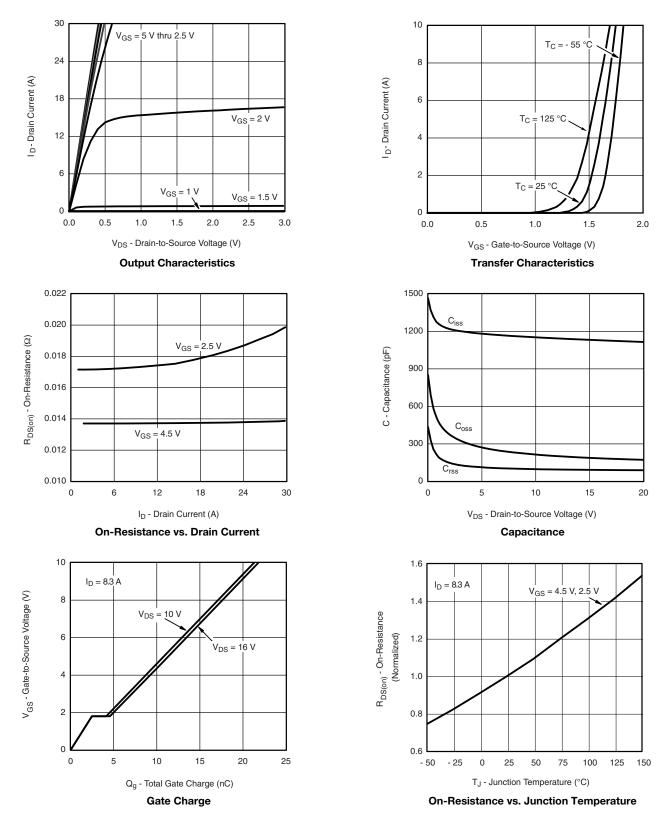
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



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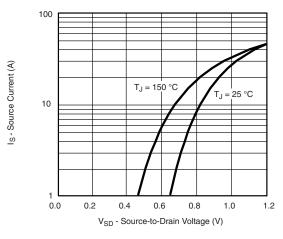
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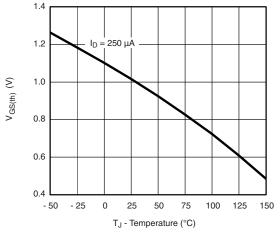
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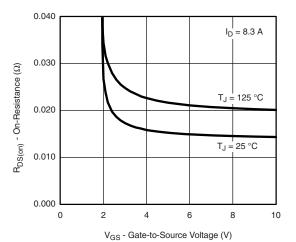
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



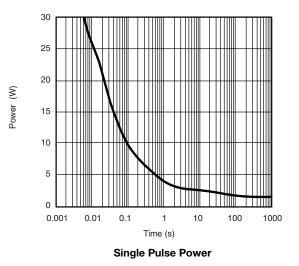
Source-Drain Diode Forward Voltage

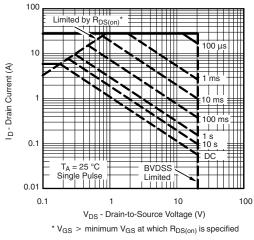


Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage





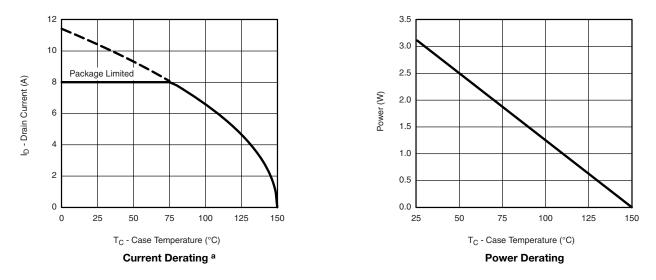
Safe Operating Area, Junction-to-Ambient



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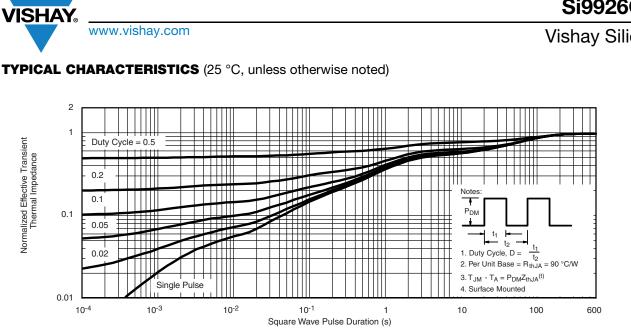
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

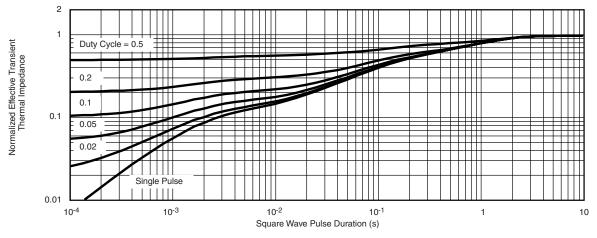


Notes

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



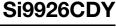
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68606.

Document Number: 68606



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Package Information

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SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012





	MILLIM	IETERS	INC	HES	
DIM	Min	Мах	Min	Max	
A	1.35	1.75	0.053	0.069	
A ₁	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27	BSC	0.050 BSC		
н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498					

Application Note 826

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RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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