## SUD50P06-15L

www.vishay.com

**PRODUCT SUMMARY** 

 $R_{DS(on)}$  max. ( $\Omega$ ) at  $V_{GS}$  = -10 V

 $R_{DS(on)}$  max. ( $\Omega$ ) at  $V_{GS}$  = -4.5 V

V<sub>DS</sub> (V)

I<sub>D</sub> (A) <sup>d</sup>

Configuration

**Vishay Siliconix** 

# P-Channel 60 V (D-S), 175 °C MOSFET



-60

0.015

0.020

-50

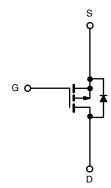
Single

#### FEATURES

• TrenchFET<sup>®</sup> power MOSFET

• 175 °C junction temperature

• Material categorization: for definitions of <sup>COMPLIANT</sup> compliance please see <u>www.vishay.com/doc?99912</u>



RoHS

P-Channel MOSFET

ORDERING INFORMATION	
Package	DPAK (TO-252)
Lead (Pb)-free	SUD50P06-15L-E3

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> =	= 25 °C, unless otherw	ise noted)			
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V <sub>DS</sub>	-60	V	
Gate-source voltage		V <sub>GS</sub>	± 20	v	
Continuous drain current (T <sub>J</sub> = 175 °C)	T <sub>C</sub> = 25 °C		-50 d		
	T <sub>C</sub> = 125 °C	D ID	-39	A	
Pulsed drain current		I <sub>DM</sub>	I <sub>DM</sub> -80		
Avalanche current		I <sub>AR</sub>	-50		
Repetitive avalanche energy <sup>a</sup>	L = 0.1 mH	E <sub>AR</sub>	125	mJ	
Power dissipation	T <sub>C</sub> = 25 °C	р	136 <sup>c</sup>	w	
	T <sub>A</sub> = 25 °C	P <sub>D</sub>	3 b, c	vv	
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C	

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT	
Junction-to-ambient <sup>b</sup>	t ≤ 10 s	R <sub>thJA</sub>	15	18	°C/W	
	Steady state		40	50		
Junction-to-case		R <sub>thJC</sub>	0.82	1.1		

Notes

b. When mounted on 1" square PCB (FR4 material)

c. See SOA curve for voltage derating

d. Package limited

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a. Duty cycle ≤ 1%

## SUD50P06-15L



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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = -250 \mu\text{A}$	-60	-	-	V	
Gate threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = -250 \ \mu A$	-1	-	-3	V	
Gate-body leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$	-	-	± 100	nA	
Zero gate voltage drain current		$V_{DS} = -48 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	-1	μΑ	
	I <sub>DSS</sub>	$V_{DS} = -48 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125 \text{ °C}$	-	-	-50		
		$V_{DS} = -48 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 175 \text{ °C}$	-	-	-150		
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} = -5 V, V_{GS} = -10 V$	-50	-	-	А	
Drain-source on-state resistance <sup>a</sup>		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -17 A	-	0.012	0.015	1	
	Б	$V_{GS}$ = -10 V, $I_D$ = -50 A, $T_J$ = 125 °C	-	-	0.025	Ω	
	R <sub>DS(on)</sub>	$V_{GS}$ = -10 V, $I_D$ = -50 A, $T_J$ = 175 °C	-	-	0.030		
		$V_{GS} = -4.5 \text{ V}, \text{ I}_{D} = -14 \text{ A}$	-	-	0.020		
Forward transconductance a	9 <sub>fs</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -17 A	-	61	-	S	
Dynamic <sup>b</sup>	-						
Input capacitance	C <sub>iss</sub>		-	4950	-	pF	
Output capacitance	C <sub>oss</sub>	$V_{GS} = 0 V, V_{DS} = -25 V, f = 1 MHz$	-	480	-		
Reverse transfer capacitance	C <sub>rss</sub>		-	405	-		
Total gate charge <sup>c</sup>	Qg		-	110	165		
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>	$V_{DS} = -30 \text{ V}, \text{ V}_{GS} = -10 \text{ V}, \text{ I}_{D} = -50 \text{ A}$	-	19	-	nC	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>		-	28	-		
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>		-	15	23		
Rise time <sup>c</sup>	tr	$\begin{array}{l} V_{\text{DD}} = \text{-30 V, } R_{\text{L}} = 0.6 \ \Omega \\ I_{\text{D}} \cong \text{-50 A, } V_{\text{GEN}} = \text{-10 V, } R_{\text{G}} = 6 \ \Omega \end{array}$	-	70	105	ns	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>		-	175	260		
Fall time <sup>c</sup>	t <sub>f</sub>		-	175	260		
Source-Drain Diode Ratings and Ch	aracteristics (	T <sub>C</sub> = 25 °C) <sup>b</sup>	•				
Continuous current	IS		-	-	-50	^	
Pulsed current	I <sub>SM</sub>		-	-	-80	- A	
Forward voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = -50 A, V <sub>GS</sub> = 0 V	-	1	1.6	V	
Reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = -50 A, di/dt = 100 A/μs	-	45	70	ns	

Notes

a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %

b. Guaranteed by design, not subject to production testing

c. Independent of operating temperature

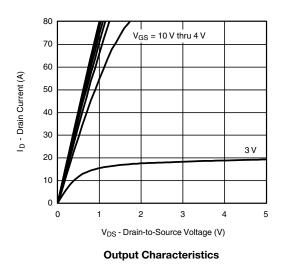
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

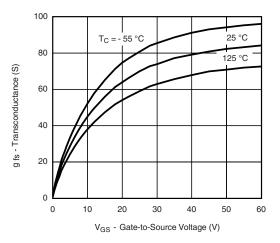
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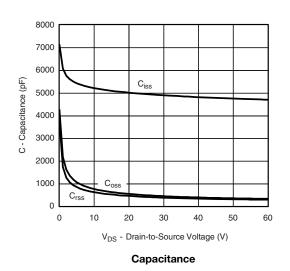
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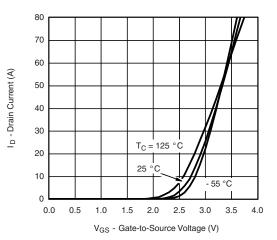
### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



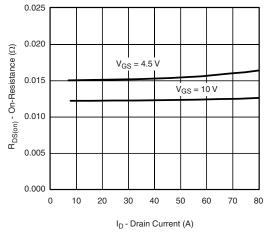




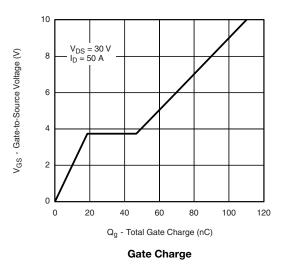




Transfer Characteristics



**On-Resistance vs. Drain Current** 



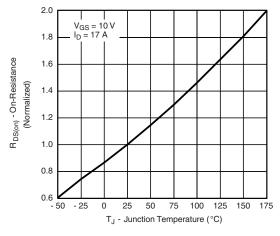
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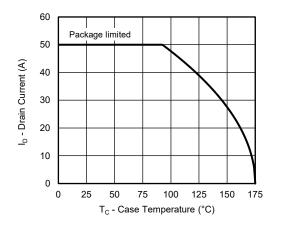
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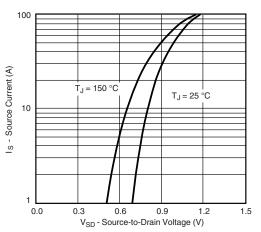


**On-Resistance vs. Junction Temperature** 

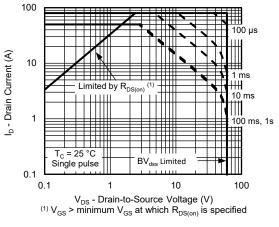
### THERMAL RATINGS



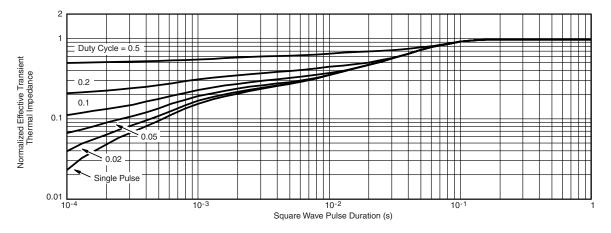
Max. Avalanche and Drain Current vs. Case Temperature



Source-Drain Diode Forward Voltage



Safe Operating Area



#### Normalized Thermal Transient Impedance, Junction-to-Case

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