TLV841 Small Size Nano-Power Voltage Supervisor in WCSP Package

1 Features

Designed for high performance:

- Nano quiescent current: 125 nA (typical)
- High threshold accuracy: ±0.5% (typical)
- Built-in precision hysteresis (V_{HYS}): 5% (typical)

Designed for a wide range of applications:

- Operating voltage range: 0.7 V to 5.5 V
- Adjustable threshold voltage: 0.505 V (typical)
- Fixed (V_{IT-}) voltage: 0.8 V to 4.9 V in 0.1 V steps
- Separate SENSE pin (TLV841S)
- Active-low manual reset ($\overline{MR}$) (TLV841M)
- Push-button monitoring for TLV841 (S/M variants)
- Reset time delay (t_D): Capacitor-based programmable (TLV841C)
  - Min time delay: 40 µs (typical) without capacitor
- Reset time delay (t_D): Fixed time delay options (TLV841M and TLV841S)
  - 40 µs, 2 ms, 10 ms, 30 ms, 50 ms, 80 ms, 100 ms, 150 ms, 200 ms
- Temperature range: –40°C to +125°C

Multiple output topologies, package type:

- TLV841xxDL: open-drain, active-low ($\overline{RESET}$)
- TLV841xxPL: push-pull, active-low ($\overline{RESET}$)
- TLV841xxDH: open-drain, active-high (RESET)
- TLV841xxPH: push-pull, active-high (RESET)
- Package: 0.73-mm x 0.73-mm DSBGA

2 Applications

- Personal electronics including wearables and hearing devices
- Home theater and entertainment
- Electronic point of sale
- Grid infrastructure
- Data center and enterprise computing

3 Description

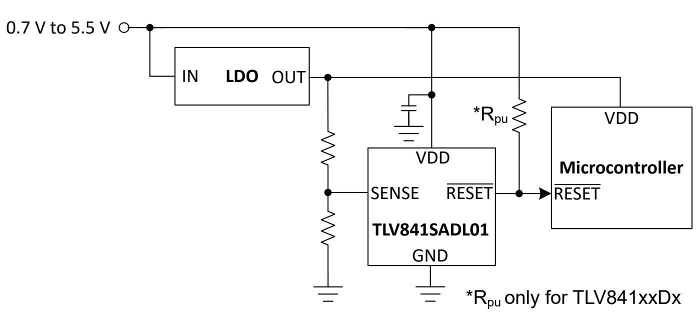
TLV841 is a nano power, precision voltage supervisor with ±0.5% threshold accuracy in an ultra small DSBGA package. The TLV841 offers three pinout variants (S, M, C) to provide many unique options in the smallest total solution size in its class. Built-in hysteresis along with fixed or programmable (TLV841C) reset delay prevent false reset signals when monitoring a voltage rail or push button signals. On active-low outputs of TLV841S, increasing the voltage threshold hysteresis can be achieved by adding an external resistor between the SENSE and $\overline{RESET}$ pins. TLV841 with its precision performance, low power consumption, and best in-class features in the smallest compact form factor, offers an ideal solution for wide range battery powered applications such as personal and consumer products.

The separate VDD and SENSE (TLV841S) pins allow for the redundancy sought by high-reliability systems. SENSE is decoupled from VDD and can monitor rail voltages other than VDD or can be used as a push-button input. Optional use of external resistors are supported by the high impedance input of the SENSE pin. TLV841S offers fixed reset delay timing options with no need of an external capacitor. TLV841C allows programmable reset time delay including a minimum delay when the CT pin is left floating. TLV841M offers a separate manual reset ($\overline{MR}$) pin to force a reset condition with an external signal or be used as a push button input. TLV841M can be setup for VDD and $\overline{MR}$ pin monitoring to create a simple two-channel supervisor solution. TLV841 operates over a temperature range of -40°C to +125°C (T_A).

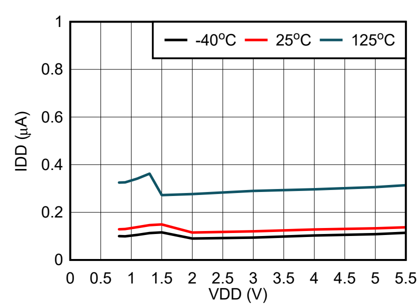
Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TLV841	DSBGA (4)	0.73 mm × 0.73 mm

(1) For package details, see the mechanical drawing addendum at the end of the data sheet.



Typical Application Circuit



Typical Supply Current

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2021) to Revision D (January 2023)	Page
• Removed Table 12-2	25

Changes from Revision B (May 2021) to Revision C (June 2021)	Page
• RTM of device	1

5 Device Comparison

Figure 5-1 shows the device naming nomenclature to compare the different device variants. See Table 12-1 for a more detailed explanation. Please contact Texas Instruments for availability of variant options.

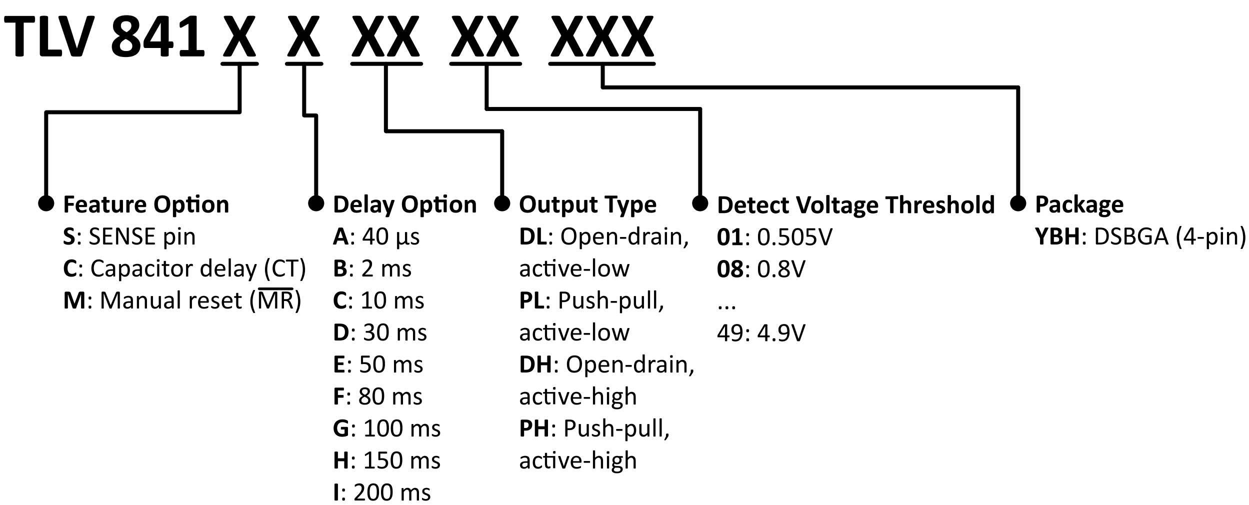


Figure 5-1. Device Naming Nomenclature

6 Pin Configuration and Functions

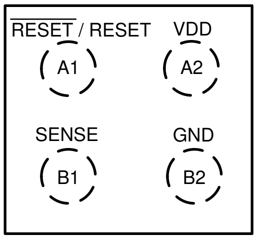


Figure 6-1. YBH 4-Pin DSBGA Package (TLV841S) Top View

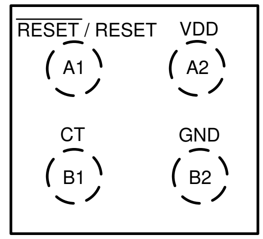


Figure 6-2. YBH 4-Pin DSBGA Package (TLV841C) Top View

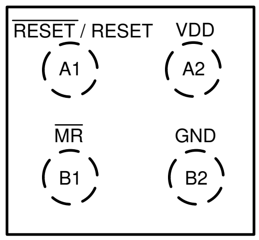


Figure 6-3. YBH 4-Pin DSBGA Package (TLV841M) Top View

Table 6-1. Pin Functions

PIN				I/O	DESCRIPTION
PIN NO.	TLV841S	TLV841C	TLV841M		
A1	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	O	**Active-Low Output Reset Signal for TLV841xxxL**: This pin is driven logic low when VDD and SENSE voltage falls below the negative voltage threshold (V_{IT-}) or when the $\overline{\text{MR}}$ voltage falls below the logic low threshold. $\overline{\text{RESET}}$ remains logic low (asserted) until $\overline{\text{MR}}$ is above the logic high threshold or for the duration of the delay time period (t_D) after VDD or SENSE voltage rises above V_{IT-} + V_{HYS}
A1	RESET	RESET	RESET	O	**Active-High Output Reset Signal for TLV841xxxH**: This pin is driven logic high when VDD or SENSE voltage falls below the negative voltage threshold (V_{IT-}) or when the $\overline{\text{MR}}$ voltage falls below the logic low threshold. RESET remains logic high (asserted) until $\overline{\text{MR}}$ is above the logic high threshold or for the duration of the delay time period (t_D) after VDD or SENSE voltage rises above V_{IT-} + V_{HYS}
A2	VDD	VDD	VDD	I	**Input Supply Voltage**: The VDD pin connects to the power supply to power the device. TLV841C and TLV841M monitor VDD voltage. TLV841S monitors SENSE only. Good analog design practice recommends placing a minimum 0.1 µF ceramic capacitor as near as possible to the VDD pin.
B1	SENSE	_	_	I	**SENSE pin**: This pin is connected to the voltage to be monitored. When the voltage on SENSE falls below the negative threshold voltage V_{IT-}, reset asserts. When the voltage on SENSE rises above the positive threshold voltage (V_{IT-} + V_{HYS}), reset deasserts. For noisy applications, placing a 10 nF to 100 nF ceramic capacitor close to this pin may be needed for optimum performance.
B1	_	CT	_	I	**Capacitor Time Delay Pin**: The CT pin offers a user-programmable reset deassert delay time. Connect an external capacitor on this pin to adjust time delay. When not in use leave pin floating for the smallest fixed time delay.
B1	_	_	$\overline{\text{MR}}$	I	**Manual Reset**: Pull this pin to a logic low to assert a reset signal in the $\overline{\text{RESET}}$ output pin ($\overline{\text{RESET}}$ signal for DL and PL option). After $\overline{\text{MR}}$ pin is left floating or pulls to logic high, the $\overline{\text{RESET}}$ output deasserts to the nominal state after the reset delay time (t_D)expires. **If unused, the pin can be left floating or connected to VDD.**
B2	GND	GND	GND	_	**Ground**

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted[(1)]

		MIN	MAX	UNIT
Voltage	VDD, SENSE (TLV841S)	–0.3	6	V
Voltage	CT (TLV841C), $\overline{\text{MR}}$ (TLV841M), $\overline{\text{RESET}}$ (TLV841xxPx), RESET (TLV841xxPx)	–0.3	V_{DD}+0.3 [(3)]	V
	$\overline{\text{RESET}}$ (TLV841xxDx), RESET (TLV841xxDx)	–0.3	6	
Current	$\overline{\text{RESET}}$, RESET		±20	mA
Temperature[(2)]	Operating ambient temperature, T_A	–40	125	°C
Temperature	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.
(3) The absolute maximum rating is (VDD + 0.3) V or 6 V, whichever is smaller

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	± 2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[(2)]	± 750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	VDD (TLV841C, TLV841M)	0.7		5.5	V
	VDD (TLV841S)	0.85		5.5	
	VDD (TLV841xxPH)	1		5.5	
	SENSE	0		5.5	
	$\overline{\text{MR}}$ [(1)], CT	0		V_{DD}	
	$\overline{\text{RESET}}$(TLV841xxPL), RESET (TLV841xxPH)	0		V_{DD}	
	$\overline{\text{RESET}}$(TLV841xxDL), RESET (TLV841xxDH)	0		5.5	
Current	$\overline{\text{RESET}}$, RESET	–5		5	mA
T_A	Operating free air temperature	–40		125	°C
C_{CT}	CT pin capacitor range	0		10	µF

(1) If the logic signal driving $\overline{\text{MR}}$ is less than V_{DD}, then additional current flows into VDD and out of $\overline{\text{MR}}$. $\overline{\text{MR}}$ pin voltage should not be higher than V_{DD}.

7.4 Thermal Information

THERMAL METRIC[(1)]		TLV841 YBH (WCSP) 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	58.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

At $V_{DDMIN} \le V_{DD} \le 5.5$ V, CT = $\overline{MR}$ = Open, $\overline{RESET}$/RESET pull-up resistor $R_{pull\text{-}up}$ [3] = 100 kΩ to VDD, output reset load C_{LOAD} = 10 pF and over the operating free-air temperature range –40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
COMMON PARAMETERS							
$V_{ADJ\text{-}VIT-}$	Negative-going input threshold for TLV841Sxxx01 ADJ version				0.505		V
V_{IT-}	Negative-going input threshold range Fixed threshold version [1]			0.8		4.9	V
V_{IT-_ACC}	Negative-going input threshold accuracy	V_{IT-} = 0.505 V (TLV841Sxx01) or 0.8 V to 1.7 V (Fixed threshold)		-2.5	±0.5	2.5	%
		V_{IT-} = 1.8 V to 4.9 V (Fixed threshold)		-2	±0.5	2	
V_{HYS}	Hysteresis on V_{IT-} pin	V_{IT-} = 0.505 V and 0.8 V		3	5	8	%
		V_{IT-} = 0.9 V to 4.9 V		3	5	7	
V_{POR}	Power on reset voltage [2]	TLV841xxxLxx	$V_{OL(MAX)}$ = 300 mV $I_{\overline{RESET}(Sink)}$ = 15 µA			700	mV
		TLV841xxxHxx	$V_{OH(MIN)}$ = 0.8VDD $I_{RESET(Source)}$ = 15 µA			900	
V_{OL}	Low level output voltage		V_{DD} = 0.85 V $I_{\overline{RESET}(Sink)}$ = 15 µA $I_{RESET(Sink)}$ = 15 µA			300	mV
			V_{DD} = 3.3 V $I_{\overline{RESET}(Sink)}$ = 2 mA $I_{RESET(Sink)}$ = 2 mA			300	mV
			V_{DD} = 5.5 V $I_{\overline{RESET}(Sink)}$ = 2 mA $I_{RESET(Sink)}$ = 2 mA			300	mV
V_{OH}	High level output voltage		V_{DD} = 1 V $I_{\overline{RESET}(Source)}$ = 15 µA $I_{RESET(Source)}$ = 15 µA	$0.8V_{DD}$			V
			V_{DD} = 1.8 V $I_{\overline{RESET}(Source)}$ = 500 µA $I_{RESET(Source)}$ = 500 µA	$0.8V_{DD}$			V
			$V_{DD} \ge 3.3$ V $I_{\overline{RESET}(Source)}$ = 2 mA $I_{RESET(Source)}$ = 2 mA	$0.8V_{DD}$			V
$I_{lkg(OD)}$	Open-Drain output leakage current	$V_{DD} = V_{PULLUP}$ = 5.5 V	T_A = –40°C to 85°C		10	100	nA
					10	350	
I_{DD}	Supply current into VDD pin	Supply current into VDD pin	V_{DD} = 5.5 V V_{IT-} = 1.9 V to 4.9 V		0.125	1	µA

7.5 Electrical Characteristics (continued)

At $V_{DDMIN} \leq V_{DD} \leq 5.5$ V, CT = $\overline{MR}$ = Open, $\overline{RESET}$/RESET pull-up resistor $R_{pull\text{-}up}$ [(3)] = 100 kΩ to VDD, output reset load C_{LOAD} = 10 pF and over the operating free-air temperature range –40℃ to 125℃, unless otherwise noted. Typical values are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TLV841S						
I_{SENSE}	Current into SENSE pin, fixed threshold variant	$V_{DD} = V_{SENSE} = 5.5$ V V_{IT-} = 0.8 V to 4.9 V		0.025	0.1	µA
	Current into SENSE pin, ADJ variant	$V_{DD} = V_{SENSE} = 5.5$ V V_{IT-} = 0.505 V		0.025	0.05	
TLV841M						
$V_{\overline{MR}\_L}$	Manual reset logic low input				$0.3V_{DD}$	V
$V_{\overline{MR}\_H}$	Manual reset logic high input		$0.7V_{DD}$			V
$R_{\overline{MR}}$	Manual reset internal pull-up resistance			100		kΩ
TLV841C						
R_{CT}	CT pin internal resistance		410	500	590	kΩ

(1) V_{IT-} threshold voltage range from 0.8 V to 4.9 V (for DL, PL, DH) and 1 V to 4.9 V (for PH) in 100 mV steps, for released versions see Device Voltage Thresholds table.
(2) V_{POR} is the minimum V_{DD} voltage level for a controlled output state.
(3) Pull up resistance applicable for open drain variants

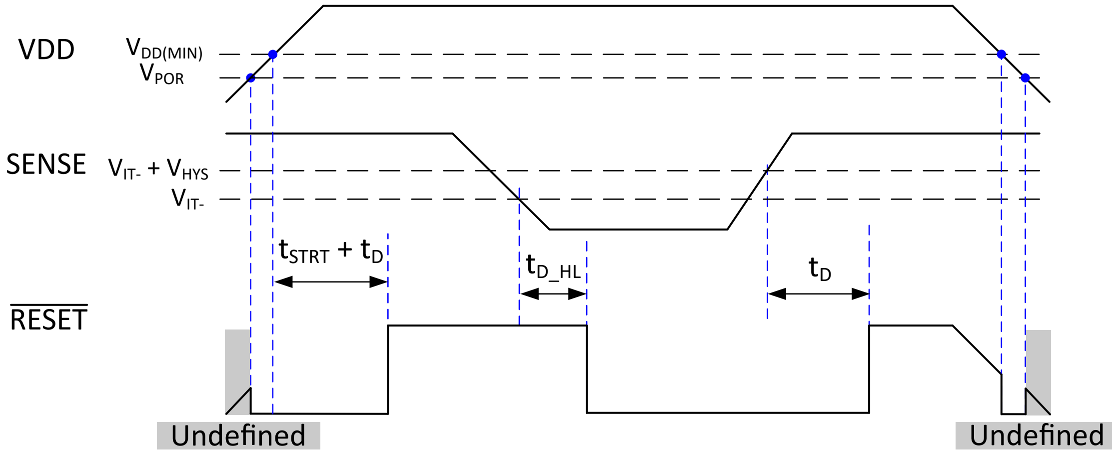
7.6 Timing Requirements

At $V_{DDMIN} \le V_{DD} \le 5.5$ V, CT = $\overline{MR}$ = Open, $\overline{RESET}$ pull-up resistor $R_{pull-up}$ = 100 kΩ to VDD, output load is C_{LOAD} = 10 pF and over the operating free-air temperature range –40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{P_HL}	Propagation detect delay for V_{DD} falling below V_{IT-}	V_{DD} = (V_{IT+} + 10%) to (V_{IT-} – 10%) (2)		30	50	µs
t_D	Reset time delay (TLV841C variant)	CT pin = Open or NC		40	80	µs
		CT pin = 10 nF		6.2		ms
		CT pin = 1 µF		619		ms
t_D	Reset time delay (TLV841S and TLV841M variant) (5)	Variant A (3)		40	80	µs
		Variant B (3)		2		ms
		Variant C (3)		10		ms
		Variant D (3)		30		ms
		Variant E (3)		50		ms
		Variant F (3)		80		ms
		Variant G (3)		100		ms
		Variant H (3)		150		ms
		Variant I (3)		200		ms
t_{GI_VIT-}	Glitch immunity V_{IT-}	5% V_{IT-} overdrive (4)		10		µs
t_{STRT}	Startup Delay (1)				300	µs
$t_{\overline{MR}\_RES}$	Propagation delay from $\overline{MR}$ low to reset	V_{DD} = 3.3 V, $\overline{MR}$ < $V_{\overline{MR}\_L}$		t_{P_HL}		µs
$t_{\overline{MR}\_tD}$	Delay from release $\overline{MR}$ to deassert reset	V_{DD} = 3.3 V, $\overline{MR}$ = $V_{\overline{MR}\_L}$ to $V_{\overline{MR}\_H}$		t_D		ms
$t_{\overline{MR}\_PW}$	Glitch immunity $\overline{MR}$ pin			10		µs

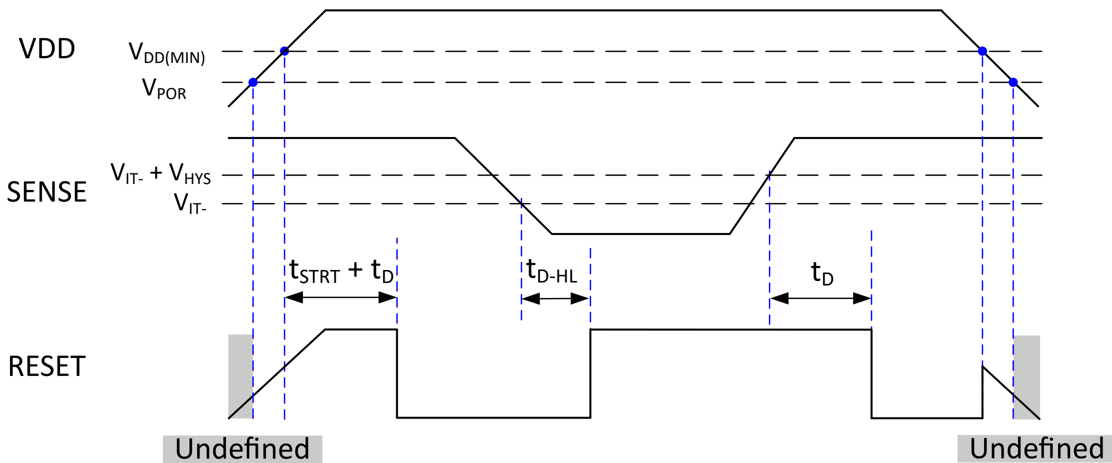
(1) When VDD starts from less than the specified minimum V_{DD} and then exceeds V_{POR}, reset is release after the startup delay (t_{STRT}). For TLV841C variants a capacitor at CT pin will add t_D delay to t_{STRT} time
(2) t_{P_HL} measured from threhold trip point (V_{IT-}) to V_{OL} for active low variants and V_{OH} for active high variants.
(3) Refer device nomenclature table for variant description. V_{DD} transition from V_{IT-} – 10% to V_{IT+} + 10% for TLV841M and TLV841C; V_{SENSE} transition from V_{IT-} – 10% to V_{IT+} + 10% for TLV841S
(4) Overdrive % = [(V_{DD}/ V_{IT-}) – 1] × 100% for TLV841M and TLV841C; Overdrive % = [(V_{SENSE}/ V_{IT-}) – 1] × 100% for TLV841S
(5) Specified by design and characterization

7.7 Timing Diagrams



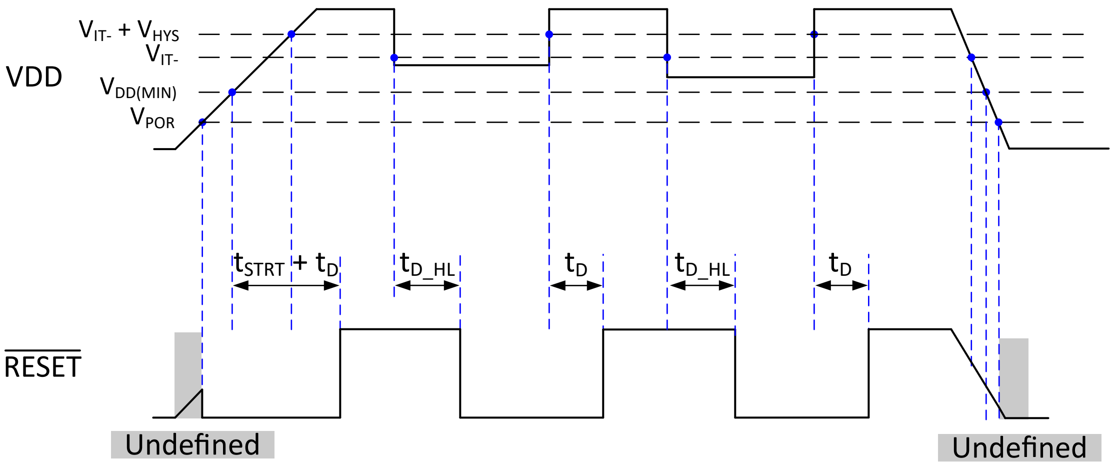
A. Open-Drain timing diagram assumes the $\overline{RESET}$ pin is connected via an external pull-up resistor to VDD.

Figure 7-1. Timing Diagram for TLV841SxxL (SENSE) Active Low Output [Open-Drain and Push-Pull Output Topology]



A. Open-Drain timing diagram assumes the RESET pin is connected via an external pull-up resistor to VDD.

Figure 7-2. Timing Diagram for TLV841SxxH (SENSE) Active High Output [Open-Drain and Push-Pull Output Topology]

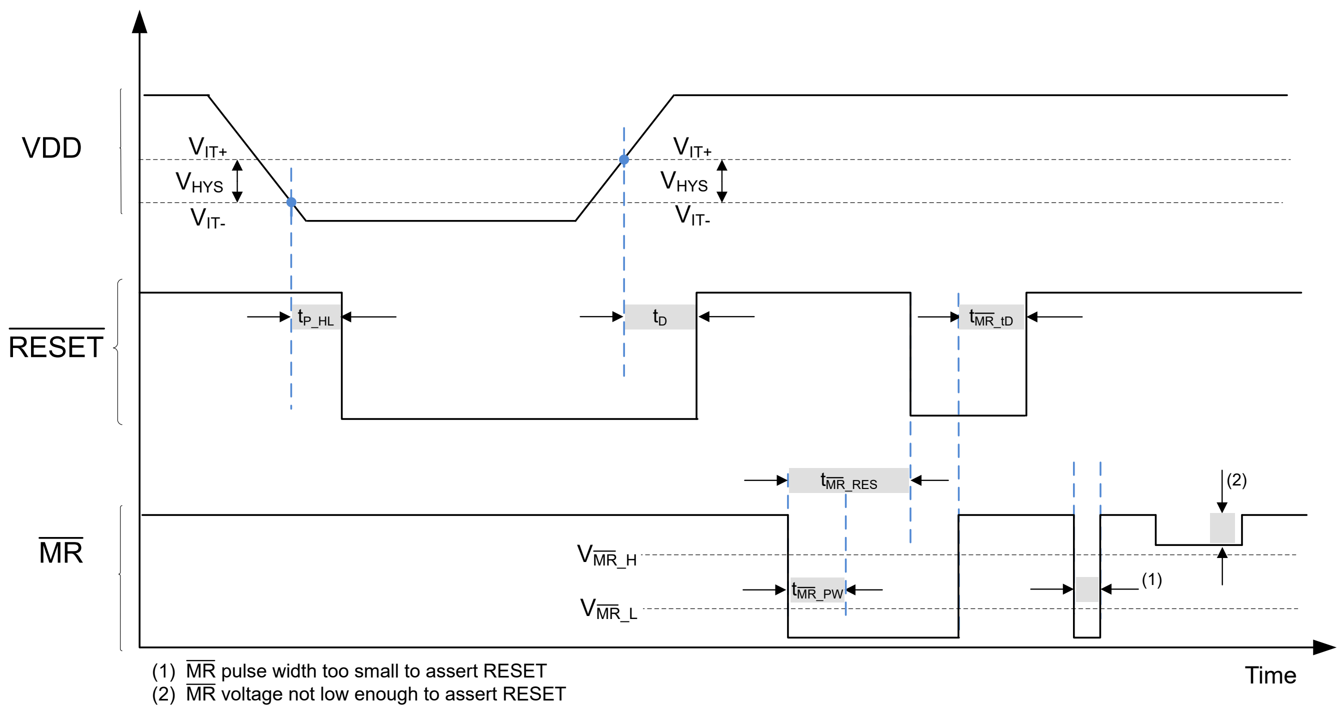


A. Open-Drain timing diagram assumes the $\overline{RESET}$ / RESET pin is connected via an external pull-up resistor to VDD.

B. $t_{D\ (no\ cap)}$ is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to CT pin then t_D programmed time will be added to the startup time, VDD slew rate = 1 V / µs.

C. Be advised that the VDD falling slew rate is (slew rate > 1 V / µs) and resulting $\overline{RESET}$in what is shown above figure. The $\overline{RESET}$ behavior would be similar to Figure 7-1 if the slew rate was much slower or if VDD decay time is larger than the prop delay (t_{D_HL}).

Figure 7-3. Timing Diagram for TLV841CxxL (CT) Active Low Output [Open-Drain and Push-Pull Output Topology]



A. Open-Drain timing diagram assumes the $\overline{RESET}$ / RESET pin is connected via an external pull-up resistor to VDD.

Figure 7-4. Timing Diagram for TLV841MxxL Active Low Output ($\overline{MR}$) [Open-Drain and Push-Pull Output Topology]

7.8 Typical Characteristics

Typical characteristics show the typical performance of the TLV841 device. Test conditions are T_A = 25°C, V_{DD} = 3.3 V, $R_{pull-up}$ = 100 kΩ, C_{Load} = 50 pF, unless otherwise noted.

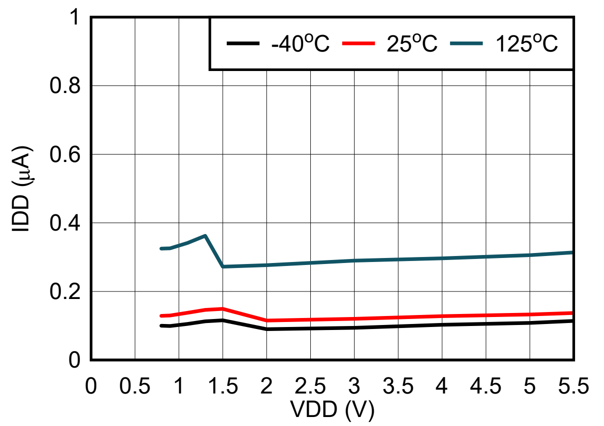


Figure 7-5. Supply Current vs Supply Voltage for TLV841S

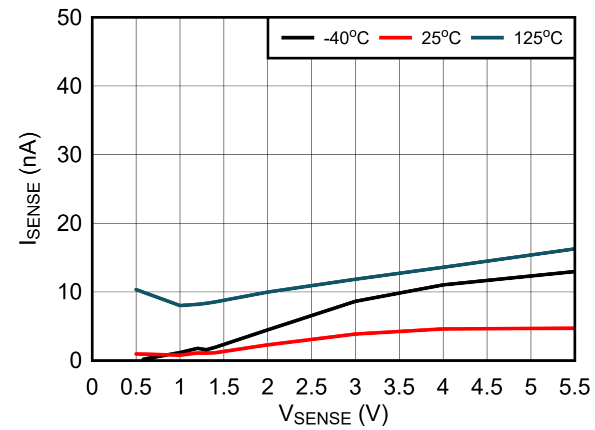


Figure 7-6. SENSE Current vs V_{SENSE}

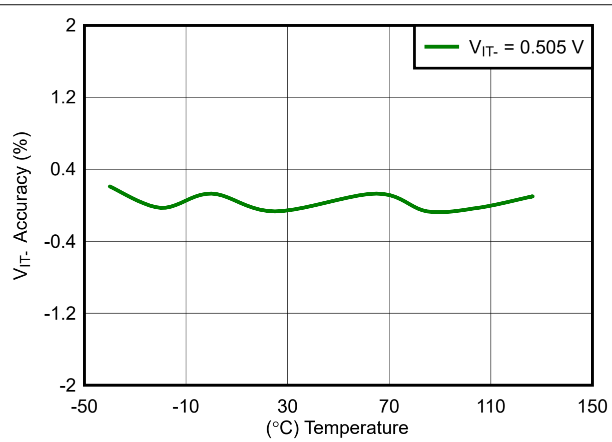


Figure 7-7. V_{IT-} Accuracy vs Temperature

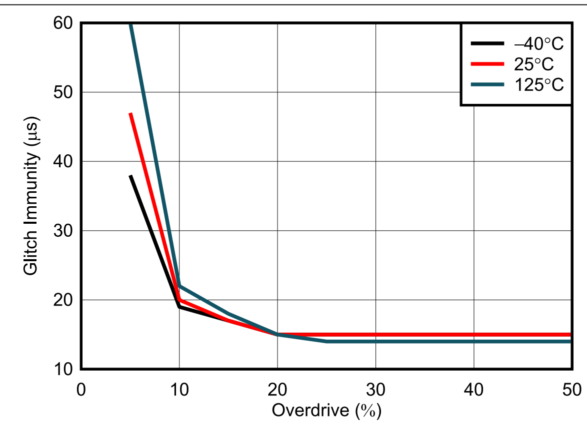


Figure 7-8. SENSE Glitch Immunity (V_{IT-}) vs Overdrive

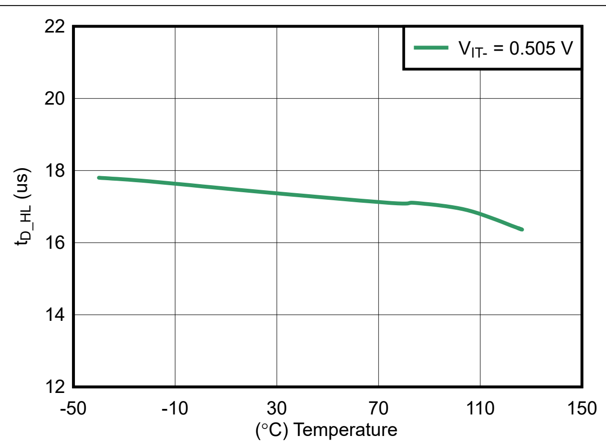


Figure 7-9. SENSE Delay (t_{D_HL}) vs Temperature

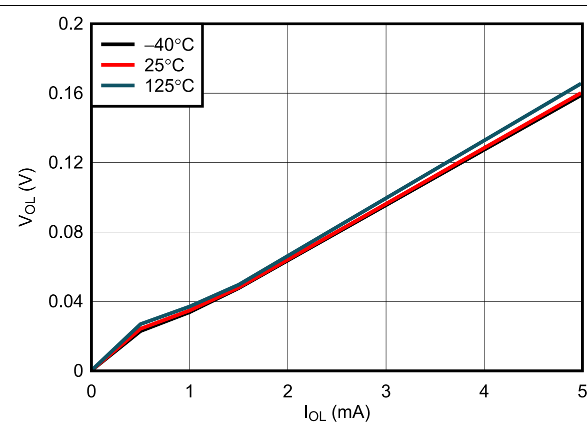


Figure 7-10. V_{OL} vs I_{OL}

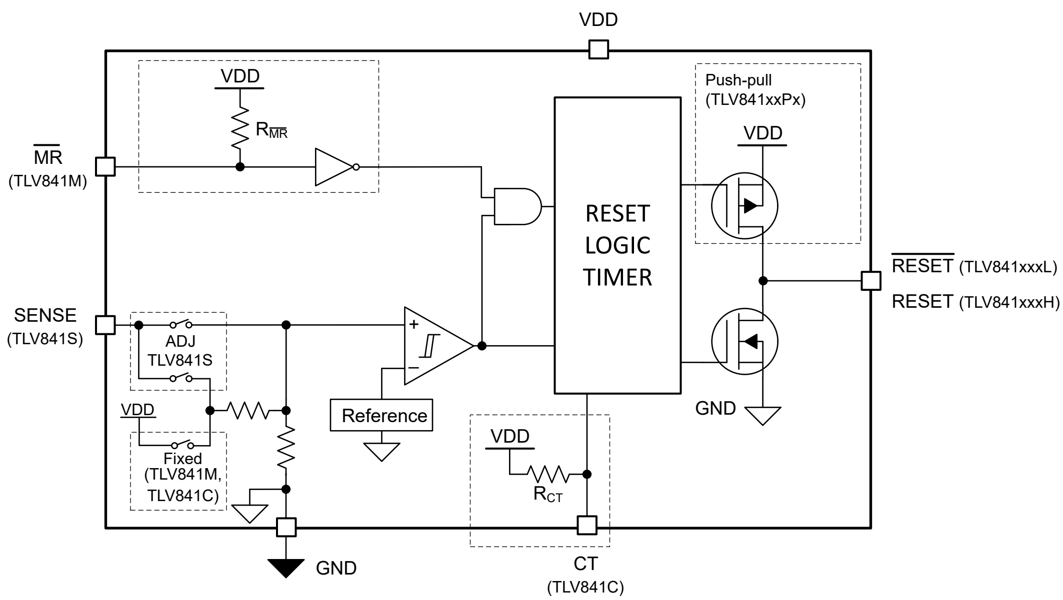
8 Detailed Description

8.1 Overview

The TLV841 is a family of very small, accurate, nano-quiescent current voltage supervisors with fixed threshold voltages. TLV841S features a separate SENSE pin for adjustable voltage threshold without losing accuracy, TLV841C features a programable reset time delay using external capacitor, and TLV841M features an active-low manual reset ($\overline{MR}$). The TLV841 family provide ±0.5% typical monitor threshold accuracy with hysteresis and glitch immunity.

The adjustable variant of TLV841S has an internal reference voltage of 0.505 V and can be used to accurately monitor any voltage above 0.505 V within the recommended operating conditions. In addition to the adjustable threshold variant, fixed negative threshold voltages (V_{IT-}) can be factory set from 0.8 V to 4.9 V in 100 mV steps. TLV841 is available in a very small (0.73 mm x 0.73 mm) 4-pin BGA package.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Voltage (VDD)

For TLV841C and TLV841M, the VDD pin is monitored by the internal comparator to indicate when VDD falls below the fixed threshold voltage. For TLV841S, the SENSE pin is monitored by the internal comparator. VDD also functions as the supply for the internal bandgap, internal regulator, state machine, buffers and other control logic blocks. Good design practice involve placing a 0.1 μF to 1 μF bypass capacitor at VDD input for noisy applications to ensure enough charge is available for the device to power up correctly.

8.3.1.1 VDD Hysteresis

The internal comparator has built-in hysteresis to avoid erroneous output reset release. If the voltage at the VDD (TLV841C, TLV841M) pin falls below V_{IT-} the output reset is asserted. When the monitored voltage goes above V_{IT-} plus hysteresis (V_{HYS}) the output reset is deasserted after t_D delay.

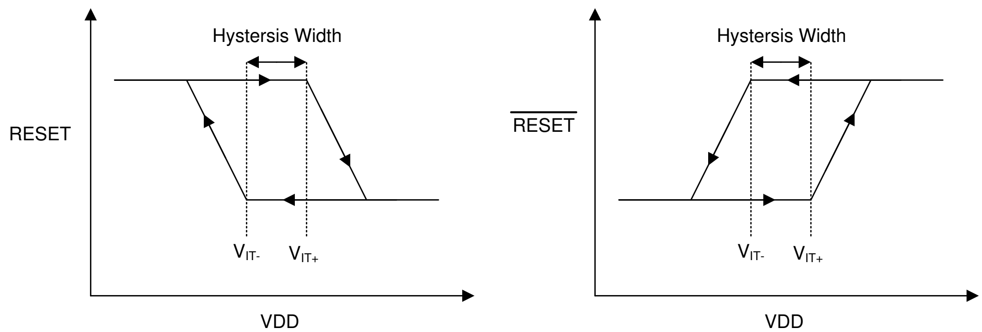


Figure 8-1. Hysteresis Diagram

8.3.1.2 VDD Transient Immunity

The TLV841 is immune to quick voltage transients or excursion on VDD. Sensitivity to transients depends on both pulse duration (t_{GI_VIT-}), specified in Section 7.6, and overdrive. Overdrive is defined by how much VDD deviates from the specified threshold. Threshold overdrive is calculated as a percent of the threshold in question, as shown in Equation 1.

$$\text{Overdrive} = |\,((V_{DD} / V_{IT-}) - 1) \times 100\%\,| \tag{1}$$

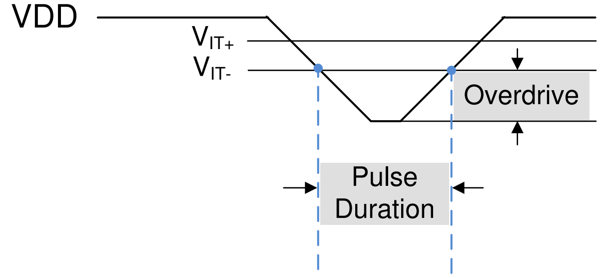


Figure 8-2. Overdrive vs Pulse Duration

8.3.2 SENSE Input (TLV841S)

The SENSE input can vary from 0 V to 5.5 V, regardless of the device supply voltage used. The SENSE pin is used to monitor a critical voltage rail or push-button input. If the voltage on this pin drops below V_{IT-}, then $\overline{\text{RESET}}$/RESET is asserted. When the voltage on the SENSE pin rises above the positive threshold voltage V_{IT-} + V_{HYS}, $\overline{\text{RESET}}$/RESET deasserts after the user-defined $\overline{\text{RESET}}$/RESET delay time. The internal comparator has built-in hysteresis to ensure well-defined $\overline{\text{RESET}}$/RESET assertions and deassertions even when there are small changes on the voltage rail being monitored.

The TLV841 device is relatively immune to short transients on the SENSE pin. Glitch immunity ($t_{GI\_V_{IT-}}$), specified in Section 7.6, is dependent on threshold overdrive, as illustrated in Figure 7-8. Although not required in most cases, for noisy applications, good analog design practice is to place a 10 nF to 100 nF bypass capacitor at the SENSE input to reduce sensitivity to transient voltages on the monitored signal.

8.3.2.1 SENSE Hysteresis

The internal comparator has built-in hysteresis to avoid erroneous output reset release. If the voltage at the SENSE (TLV841S) pin falls below V_{IT-} the output reset is asserted. When the monitored voltage goes above V_{IT-} plus hysteresis (V_{HYS}) the output reset is deasserted after t_D delay.

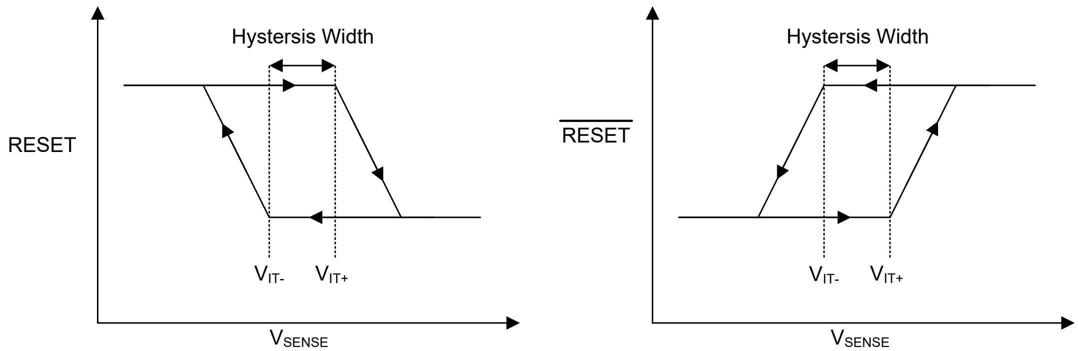


Figure 8-3. Hysteresis Diagram

8.3.2.2 Immunity to SENSE Pin Voltage Transients

The TLV841S is immune to short voltage transient spikes or excursion on the SENSE pin. To further improve the noise immunity on the SENSE pin, placing a 10 nF to 100 nF capacitor between the SENSE pin and GND can reduce the sensitivity to sensitivity to transient voltages on the monitored signal.

Sensitivity to transients depends on both transient duration and overdrive (amplitude) on the transient voltage. Overdrive is defined by how much V_{SENSE} exceeds the specified threshold and is important to know because the smaller the overdrive, the slower the resonse of the output. Threshold overdrive is calculated as a percent of the threshold in question, as shown in Equation 2.

$$\text{Overdrive} = | ((V_{SENSE} / V_{IT-}) - 1) \times 100\% | \quad (2)$$

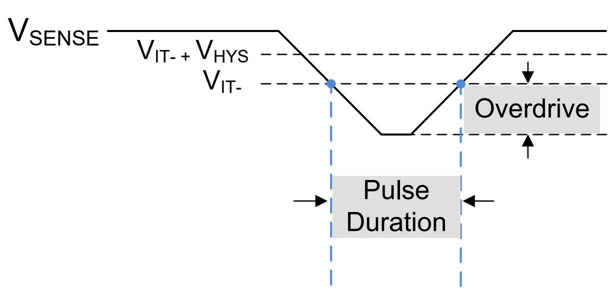


Figure 8-4. Overdrive vs Pulse Duration

8.3.3 User-Programmable Reset Time Delay for TLV841C only

The reset time delay can be set to a typical value of 40 µs by leaving the CT pin floating, or a maximum value of approximately 6.2 seconds by connecting 10 µF delay capacitor. The reset time delay (t_D) can be programmed by connecting a capacitor no larger than 10 µF between the CT pin and GND.

The relationship between external capacitor ($C_{CT\_EXT\ (typ)}$) in µF at CT pin and the time delay ($t_{D\ (typ)}$) in seconds is given by Equation 3.

$$t_{D\ (typ)} = -\ln(0.29) \times R_{CT\ (typ)} \times C_{CT\_EXT\ (typ)} + t_{D\ (no\ cap,\ typ)} \quad (3)$$

Equation 3 is simplified to Equation 4 by plugging $R_{CT\ (typ)}$ and $t_{D\ (no\ cap,\ typ)}$ given in *Section 7.5* and *Section 7.6*:

$$t_{D\ (typ)} = 618937 \times C_{CT\_EXT\ (typ)} + 40\ \mu s \quad (4)$$

Equation 5 solves for external capacitor value C_{CT_EXT} in units of µF where $t_{D\ (typ)}$ is in units of seconds

$$C_{CT\_EXT} = (t_{D\ (typ)} - 40\ \mu s) \div 618937 \quad (5)$$

The reset delay varies according to three variables: the external capacitor C_{CT_EXT}, CT pin internal resistance R_{CT} provided in Section 7.5, and a constant. The maximum variance due to the constant is show in Equation 6:

$$t_{D\ (max)} = -\ln(0.25) \times R_{CT\ (max)} \times C_{CT\_EXT\ (max)} + t_{D\ (no\ cap,\ max)} \quad (6)$$

The recommended maximum delay capacitor for the TLV841C is limited to 10 µF as this ensures enough time for the capacitor to fully discharge when a voltage fault occurs. Also, having a too large of a capacitor value can cause very slow charge up (rise times) and system noise can cause the the internal circuit to trip earlier or later near the threshold. This leads to variation in time delay where it can make the delay accuracy worse in the presence of system noise.

When a voltage fault occurs, the previously charged up capacitor discharges and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the delay will be shorter than expected. The capacitor will begin charging from a voltage above zero and resulting in shorter than expected time delay. A larger delay capacitor can be used so long as the capacitor has enough time to fully discharge during the duration of the voltage fault. The amount of time required to discharge the delay capacitor relative to the reset delay rises as VDD fault undervoltage increases as shown in Figure 8-5. From the graph below, to ensure the C_{CT_EXT} capacitor is fully discharged, the time period or duration of the voltage fault needs to be greater than 10% of the programmed reset time delay.

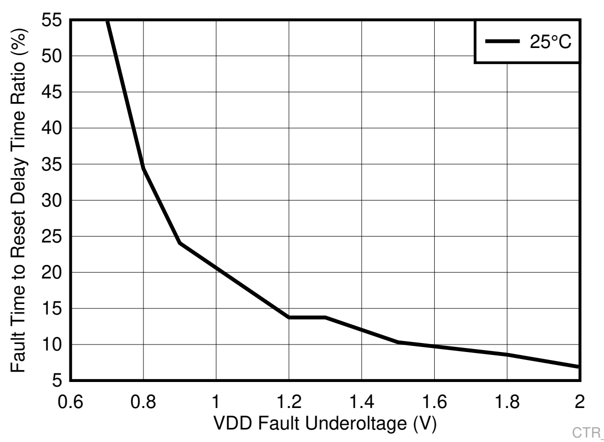


Figure 8-5. C_{CT_EXT} Discharge Time During Fault Condition (C_{CT_EXT} = 1 µF)

8.3.4 Manual Reset ($\overline{MR}$) Input for TLV841M only

The manual reset ($\overline{MR}$) input allows a processor GPIO or other logic circuits to initiate a reset. A logic low on $\overline{MR}$ with pulse duration longer than $t_{\overline{MR}\_RES}$ will causes reset output to assert. After $\overline{MR}$ returns to a logic high ($V_{\overline{MR}\_H}$) and VDD is above V_{IT+}, reset is deasserted after the user programmed reset time delay (t_D) expires.

If $\overline{MR}$ is not controlled externally, then $\overline{MR}$ can be left disconnected. If the logic signal controlling $\overline{MR}$ is less than VDD, then additional current flows from VDD into $\overline{MR}$ internally. For minimum current consumption, drive $\overline{MR}$ to either VDD or GND. $V_{\overline{MR}}$ should not be higher than VDD voltage.

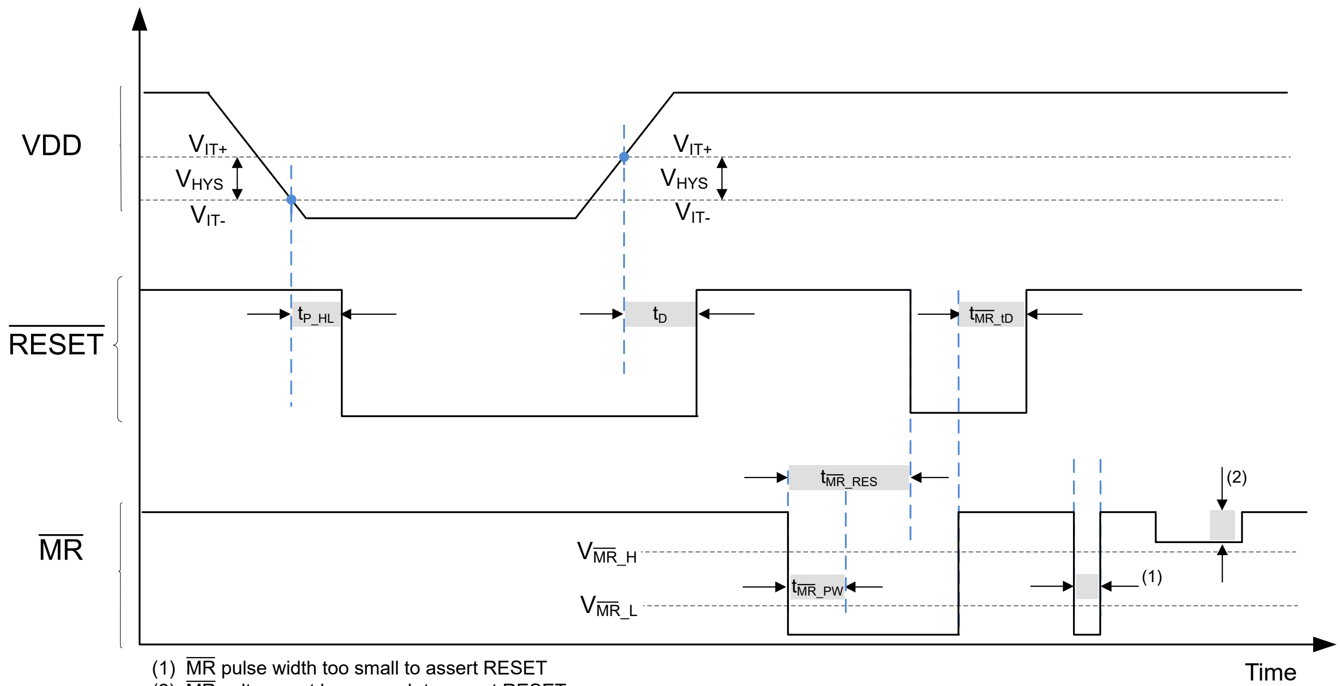


Figure 8-6. Timing Diagram $\overline{MR}$ and $\overline{RESET}$ (TLV841M)

8.3.5 Output Logic

8.3.5.1 $\overline{RESET}$ Output, Active-Low

$\overline{RESET}$ (Active-Low) applies to TLV841xxD**L** (Open-Drain) and TLV841xxP**L** (Push-Pull) hence the "**L**" in the device name. $\overline{RESET}$ remains high (deasserted) as long as VDD/SENSE is above the negative threshold (V_{IT-}) and the $\overline{MR}$ pin is floating or above $V_{\overline{MR}\_H}$. If VDD/SENSE falls below the negative threshold (V_{IT-}) or if $\overline{MR}$ is driven low, then $\overline{RESET}$ is asserted.

When $\overline{MR}$ is again logic high or floating and VDD/SENSE rise above V_{IT+} (V_{IT-} + V_{HYS}), the delay circuit will hold $\overline{RESET}$ low for the specified reset time delay (t_D). When the reset time delay has elapsed, the $\overline{RESET}$ pin goes back to logic high voltage V_{OH}.

The TLV841xx**D**L (Open-Drain) version, denoted with "**D**" in the device name, requires an external pull-up resistor to hold $\overline{RESET}$ pin high. Connect the external pull-up resistor to the desired pull-up voltage source and $\overline{RESET}$ can be pulled up to any voltage up to 5.5 V independent of the VDD voltage. To ensure proper voltage levels, give some consideration when choosing the external pull-up resistor values. The external pull-up resistor value determines the actual V_{OL}, the output capacitive loading, and the output leakage current ($I_{lkg(OD)}$).

The Push-Pull variant (TLV841xx**P**L), denoted with "**P**" in the device name, does not require an external pull-up resistor

8.3.5.2 RESET Output, Active-High

RESET (active-high), denoted with no bar above the pin label, applies only to TLV841xxD**H** (open-drain) and TLV841xxP**H** (push-pull) active-high version, hence the **"H"** in the device name. RESET remains low (deasserted) as long as VDD/SENSE is above the threshold (V_{IT-}) and the manual reset signal ($\overline{MR}$) is floating or above $V_{\overline{MR}\_H}$. If VDD/SENSE falls below the negative threshold (V_{IT-}) or if $\overline{MR}$ is driven low, then RESET is asserted driving the RESET pin to high voltage V_{OH}.

When $\overline{MR}$ is again logic high or floating and VDD/SENSE is above V_{IT+} (V_{IT-} + V_{HYS}) the delay circuit will hold RESET high for the specified reset time delay (t_D). When the reset time delay has elapsed, the RESET pin goes back to low voltage V_{OL}

The TLV841xx**D**H (Open-Drain) version, denoted with "**D**" in the device name, requires an external pull-up resistor to hold $\overline{RESET}$ pin high. Connect the external pull-up resistor to the desired pull-up voltage source and $\overline{RESET}$ can be pulled up to any voltage up to 5.5 V independent of the VDD voltage. To ensure proper voltage levels, give some consideration when choosing the external pull-up resistor values. The external pull-up resistor value determines the actual V_{OL}, the output capacitive loading, and the output leakage current ($I_{lkg(OD)}$).

The Push-Pull variant (TLV841xx**P**H), denoted with "**P**" in the device name, does not require an external pull-up resistor

8.4 Device Functional Modes

Table 8-1 and Table 8-2 summarizes the various functional modes of the device. Logic high is represented by "H" and logic low is represented by "L".

Table 8-1. Truth Table for TLV841S

VDD	SENSE	RESET (ACTIVE-HIGH)	$\overline{RESET}$ (ACTIVE-LOW)
$VDD < V_{POR}$	—	Undefined	Undefined
$V_{POR} < V_{DD} < V_{DD(MIN)}$ (1)	—	H	L
$VDD \geq V_{DD(MIN)}$	$V_{SENSE} < V_{IT-}$	H	L
$VDD \geq V_{DD(MIN)}$	$V_{SENSE} > V_{IT-} + V_{HYS}$	L	H

(1) When V_{DD} falls below $V_{DD(MIN)}$, undervoltage-lockout (UVLO) takes effect and $\overline{RESET}$ is held logic low (RESET is held logic high) until V_{DD} falls below V_{POR} at which the $\overline{RESET}$/RESET output is undefined.

Table 8-2. Truth Table for TLV841M

VDD	$\overline{MR}$	RESET (ACTIVE-HIGH)	$\overline{RESET}$ (ACTIVE-LOW)
$VDD < V_{POR}$	—	Undefined	Undefined
$V_{POR} < V_{DD} < V_{IT-}$	—	H	L
$VDD \geq V_{IT-}$	L	H	L
$VDD \geq V_{IT-}$	H	L	H
$VDD \geq V_{IT-}$	Floating	L	H

8.4.1 Normal Operation ($V_{DD} > V_{POR}$)

When VDD is greater than V_{POR}, the reset signal is determined by the voltage on the VDD pin with respect to the trip point (V_{IT-})

- $\overline{MR}$ high: The reset signal corresponds to VDD with respect to the threshold voltage.
- $\overline{MR}$ low: In this mode, the reset is asserted regardless of the threshold voltage.

8.4.2 Below Power-On-Reset ($V_{DD} < V_{POR}$)

When the voltage on VDD is lower than V_{POR}, the device does not have enough bias voltage to internally pull the asserted output low or high and reset voltage level is undefined.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

9.2 Typical Application

Design 1: Adjustable Voltage Supervisor with Push-Button Functionality

A typical application for the TLV841S is voltage rail monitoring with push-button functionality. In this design application, the TLV841SADL01 is being used to monitor a 3.3 V power rail and will trigger a reset when the voltage drops below 2.90 V or when the push-button is pressed. The reset output connects to an MCU for system resetting or servicing the push-button.

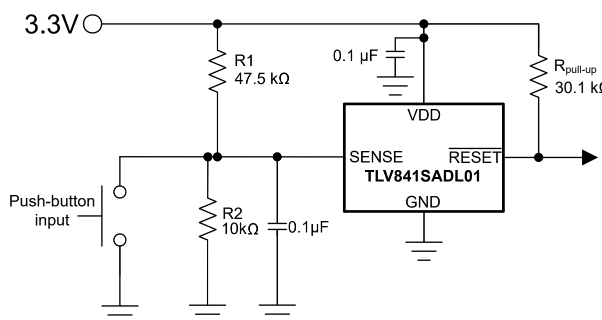


Figure 9-1. Design 1 - Adjustable Voltage Supervisor with Push-Button Functionality Circuit

9.2.1 Design Requirements

The design requirements, described in Table 9-1, for this design has a defined reset threshold voltage of 2.90 V, a reset delay of 40 µs and an output current no larger than 150 µA.

Table 9-1. Design Requirements

PARAMETER	DESIGN REQUIREMENTS	DESIGN RESULTS
Reset Asserting	Reset needs to assert when under the reset condition of a button press or VDD ≤ 2.90 V.	Reset asserted when under the reset condition of a button pressed or VDD ≤ 2.90 V.
Reset Asserting Timing	Reset output needs to assert when the reset conditions are met for 20 µs, and needs to de-assert after 40 µs of no reset conditions.	Reset output asserted when the reset conditions were met for 26.4 µs and deasserted after 46.8 µs of no reset conditions.
Output Current	The output current must not exceed 150 µA.	The output current was 110 µA under the reset condition.

9.2.2 Detailed Design Procedure

The TLV841SADL01 can monitor any voltage above 0.505 V using an external voltage divider. This device has a negative going input threshold voltage of 0.505 V; however, the design needs to assert a reset when VDD drops below 2.90 V. By using a resistor divider (R1 = 47.5 kΩ, R2 = 10 kΩ) the negative going threshold voltage becomes 2.90 V. The device's positive going voltage threshold is V_{IT-} + V_{HYS}. The typical V_{HYS} is 25 mV. This in combination with the resistor divider makes the design's positive going threshold voltage equal to 3.05 V. If VDD falls below 2.90 V, $\overline{\text{RESET}}$ will assert. If VDD rises above 3.05 V, $\overline{\text{RESET}}$ will deassert. See Figure 9-2 for a timing diagram detailing the voltage levels and reset assertion/deassertion conditions.

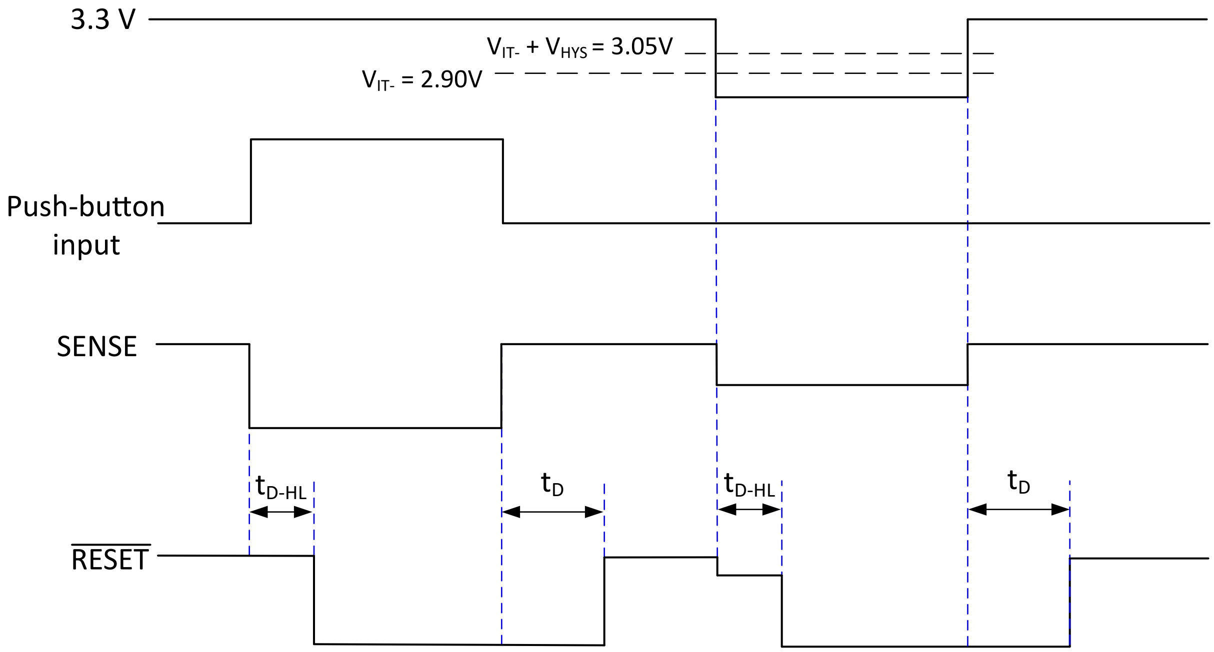


Figure 9-2. Design 1 Timing Diagram

This design will also enter a reset condition when the "push-button input" is asserted. The push-button is tied to ground and when pressed will drop the SENSE voltage to 0 V, making the device assert a reset. As a good analog practice, a 0.1 µF capacitor was also placed on VDD.

The desired reset timing conditions are sense propagation delay time (t_{P_HL} of 25 µs (how long it takes to assert $\overline{\text{RESET}}$) and a reset delay time of 40 µs (how long it takes to deassert $\overline{\text{RESET}}$). Figure 9-3 and Figure 9-4 are the results of the described application where the measured propagation delay and reset delay time are shown respectively.

For the requirement of a maximum output current, an external pull-up resistor needs to be selected so that the current through the external pull-up resistor exceeds no more than 150 µA. When the reset output is low, the voltage drop across the external pull-up resistor is equal to VDD. Ohm’s law is used to calculate the minimum resistor value. The resistor needs to be greater than 22 kΩ in order to pull less than 150 µA in the reset asserted low condition. A resistor value of 30.1 kΩ was selected to accomplish this.

Note that this design does not account for tolerances.

9.2.3 Application Curves: TLV841EVM

These application curves are taken with the TLV841SADL01 part on the TLV841EVM. Please see the TLV841 User Guide for more information.

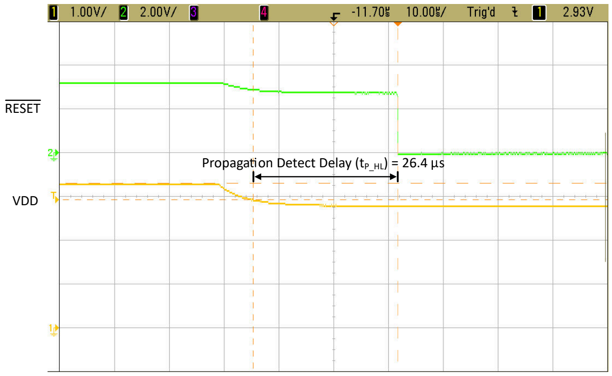


Figure 9-3. TLV841EVM Propagation Delay Time Delay (t_{D_HL})

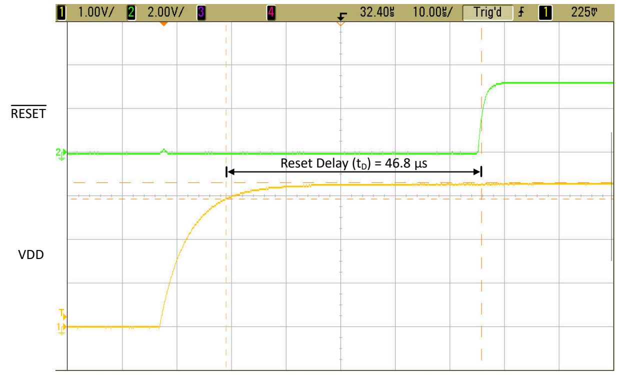


Figure 9-4. TLV841EVM $\overline{RESET}$ Time Delay (t_D)

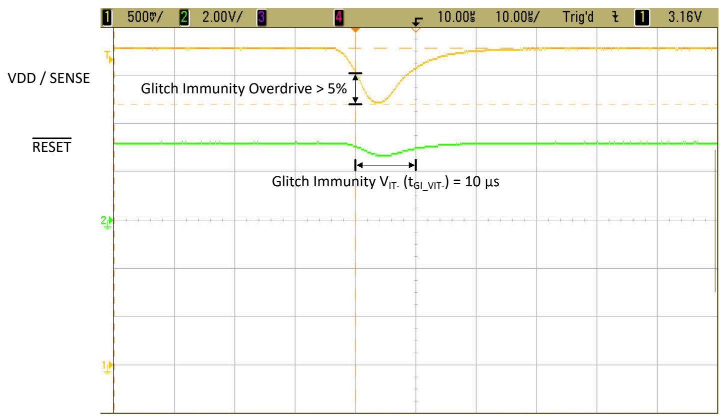


Figure 9-5. TLV841EVM SENSE Pin Glitch Immunity (t_{GI_VIT-})

10 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range between 0.7 V and 5.5 V. TI recommends an input supply capacitor of 0.1 µF between the VDD pin and GND pin. This device has a 6 V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 6 V, additional precautions must be taken.

11 Layout

11.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice recommends placing a minimum 0.1 µF ceramic capacitor as near as possible to the VDD pin. If a capacitor is not connected to the CT pin (TLV841C), then minimize parasitic capacitance on this pin so the rest time delay is not adversely affected.

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a greater than 0.1 µF ceramic capacitor as near as possible to the VDD pin.
- If a C_{CT_EXT} capacitor is used (TLV841C), place the capacitor as close as possible to the CT pin. If the CT pin is left unconnected, make sure to minimize the amount of parasitic capacitance on the pin to less than 5 pF.
- If a SENSE capacitor (C_{SENSE}) is used (TLV841S), place the capacitor as close as possible to the SENSE pin to further improve the noise immunity on the SENSE pin. Placing a 10 nF to 100 nF capacitor between the SENSE pin and GND can reduce the sensitivity to sensitivity to transient voltages on the monitored signal.
- Place the pull-up resistors on $\overline{\text{RESET}}$ pin as close to the pin as possible.

11.2 Layout Example

The layout example in Figure 11-1 shows how the TLV841S is laid out on a printed circuit board (PCB) for every device variant.

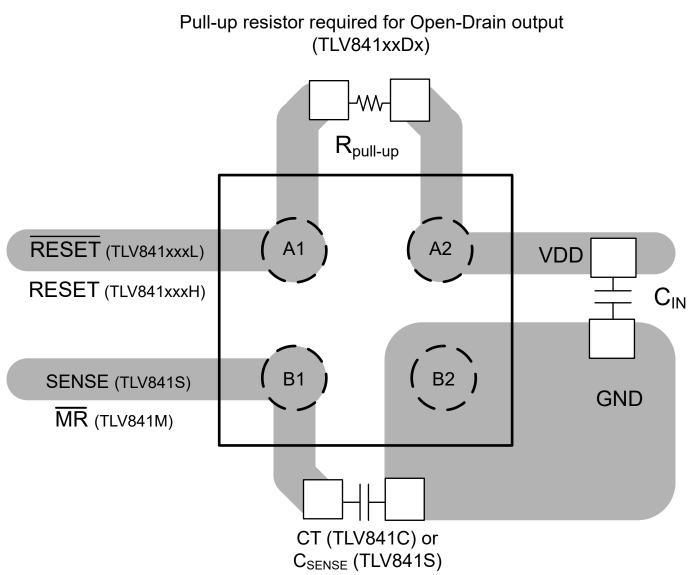


Figure 11-1. TLV841 Recommended Layout

12 Device and Documentation Support

12.1 Device Nomenclature

Figure 5-1 in Section 5 and Table 12-1 shows how to decode the function of the device based on its part number.

Table 12-1. Device Naming Convention

DESCRIPTION	NOMENCLATURE	VALUE
Generic Part number	TLV841	TLV841
Feature Option	S	SENSE pin option
	C	CT pin for programmable delay using external capacitor
	M	Manual Reset ($\overline{MR}$) pin option
Delay Option	A	40 µs (No internal reset time delay)
	B	2 ms reset time delay
	C	10 ms reset time delay
	D	30 ms reset time delay
	E	50 ms reset time delay
	F	80 ms reset time delay
	G	100 ms reset time delay
	H	150 ms reset time delay
	I	200 ms reset time delay
Variant code (Output Topology)	DL	Open-Drain, Active-Low
	PL	Push-Pull, Active-Low
	DH	Open-Drain, Active-High
	PH	Push-Pull, Active-High
Detect Voltage Option	## (two characters)	Example: 12 stands for 1.2 V threshold
Package	YBH	DSBGA (4)
Reel	R	Large Reel

12.2 Documentation Support

12.2.1 Related Documentation

The following related documents are available for download at www.ti.com:

- *Optimizing Resistor Dividers at a Comparator Input*, SLVA450
- *Sensitivity Analysis for Power Supply Design*, SLVA481
- *Getting Started With TMS320C28x Digital Signal Controllers*, SPRAAM0
- TLV841EVM-775 Evaluation Module User Guide, SBVU030
- C2000 Delfino Family of Microprocessors
- TMS320F2833x microcontroller, SPRS439

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 Trademarks

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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV841SADL01YBHR	ACTIVE	DSBGA	YBH	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9	Samples
TLV841SADL41YBHR	ACTIVE	DSBGA	YBH	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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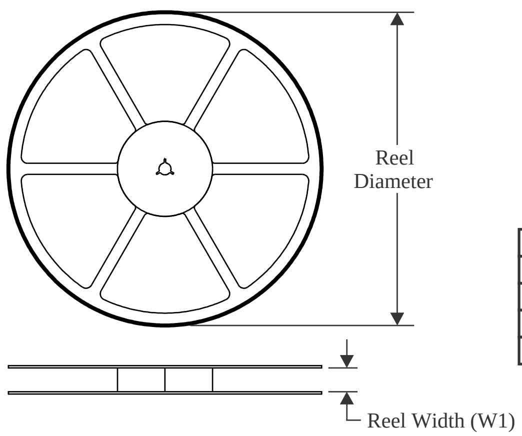
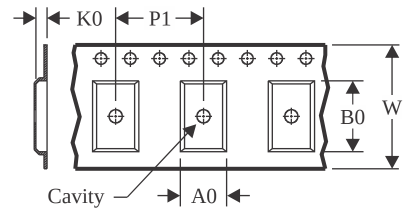
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

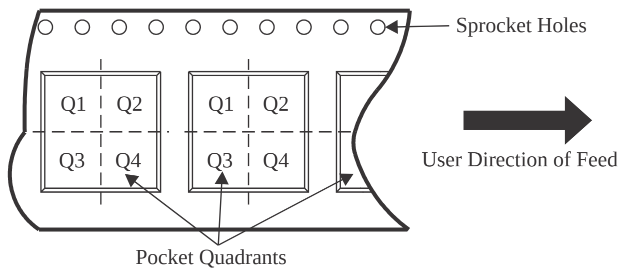


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

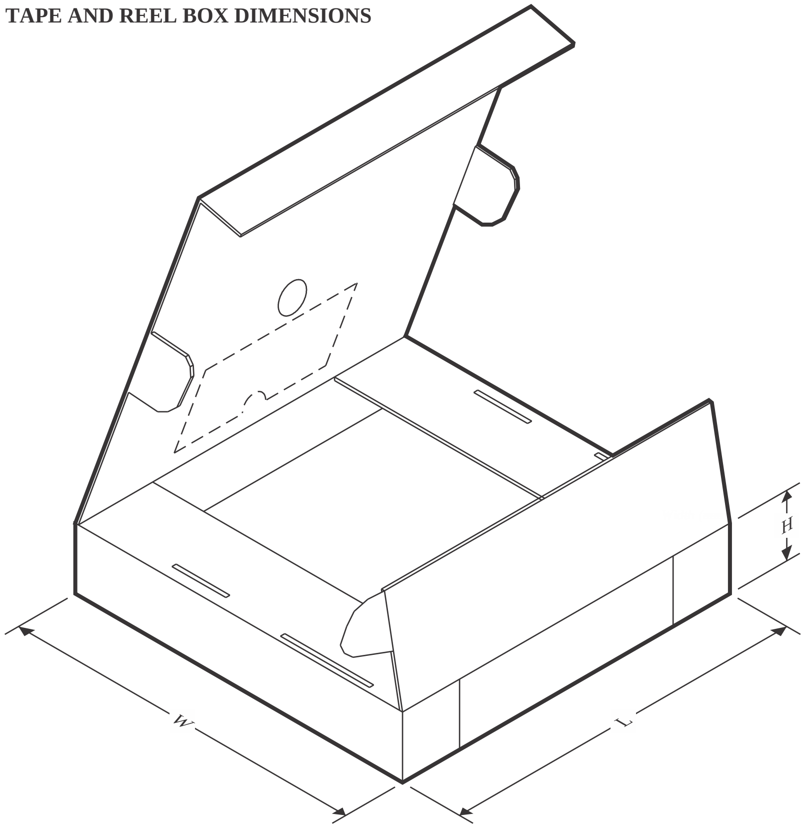
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

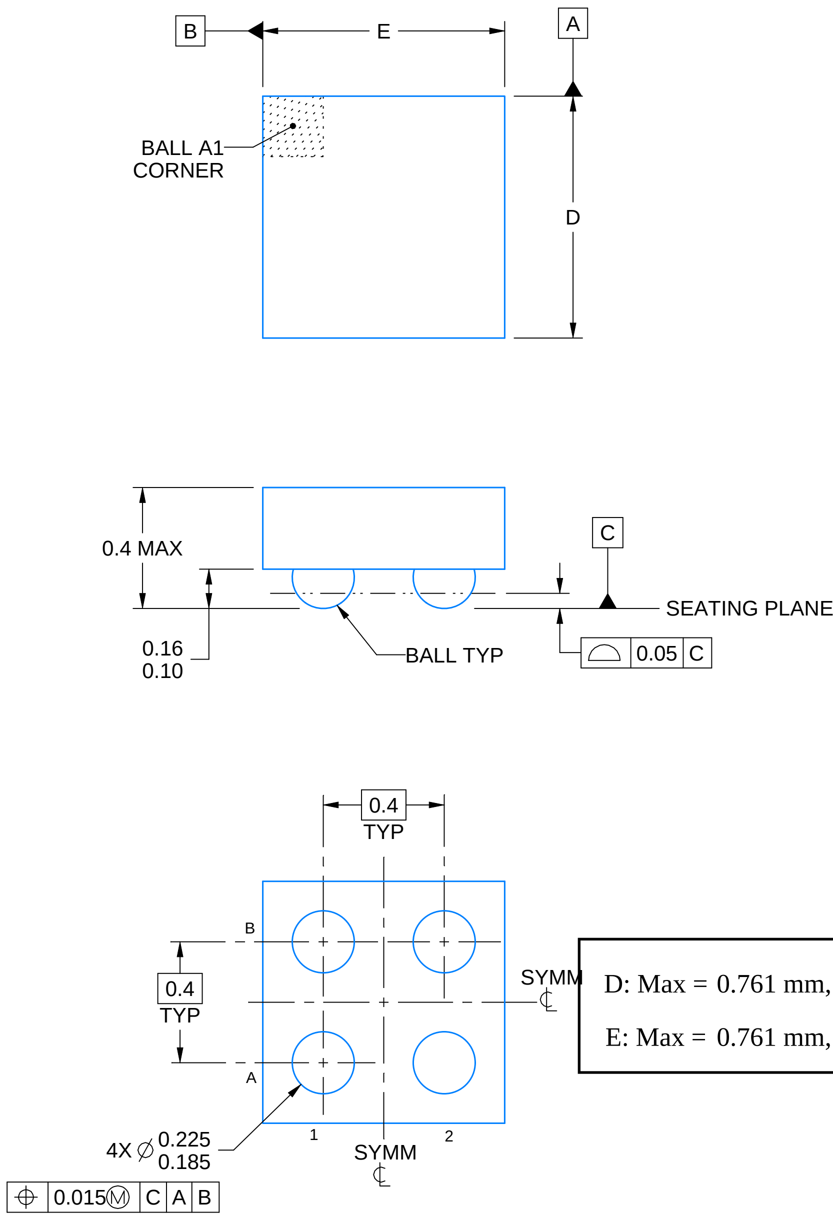
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV841SADL01YBHR	DSBGA	YBH	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV841SADL41YBHR	DSBGA	YBH	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV841SADL01YBHR	DSBGA	YBH	4	3000	182.0	182.0	20.0
TLV841SADL41YBHR	DSBGA	YBH	4	3000	182.0	182.0	20.0



D: Max = 0.761 mm, Min =0.701 mm
E: Max = 0.761 mm, Min =0.701 mm

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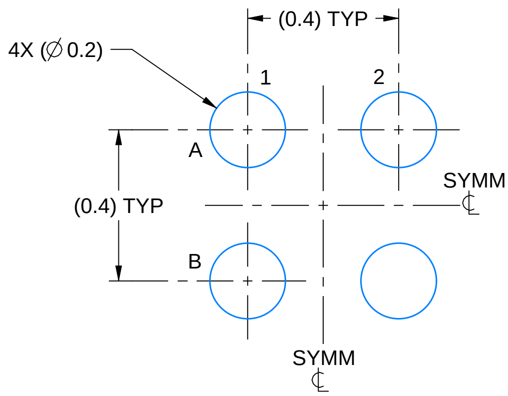
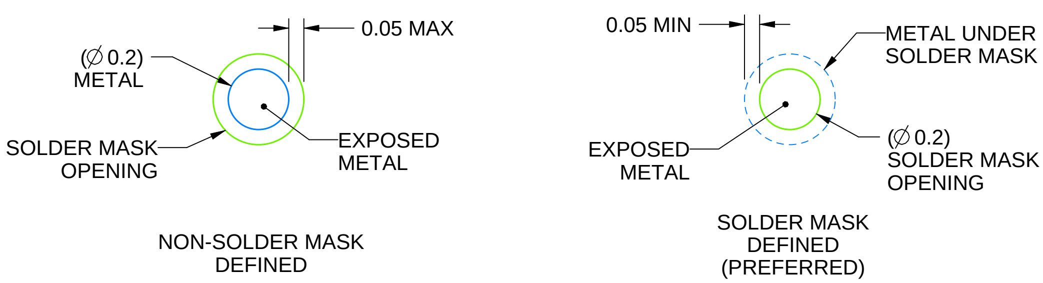
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

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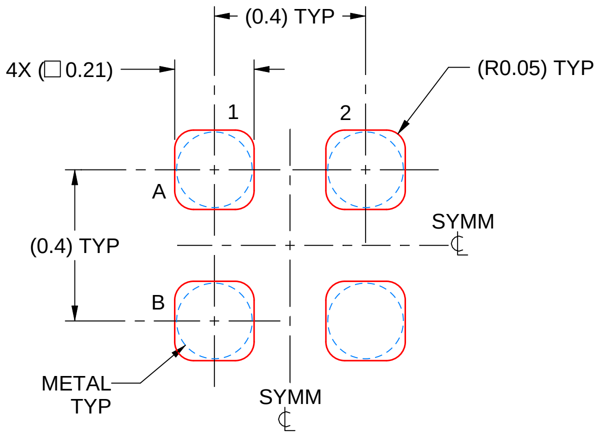
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.