



TPS7A33 –36-V, 1-A, Ultralow-Noise Negative Voltage Regulator

1 Features

- Input Voltage Range: –3 V to –36 V
- Noise:
 - 16 μV_{RMS} (10 Hz to 100 kHz)
- Power-Supply Ripple Rejection:
 - 72 dB (10 kHz)
- Adjustable Output: –1.18 V to –33 V
- Maximum Output Current: 1 A
- Stable With Ceramic Capacitors $\geq 10 \mu\text{F}$
- Built-In Current-Limit and Thermal Shutdown Protection
- Available in an External Heatsink-Capable, High Thermal Performance TO-220 Package
- Operating Temperature Range: –40°C to 125°C

2 Applications

- Supply Rails for Operational Amplifiers, DACs, ADCs, and Other High-Precision Analog Circuitry
- Audio
- Post DC-DC Converter Regulation and Ripple Filtering
- Test and Measurement
- Medical
- Industrial Instrumentation
- Base Stations and Telecom Infrastructure
- 12-V and 24-V Industrial Buses

3 Description

The TPS7A33 series of linear regulators are negative voltage (–36 V), ultralow-noise (16- μV_{RMS} , 72-dB PSRR) linear regulators capable of sourcing a maximum load of 1 A.

The TPS7A33 series include a complementary metal oxide semiconductor (CMOS) logic-level-compatible enable pin (EN) to allow for user-customizable power management schemes. Other features available include built-in current limit and thermal shutdown features to protect the device and system during fault conditions.

The TPS7A33 family is designed using bipolar technology primarily for high-accuracy, high-precision instrumentation applications, where clean voltage rails are critical to maximize system performance. This feature makes it ideal to power operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other high-performance analog circuitry.

In addition, the TPS7A33 family of linear regulators is suitable for post DC-DC converter regulation. By filtering out the output voltage ripple inherent to DC-DC switching conversion, maximum system performance is ensured in sensitive instrumentation, medical, test and measurement, audio, and RF applications.

For applications where positive and negative high-performance rails are required, consider the [TPS7A4700](#) positive high-voltage, ultralow-noise, low-dropout linear regulator as well.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A33	TO-220 (7)	10.17 mm × 8.38 mm
	VQFN (20)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic

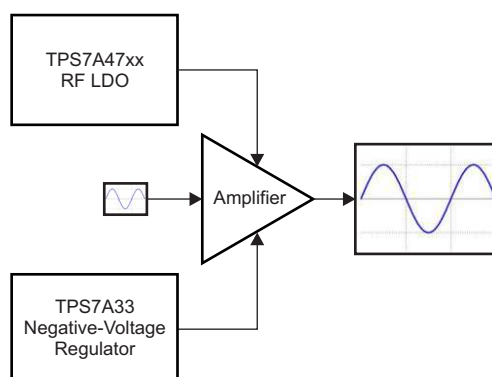


Table of Contents

1 Features	1	8 Application and Implementation	15
2 Applications	1	8.1 Application Information	15
3 Description	1	8.2 Typical Application	18
4 Revision History	2	8.3 Do's and Don'ts	20
5 Pin Configuration and Functions	4	9 Power Supply Recommendations	21
6 Specifications	5	10 Layout	21
6.1 Absolute Maximum Ratings	5	10.1 Layout Guidelines	21
6.2 ESD Ratings	5	10.2 Layout Example	21
6.3 Recommended Operating Conditions	5	10.3 Thermal Performance and Heat Sink Selection	24
6.4 Thermal Information	5	10.4 Package Mounting	25
6.5 Electrical Characteristics	6	11 Device and Documentation Support	25
6.6 Typical Characteristics	7	11.1 Device Support	25
7 Detailed Description	12	11.2 Documentation Support	25
7.1 Overview	12	11.3 Trademarks	25
7.2 Functional Block Diagram	12	11.4 Electrostatic Discharge Caution	25
7.3 Feature Description	12	11.5 Glossary	25
7.4 Device Functional Modes	14	12 Mechanical, Packaging, and Orderable Information	26

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (February 2013) to Revision D	Page
Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section	1
Corrected title of data sheet to show accurate maximum output current; changed "–1 A" to "1-A"	1
Changed front-page figures and deleted note stating that RGW package was product preview	1
Changed Pin Configuration and Functions section; updated table format and deleted footnote about RGW product-preview status	4
Deleted footnote from Pin Functions table indicating RGW product-preview status	4
Deleted footnote (2) from Absolute Maximum Ratings table	5
Deleted note from Thermal Information table stating that RGW package was product preview	5
Corrected condition values for Figure 23	9
Corrected condition values for Figure 24	9
Corrected condition values and trace indicators for Figure 25	10
Corrected condition values and trace indicators for Figure 26	10
Changed C _{SS} value from 1 μ F to 10 nF in Figure 27	10
Deleted Parametric Measurement Information section	12
Revised Functional Block Diagram	12
Changed first paragraph of Adjustable Operation section stating the device output voltage range	15
Changed Equation 2 for clarity	15
Changed last sentence of Capacitor Recommendations section	16
Changed noise reduction capacitor value from 1 μ F to 10 nF in first paragraph of Power-Supply Rejection section	17
Revised last paragraph of Power-Supply Rejection section	17
Changed noise reduction capacitor value from 1 μ F to 10 nF in second paragraph of Output Noise section	17
Added footnote (1) to Figure 32	18
Changed title for Figure 41	23
Changed title for Figure 42	23

Revision History (continued)

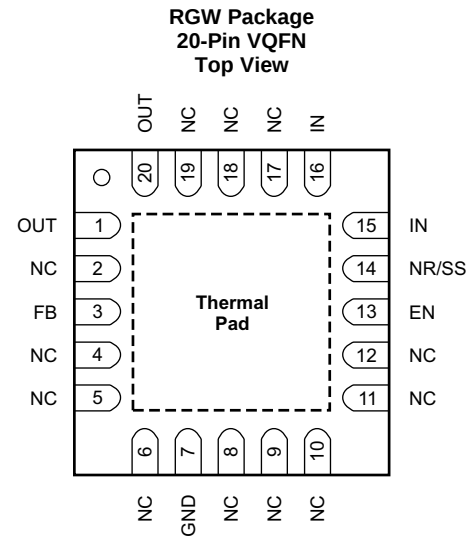
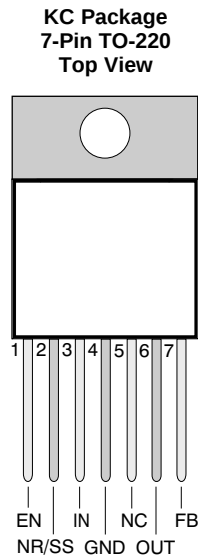
- Changed *Power Dissipation* section title to *Layout Guidelines for Thermal Performance and Heat Sink Selection* 24
- Revised wording in *Layout Guidelines for Thermal Performance* section for clarification 24

Changes from Revision B (March 2012) to Revision C	Page
• Changed product status from Mixed Status to Production Data	1
• Added last paragraph in <i>Description</i> section.....	1
• Changed typical application block diagram	1
• Updated Figure 31	17

Changes from Revision A (December 2011) to Revision B	Page
• Changed product status from Production Data to Mixed Status	1
• Added RGW pinout drawing	1
• Added RGW pinout drawing to <i>Pin Configuration and Functions</i> section	4
• Added RGW and footnote 1 to Pin Functions table	4
• Added RGW column to <i>Thermal Information</i> table.....	5

Changes from Original (December 2011) to Revision A	Page
• Changed product status from Product Preview to Production Data	1

5 Pin Configuration and Functions



Pin Functions

NAME	PIN		I/O	DESCRIPTION
	TO-220	VQFN		
EN	1	13	I	This pin turns the regulator on or off. If $V_{EN} \geq V_{EN(+HI)}$ or $V_{EN} \leq V_{EN(-HI)}$, the regulator is enabled. If $V_{EN(+LO)} \geq V_{EN} \geq V_{EN(-LO)}$, the regulator is disabled. The EN pin can be connected to IN, if not used. $ V_{EN} \leq V_{IN} $.
FB	7	3	I	This pin is the input to the control-loop error amplifier. It is used to set the output voltage of the device. TI recommends connecting a 10-nF capacitor from FB to OUT (as close to the device as possible) to maximize AC performance.
GND	4	7	—	Ground
IN	3	15, 16	I	Input supply. A capacitor greater than or equal to 10 nF must be tied from this pin to ground to assure stability. It is recommended to connect a 10- μ F capacitor from IN to GND (as close to the device as possible) to reduce circuit sensitivity to printed-circuit-board (PCB) layout, especially when long input traces or high source impedances are encountered.
NC	5	2, 4-6, 8-12, 17-19	—	This pin can be left open or tied to any voltage between GND and IN.
NR/SS	2	14	—	Noise reduction pin. A capacitor connected from this pin to GND controls the soft-start function and allows RMS noise to be reduced to very low levels. TI recommends connecting a 1- μ F capacitor from NR/SS to GND (as close to the device as possible) to filter the noise generated by the internal bandgap and maximize ac performance.
OUT	6	1, 20	O	Regulator output. A capacitor greater than or equal to 10 μ F must be tied from this pin to ground to assure stability. TI recommends connecting a 47- μ F ceramic capacitor from OUT to GND (as close to the device as possible) to maximize ac performance.
Thermal Pad	Tab	—	—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND. An external heatsink can be installed to provide additional thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Voltage	IN pin to GND pin	–36	0.3	V
	OUT pin to GND pin	–33	0.3	
	OUT pin to IN pin	–0.3	36	
	FB pin to GND pin	–2	0.3	
	FB pin to IN pin	–0.3	36	
	EN pin to GND pin	–36	10	
	NR/SS pin to IN pin	–0.3	36	
	NR/SS pin to GND pin	–2	0.3	
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T_J	–40	150	°C
	Storage temperature, T_{stg}	–65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±1000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	–35		–3	V
V_{EN}	Enable supply voltage	V_{IN}		10	V
V_{OUT}	Output voltage	–33.2		V_{REF}	V
I_{OUT}	Output current	0		1	A
$R_2^{(1)}$	R_2 is the lower feedback resistor			240	kΩ
C_{IN}	Input capacitor	10	47		μF
C_{OUT}	Output capacitor	10	47		μF
C_{NR}	Noise reduction capacitor		1		μF
C_{FF}	Feed-forward capacitor		10		nF
T_J	Operating junction temperature	–40		125	°C

- (1) This condition helps ensure stability at no load.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS7A33		UNIT
		KC (TO-220)	RGW (VQFN)	
		7 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.2	33.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	40	30.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	17.4	12.5	
Ψ_{JT}	Junction-to-top characterization parameter	6.4	0.4	
Ψ_{JB}	Junction-to-board characterization parameter	17.2	12.5	
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	0.8	2.4	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

TPS7A33

SBVS169D –DECEMBER 2011–REVISED APRIL 2015

www.ti.com

6.5 Electrical Characteristics

At $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$, $|V_{IN}| = |V_{OUT(nom)}| + 1\text{ V}$ or $|V_{IN}| = 3\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 10\text{ }\mu\text{F}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $C_{NR/SS} = 0\text{ nF}$, and FB tied to OUT, unless otherwise noted.⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		-35		-3	V
V_{REF}	Internal reference	$T_J = 25^{\circ}\text{C}$, $V_{FB} = V_{REF}$	-1.192	-1.175	-1.157	V
V_{UVLO}	Undervoltage lockout threshold			-2		V
V_{OUT}	Output voltage range ⁽²⁾	$ V_{IN} \geq V_{OUT(nom)} + 1\text{ V}$	-33.2		V_{REF}	V
	Nominal accuracy	$T_J = 25^{\circ}\text{C}$, $ V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$	-1.5		1.5	% V_{OUT}
	Overall accuracy	$5\text{ V} \leq V_{IN} \leq 35\text{ V}$ $1\text{ mA} \leq I_{OUT} \leq 1\text{ A}$ $ V_{OUT(nom)} + 1\text{ V} \leq V_{IN} \leq 35\text{ V}$ $1\text{ mA} \leq I_{OUT} \leq 1\text{ A}$		± 1		% V_{OUT}
$\Delta V_{OUT(\Delta V)}$	Line regulation	$ V_{OUT(nom)} + 1\text{ V} \leq V_{IN} \leq 35\text{ V}$		0.14		% V_{OUT}
$\Delta V_{OUT(\Delta I)}$	Load regulation	$1\text{ mA} \leq I_{OUT} \leq 1\text{ A}$		0.4		% V_{OUT}
$ V_{DO} $	Dropout voltage	$V_{IN} = 95\% V_{OUT(nom)}$, $I_{OUT} = 500\text{ mA}$		290		mV
		$V_{IN} = 95\% V_{OUT(nom)}$, $I_{OUT} = 1\text{ A}$		325	800	
I_{CL}	Current limit	$V_{OUT} = 90\% V_{OUT(nom)}$		1900		mA
I_{GND}	Ground current	$I_{OUT} = 0\text{ mA}$		210	350	μA
		$I_{OUT} = 500\text{ mA}$		5		mA
$ I_{SHDN} $	Shutdown supply current	$V_{EN} = +0.4\text{ V}$		1	3	μA
		$V_{EN} = -0.4\text{ V}$		1	3	
I_{FB}	Feedback current ⁽³⁾			14	100	nA
$ I_{EN} $	Enable current	$V_{EN} = V_{IN} = V_{OUT(nom)} + 1\text{ V}$		0.48	1	μA
		$V_{IN} = V_{EN} = -35\text{ V}$		0.51	1	
		$V_{IN} = -35\text{ V}$, $V_{EN} = +10\text{ V}$		0.5	1	
$V_{EN(+HI)}$	Positive enable high-level voltage		2		10	V
$V_{EN(+LO)}$	Positive enable low-level voltage		0		0.4	V
$V_{EN(-HI)}$	Negative enable high-level voltage		V_{IN}		-2	V
$V_{EN(-LO)}$	Negative enable low-level voltage		-0.4		0	V
V_n	Output noise voltage	$V_{IN} = -3\text{ V}$, $V_{OUT(nom)} = V_{REF}$, $C_{OUT} = 22\text{ }\mu\text{F}$, $C_{NR/SS} = 10\text{ nF}$, BW = 10 Hz to 100 kHz		16		μV_{RMS}
PSRR	Power-supply rejection ratio	$V_{IN} = -6.2\text{ V}$, $V_{OUT(nom)} = -5\text{ V}$, $C_{OUT} = 22\text{ }\mu\text{F}$, $C_{NR/SS} = 10\text{ nF}$, C_{FF} ⁽⁴⁾ = 10 nF, f = 10 kHz		72		dB
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		170		$^{\circ}\text{C}$
		Reset, temperature decreasing		150		$^{\circ}\text{C}$
T_J	Operating junction temperature		-40		125	$^{\circ}\text{C}$

(1) At operating conditions, $V_{IN} \leq 0\text{ V}$, $V_{OUT(nom)} \leq V_{REF} \leq 0\text{ V}$. At regulation, $V_{IN} \leq V_{OUT(nom)} - |V_{DO}|$. $I_{OUT} > 0$ flows from OUT to IN.

(2) To ensure stability at no load conditions, a current from the feedback resistive network equal to or greater than 5 μA is required.

(3) $I_{FB} > 0$ flows into the device.

(4) C_{FF} refers to a feed-forward capacitor connected between the FB and OUT pins.

6.6 Typical Characteristics

At $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$, $|V_{IN}| = |V_{OUT(nom)}| + 1\text{ V}$ or $|V_{IN}| = 3\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 22\text{ }\mu\text{F}$, $C_{OUT} = 22\text{ }\mu\text{F}$, $C_{NR/SS} = 0\text{ nF}$, and the FB pin tied to OUT, unless otherwise noted.

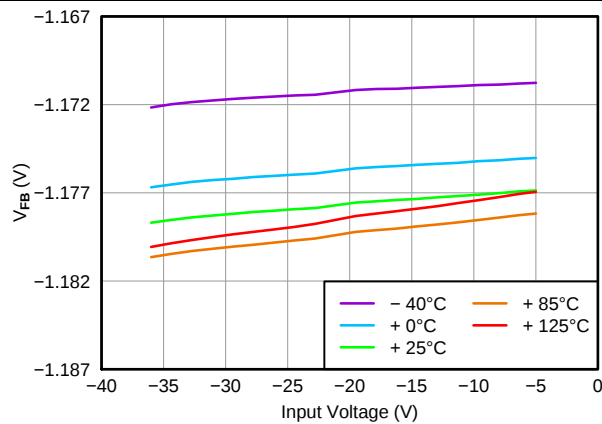


Figure 1. Feedback Voltage vs Input Voltage

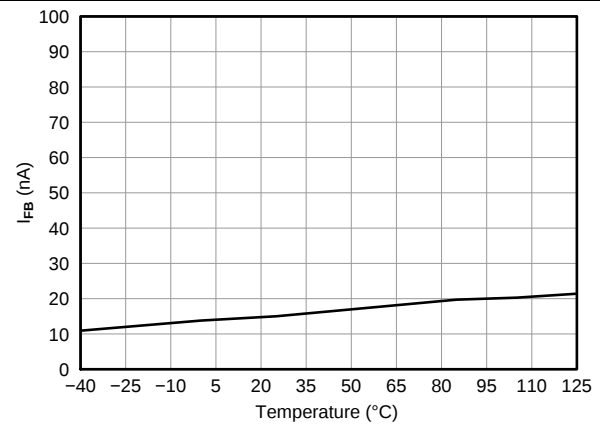


Figure 2. Feedback Current vs Temperature

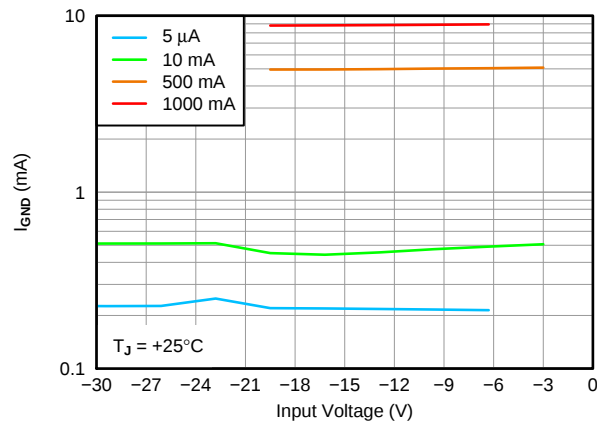


Figure 3. Ground Current vs Input Voltage

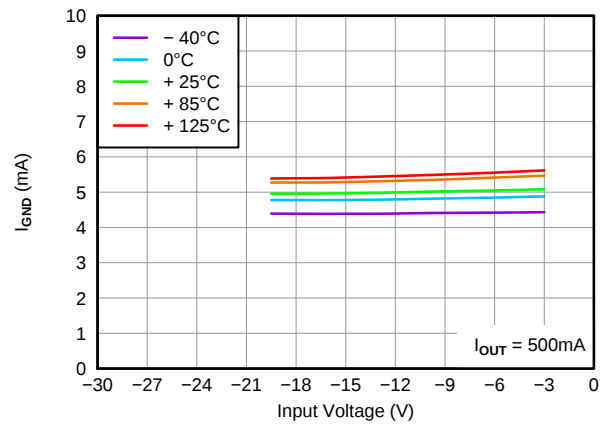


Figure 4. Ground Current vs Input Voltage

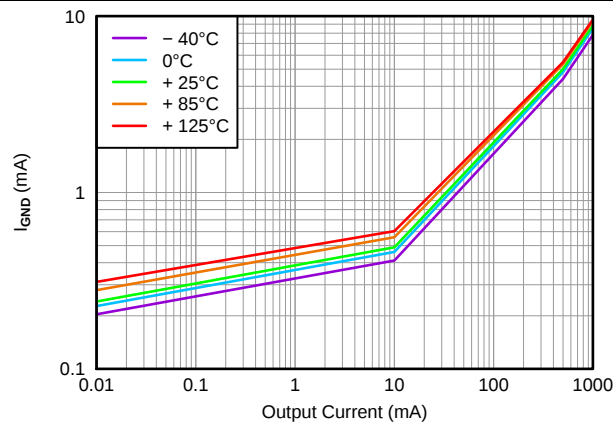


Figure 5. Ground Current vs Output Current

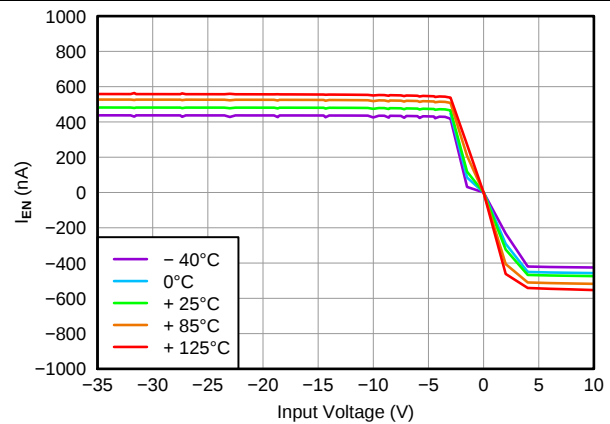
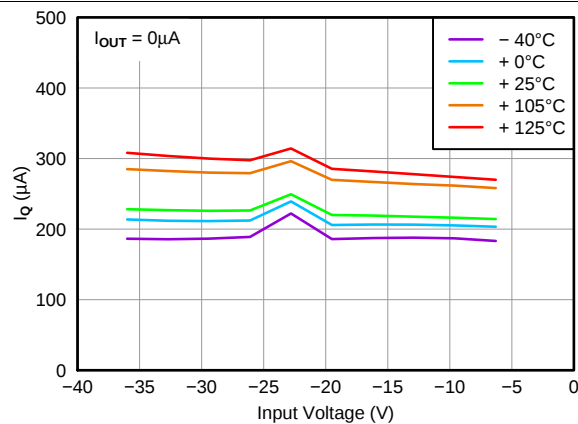
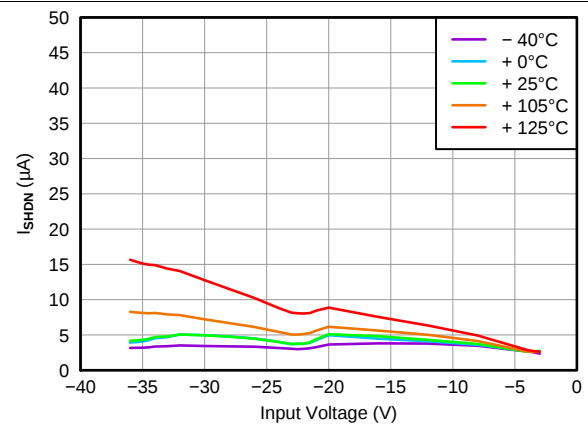
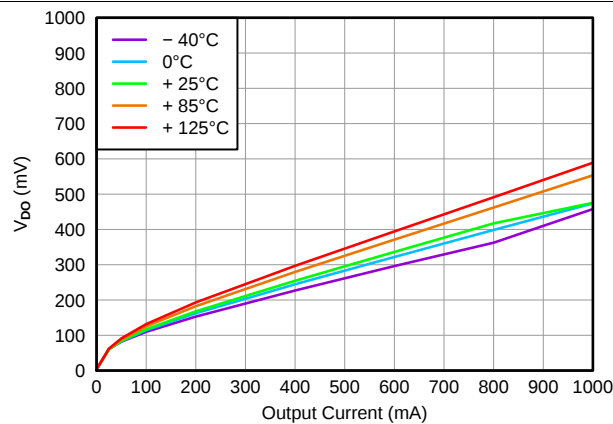
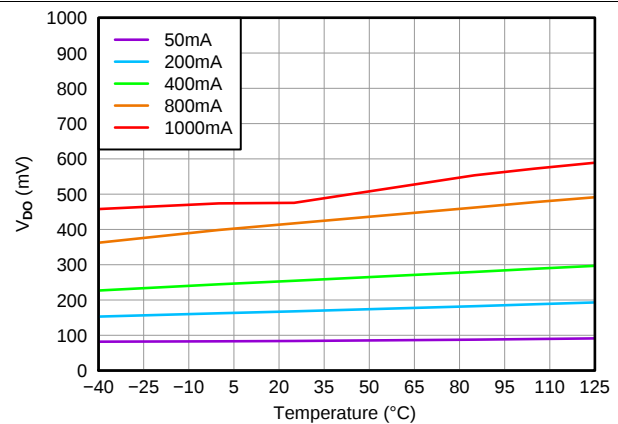
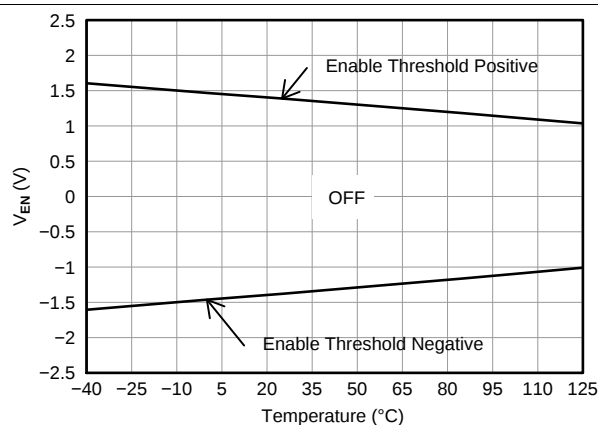
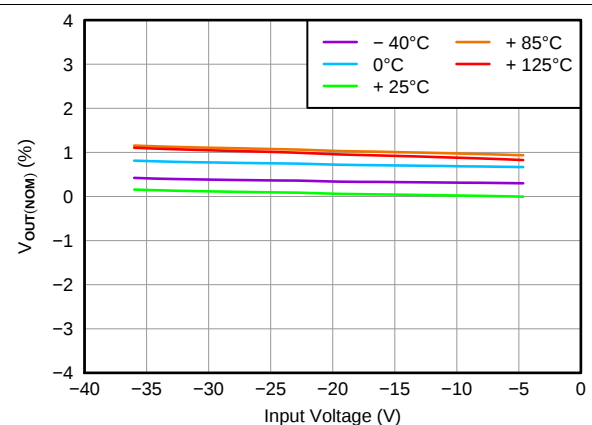


Figure 6. Enable Current vs Enable Voltage

Typical Characteristics (continued)

At $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$, $|V_{IN}| = |V_{OUT(nom)}| + 1\text{ V}$ or $|V_{IN}| = 3\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 22\text{ }\mu\text{F}$, $C_{OUT} = 22\text{ }\mu\text{F}$, $C_{NR/SS} = 0\text{ nF}$, and the FB pin tied to OUT, unless otherwise noted.


Figure 7. Quiescent Current vs Input Voltage

Figure 8. Shutdown Current vs Input Voltage

Figure 9. Dropout Voltage vs Output Current

Figure 10. Dropout Voltage vs Temperature

Figure 11. Enable Threshold Voltage vs Temperature

Figure 12. Line Regulation

Typical Characteristics (continued)

At $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$, $|V_{IN}| = |V_{OUT(nom)}| + 1\text{ V}$ or $|V_{IN}| = 3\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 22\text{ }\mu\text{F}$, $C_{OUT} = 22\text{ }\mu\text{F}$, $C_{NR/SS} = 0\text{ nF}$, and the FB pin tied to OUT, unless otherwise noted.

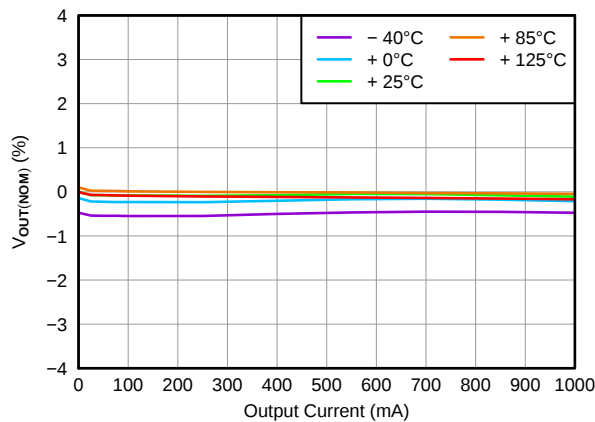


Figure 13. Load Regulation

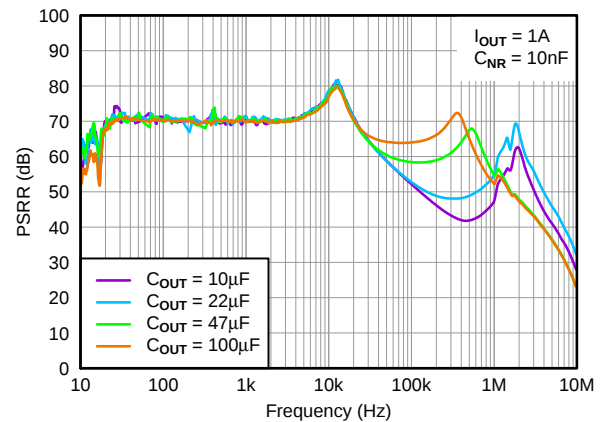


Figure 14. Power-Supply Rejection Ratio vs C_{OUT}

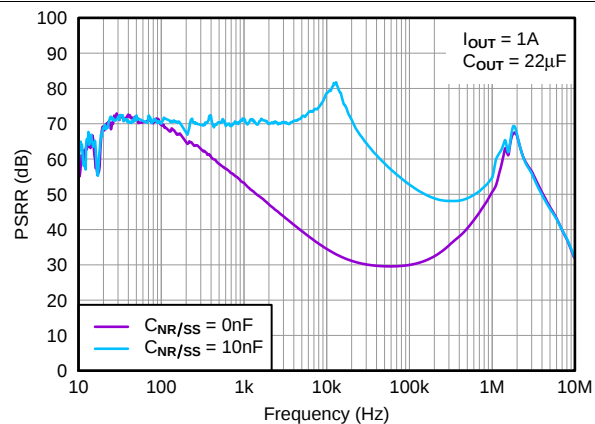


Figure 15. Power-Supply Rejection Ratio vs $C_{NR/SS}$

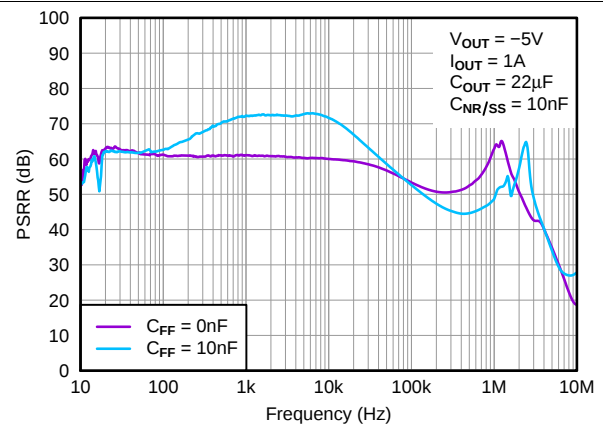


Figure 16. Power-Supply Rejection Ratio vs C_{FF}

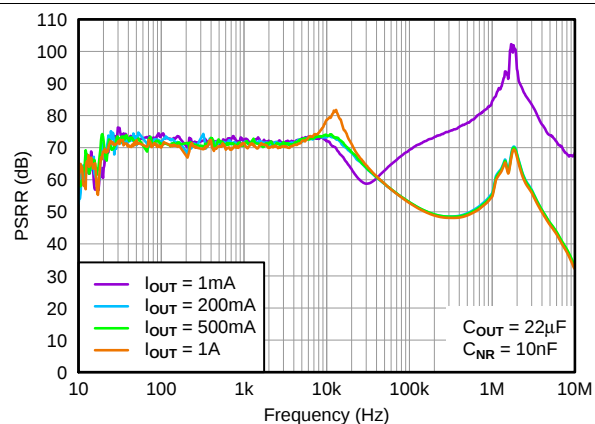


Figure 17. Power-Supply Rejection Ratio vs I_{OUT}

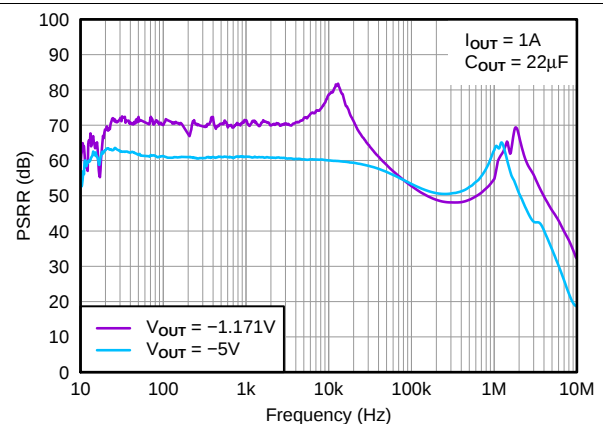


Figure 18. Power-Supply Rejection Ratio vs V_{OUT}

Typical Characteristics (continued)

At $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$, $|V_{IN}| = |V_{OUT(nom)}| + 1\text{ V}$ or $|V_{IN}| = 3\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 22\text{ }\mu\text{F}$, $C_{OUT} = 22\text{ }\mu\text{F}$, $C_{NR/SS} = 0\text{ nF}$, and the FB pin tied to OUT, unless otherwise noted.

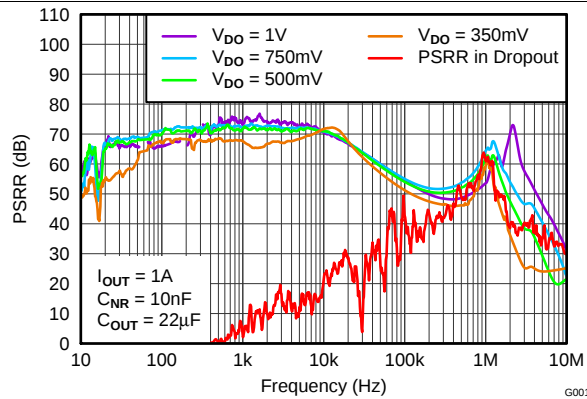


Figure 19. Power-Supply Rejection Ratio vs V_{DO}

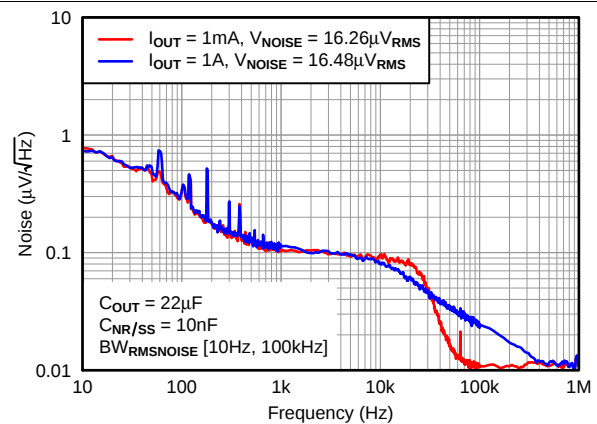


Figure 20. Output Spectral Noise Density vs Output Current

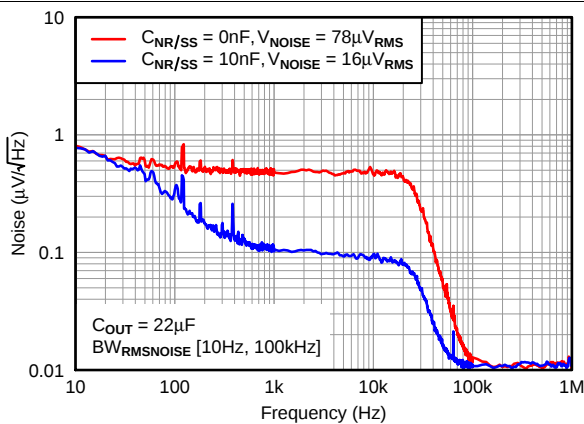


Figure 21. Output Spectral Noise Density vs $C_{NR/SS}$

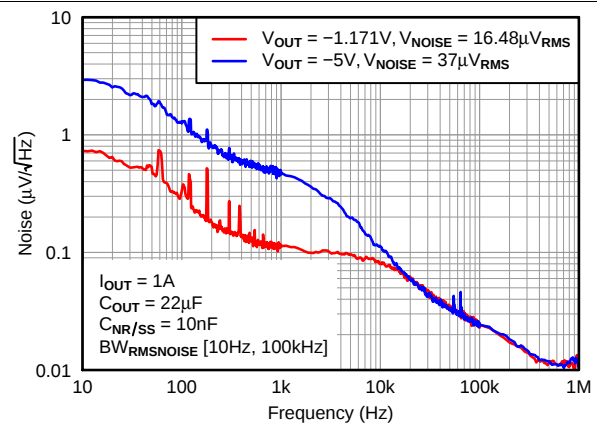


Figure 22. Output Spectral Noise Density vs $V_{OUT(nom)}$

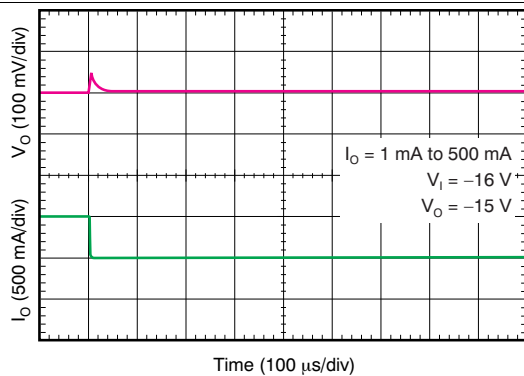


Figure 23. Load Transient

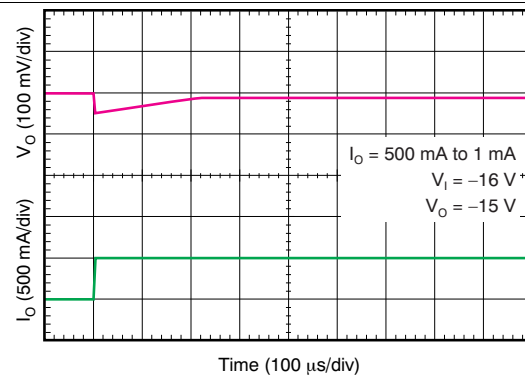


Figure 24. Load Transient

Typical Characteristics (continued)

At $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$, $|V_{IN}| = |V_{OUT(nom)}| + 1\text{ V}$ or $|V_{IN}| = 3\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 22\text{ }\mu\text{F}$, $C_{OUT} = 22\text{ }\mu\text{F}$, $C_{NR/SS} = 0\text{ nF}$, and the FB pin tied to OUT, unless otherwise noted.

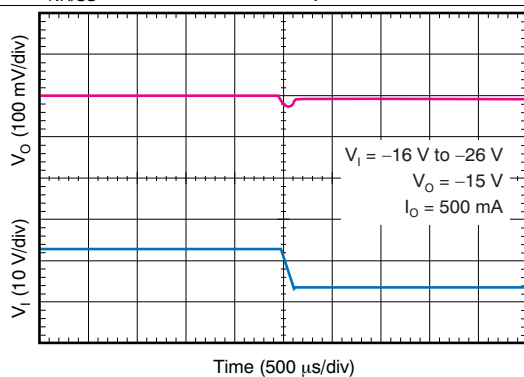


Figure 25. Line Transient

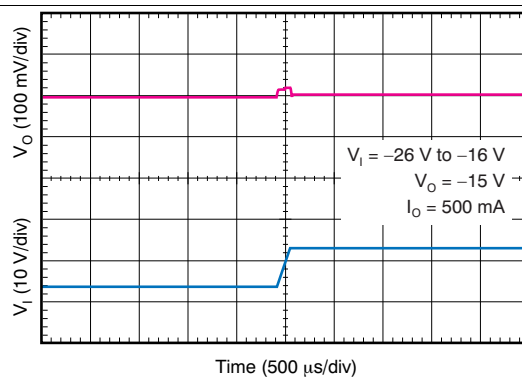


Figure 26. Line Transient

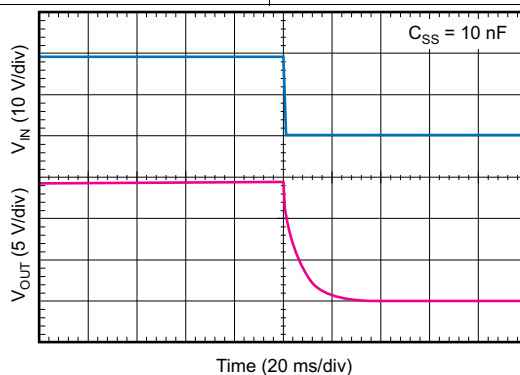


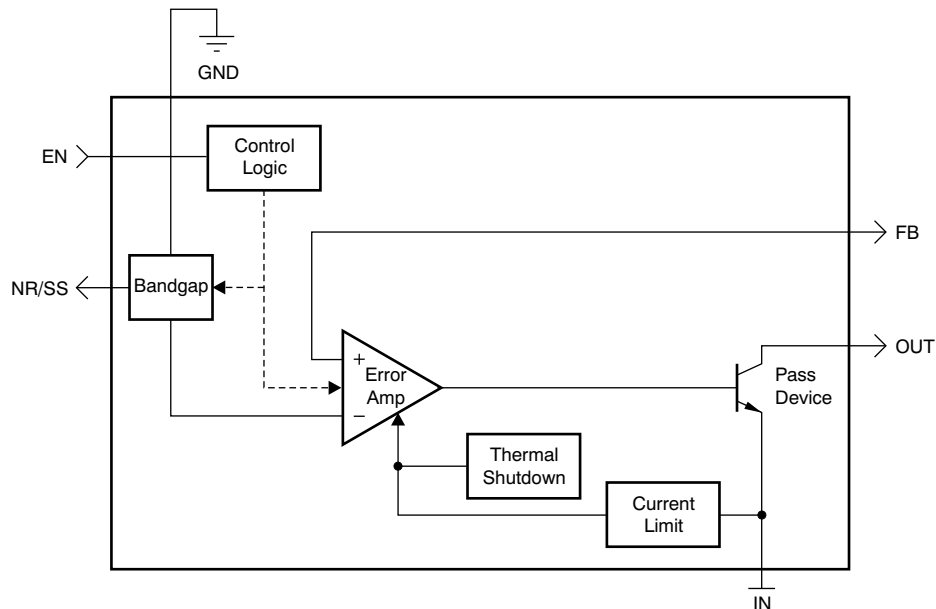
Figure 27. Capacitor-Programmable Soft-Start

7 Detailed Description

7.1 Overview

The TPS7A33 belongs to a family of new-generation linear regulators that use an innovative bipolar process to achieve ultralow-noise and very high PSRR levels at a wide input voltage and current range. These features, combined with the external heatsink-capable, high thermal performance TO-220 package, make this device ideal for high-performance analog applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal Current Limit

The fixed internal current limit of the TPS7A33xx family helps protect the regulator during fault conditions. The maximum amount of current the device can source is the current limit (1.9 A, typical), and it is largely independent of output voltage. For reliable operation, do not operate the device in current limit for extended periods of time.

Feature Description (continued)

7.3.2 Enable Pin Operation

The TPS7A33 provides a dual-polarity enable pin (EN) that turns on the regulator when $|V_{EN}| > 2$ V, whether the voltage is positive or negative, as shown in Figure 28.

This functionality allows for different system power management topologies; for example:

- Connecting the EN pin directly to a negative voltage, such as V_{IN} , or
- Connecting the EN pin directly to a positive voltage, such as the output of digital logic circuitry.

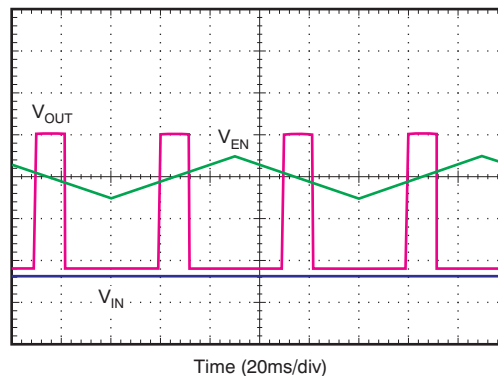


Figure 28. Enable Pin Positive and Negative Threshold

7.3.3 Programmable Soft-Start

The NR capacitor also acts as a soft-start capacitor to slow down the rise time of the output. The output rise time, when using an NR capacitor, is governed by Equation 1.

$$t_{SS} \text{ (ms)} = 1.2 \times C_{NR} \text{ (nF)} \quad (1)$$

In Equation 1, t_{SS} is the soft-start time in milliseconds, and $C_{NR/SS}$ is the capacitance at the NR pin in nanofarads.

Figure 29 shows the start-up voltage waveforms versus $C_{NR/SS}$.

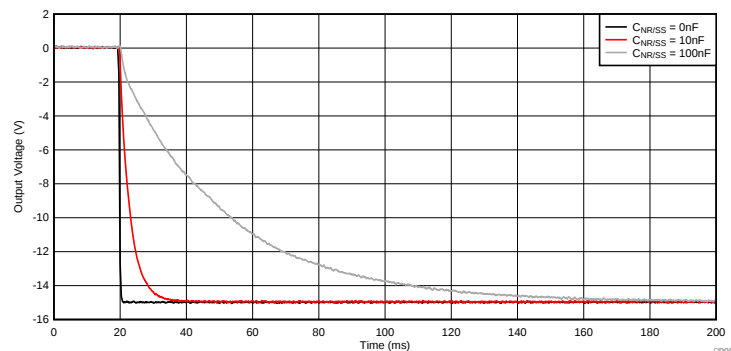


Figure 29. Start-Up vs $C_{NR/SS}$

7.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Feature Description (continued)

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to a maximum of 125°C. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A33 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A33 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage has previously exceeded the UVLO rising voltage and has not decreased below the UVLO falling threshold.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- $|V_{EN}| > |V_{(HI)}|$
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

7.4.2 Dropout Operation

If the input voltage magnitude is lower than the nominal output voltage magnitude plus the specified dropout voltage magnitude, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage magnitude is the same as the input voltage magnitude minus the dropout voltage magnitude. The transient performance of the device is significantly degraded because the pass device (as a bipolar junction transistor, or BJT) is in saturation and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- $|V_{EN}| < |V_{(HI)}|$
- The device junction temperature is greater than the thermal shutdown temperature.

[Table 1](#) shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$ V_{IN} > \{ V_{OUT(nom)} + V_{DO} , V_{IN(min)} \}$	$ V_{EN} > V_{(HI)} $	$I_{OUT} < I_{CL}$	$T_J < 125^{\circ}\text{C}$
Dropout mode	$ V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO} $	$ V_{EN} > V_{(HI)} $	—	$T_J < 125^{\circ}\text{C}$
Disabled mode (any true condition disables the device)	—	$ V_{EN} < V_{(HI)} $	—	$T_J > 165^{\circ}\text{C}$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Adjustable Operation

The TPS7A3301 has an output voltage range of $-V_{REF}$ to -33 V. The nominal output voltage of the device is set by two external resistors, as shown in [Figure 32](#).

R_1 and R_2 can be calculated for any output voltage range using [Equation 2](#). To ensure stability under no-load conditions at $V_{OUT} > V_{REF}$, this resistive network must provide a current equal to or greater than $5\text{ }\mu\text{A}$.

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right), \text{ where } \frac{|V_{REF(max)}|}{R_2} > 5\text{ }\mu\text{A} \quad (2)$$

If greater voltage accuracy is required, consider the output voltage offset contributions because of the feedback pin current and use 0.1%-tolerance resistors.

[Table 2](#) shows the resistor combinations to achieve a few of the most common rails using commercially available, 0.1%-tolerance resistors to maximize nominal voltage accuracy while adhering to the formula shown in [Equation 2](#).

Table 2. Suggested Resistors For Common Voltage Rails

V_{OUT} (V)	R_1	R_2 (k Ω)	$V_{OUT}/(R_1+R_2)$ (μA)	NOMINAL ACCURACY
-1.171	0 Ω	∞	0	$\pm 1.5\%$
-1.8	76.8 k Ω	143	8.18	$\pm(1.5\% + 0.08\%)$
-3.3	200 k Ω	110	10.64	$\pm(1.5\% + 0.13\%)$
-5	332 k Ω	102	11.48	$\pm(1.5\% + 0.5\%)$
-10	1.62 M Ω	215	5.44	$\pm(1.5\% + 0.23\%)$
-12	1.5 M Ω	162	7.22	$\pm(1.5\% + 0.29\%)$
-15	1.24 M Ω	105	11.15	$\pm(1.5\% + 0.18\%)$
-18	3.09 M Ω	215	5.44	$\pm(1.5\% + 0.19\%)$
-24	1.15 M Ω	59	19.84	$\pm(1.5\% + 0.21\%)$

8.1.2 Capacitor Recommendations

Low equivalent series resistance (ESR) capacitors should be used for the input, output, noise reduction, and bypass capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved overtemperature performance, while ceramic X5R capacitors are the most cost-effective and are available in higher values.

NOTE

High-ESR capacitors may degrade PSRR and affect stability.

8.1.3 Input and Output Capacitor Requirements

The TPS7A33 family of negative, high-voltage linear regulators achieve stability with a minimum input and output capacitance of 10 μF ; however, TI highly recommends using a 47- μF capacitor to maximize AC performance.

8.1.4 Noise Reduction and Feed-Forward Capacitor Requirements

Although the noise-reduction ($C_{\text{NR/SS}}$) and feed-forward (C_{FF}) capacitors are not needed to achieve stability, TI highly recommends using a 10-nF feed-forward capacitor and a 1- μF noise-reduction capacitor to minimize noise and maximize AC performance.

The feed-forward capacitor can also provide a soft-start effect, as detailed in the application note, *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator*, [SBVA042](#) (available for download from the TI website). [Figure 30](#) shows device start-up with no $C_{\text{NR/SS}}$, $C_{\text{FF}} = 10 \text{ nF}$, $V_{\text{IN}} = -16 \text{ V}$, and $V_{\text{OUT}} = -15 \text{ V}$.

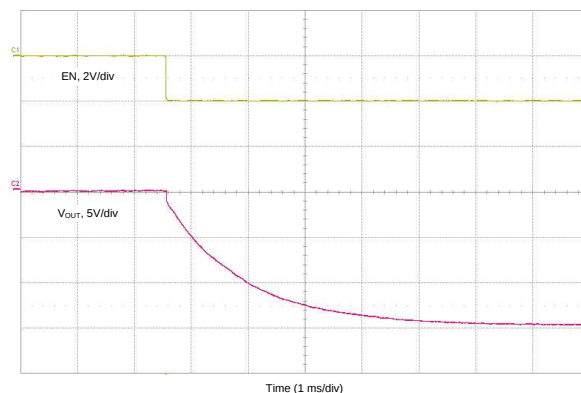


Figure 30. Start-up With a Feed-Forward Capacitor

8.1.5 Post DC-DC Converter Filtering

Most of the time, the voltage rails available in a system do not match the voltage specifications demanded by one or more of its circuits; these rails must be stepped up or down, depending on specific voltage requirements.

DC-DC converters are the preferred solution to stepping up or down a voltage rail when current consumption is not negligible. These devices offer high efficiency with minimum heat generation, but they have one primary disadvantage: they introduce a high-frequency component, and the associated harmonics, on top of the DC output signal.

If not filtered properly, this high-frequency component degrades analog circuitry performance, and reduces overall system accuracy and precision.

The TPS7A33 offers a wide-bandwidth, very-high power-supply rejection ratio (PSRR). This specification makes it ideal for post DC-DC converter filtering, as shown in [Figure 31](#). TI highly recommends using the maximum performance schematic shown in [Figure 32](#). Also, verify that the fundamental frequency (and its first harmonic, if possible) is within the bandwidth of the regulator PSRR, shown in [Figure 16](#).

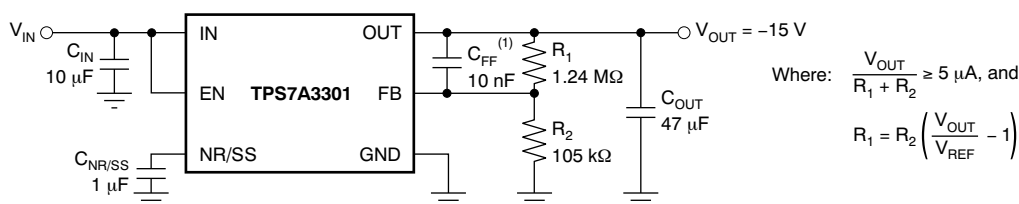
8.1.11 Power for Precision Analog

One of the primary TPS7A33 applications is to provide ultralow-noise voltage rails to high-performance analog circuitry in order to maximize system accuracy and precision.

The TPS7A33 family of negative, high-voltage linear regulators provides ultralow noise, positive and negative voltage rails to high-performance analog circuitry such as operational amplifiers, ADCs, DACs, and audio amplifiers.

Because of the ultralow noise levels at high voltages, analog circuitry with high-voltage input supplies can be used. This characteristic allows for high-performance analog solutions to optimize the voltage range, thus maximizing system accuracy.

8.2 Typical Application



- A. Refer to application report *Pros and Cons of Using a Feed-forward Capacitor with a Low-Dropout Regulator*, [SBVA042](#).

Figure 32. Adjustable Operation for Maximum AC Performance

8.2.1 Design Requirements

The design goals for this example are $V_{IN} = -16\text{ V}$, $V_{OUT} = -15\text{ V}$, and $I_{OUT} = 1\text{ A}$ maximum. The design must optimize transient response, and the input supply comes from a supply on the same printed-circuit board (PCB).

8.2.2 Detailed Design Procedure

The design space consists of C_{IN} , C_{OUT} , $C_{SS/NR}$, R_1 , R_2 , and the circuit shown in [Figure 32](#).

The first step when designing with a linear regulator is to examine the maximum load current along with the input and output voltage requirements to determine if the device thermal and dropout voltage requirements can be met. At 1 A, the input dropout voltage of the TPS7A33xx family is a maximum of 800 mV overtemperature; thus, the dropout headroom is sufficient for operation over both input and output voltage accuracy. Keep in mind that operating an LDO close to the dropout limit reduces AC performance, but has the benefit of reducing the power dissipation across the LDO.

The maximum power dissipated in the linear regulator is the maximum voltage drop across the pass element from the input to the output multiplied by the maximum load current. In this example, the maximum voltage drop across in the pass element is $(-16\text{ V}) - (-15\text{ V})$, giving us a $V_{DROP} = 1\text{ V}$. The power dissipated in the pass element is calculated by taking this voltage drop multiplied by the maximum load current. For this example, the maximum power dissipated in the linear regulator is approximately 1 W, and does not include the power consumed by the V_{BIAS} rail.

Once the power dissipated in the linear regulator is known, the corresponding junction temperature rise can be calculated. To calculate the junction temperature rise above ambient, the power dissipated must be multiplied by the junction-to-ambient thermal resistance. For thermal resistance information, refer to [Thermal Information](#) and [Thermal Performance and Heat Sink Selection](#). For this example, using the RGW package, the maximum junction temperature rise is calculated to be 17.2°C. The maximum junction temperature rise is calculated by adding junction temperature rise to the maximum ambient temperature, which is 85°C. In this example, then, the maximum junction temperature is 102.2°C. The maximum junction temperature must be less than 125°C for reliable operation. Additional ground planes, added thermal vias, and air flow all combine to lower the maximum junction temperature.

To ensure an accurate output voltage, R_1 and R_2 must also be found, and the current through these resistors must be greater than 5 µA to ensure that the leakage into the device does not affect the accuracy. Using 1% resistors, and setting R_1 to 1 MΩ to minimize the current leakage while continuing to hold it above 5 µA, then use [Equation 3](#) to calculate the proper value for R_2 and the divider current.

Typical Application (continued)

$$R2 = \frac{(R1 \cdot V_{REF})}{V_O - V_{REF}} = 85 \text{ k}\Omega \quad \text{and} \quad I_{DIVIDER} = \frac{V_O}{R1 + R2} = 13.8 \text{ }\mu\text{A} \quad (3)$$

For C_{IN} , assume that the -16 V supply has some inductance, and is placed several inches away from the PCB. For this case, select a $10\text{-}\mu\text{F}$ ceramic input capacitor to ensure that the input inductance is negligible to the regulator control loop while also keeping the physical size and cost of the capacitor low because it is a standard-value capacitor. C_{OUT} is set at $20 \text{ }\mu\text{F}$ for AC performance, C_{FF} is set at 10 nF , and C_{NR} is set at 100 nF for optimal noise performance and to minimize the size of the external capacitor.

8.2.3 Application Curves

Figure 33 and Figure 34 show typical application performance for PSRR and spectral noise density, respectively, versus $C_{NR/SS}$ with C_{FF} .

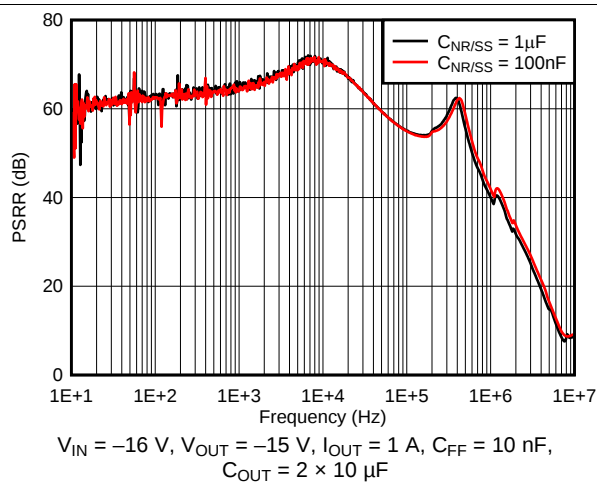


Figure 33. Power-Supply Rejection Ratio vs $C_{NR/SS}$ With C_{FF}

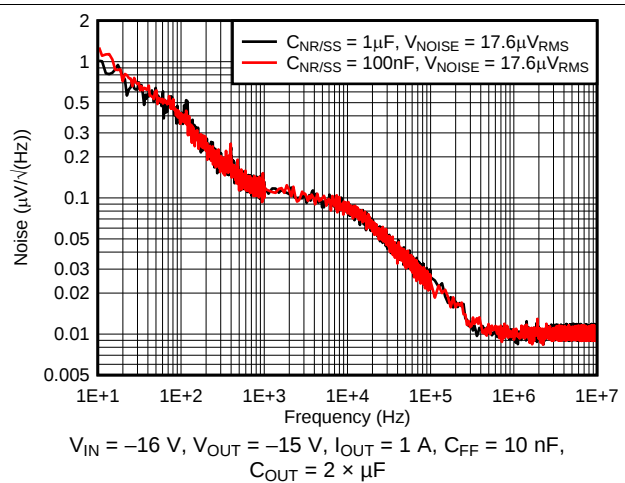


Figure 34. Output Spectral Noise Density vs $C_{NR/SS}$ With C_{FF}

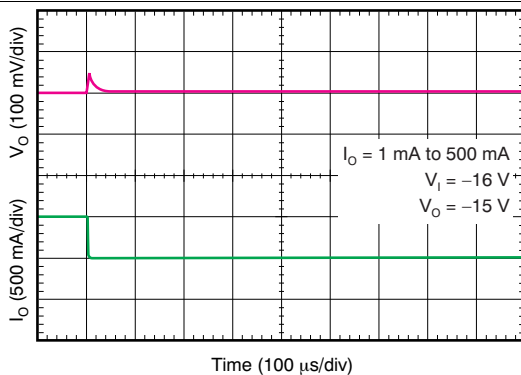


Figure 35. Load Transient

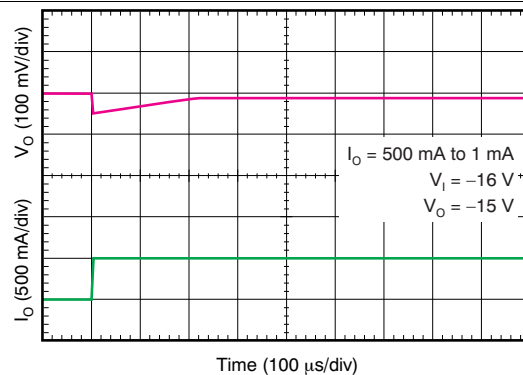
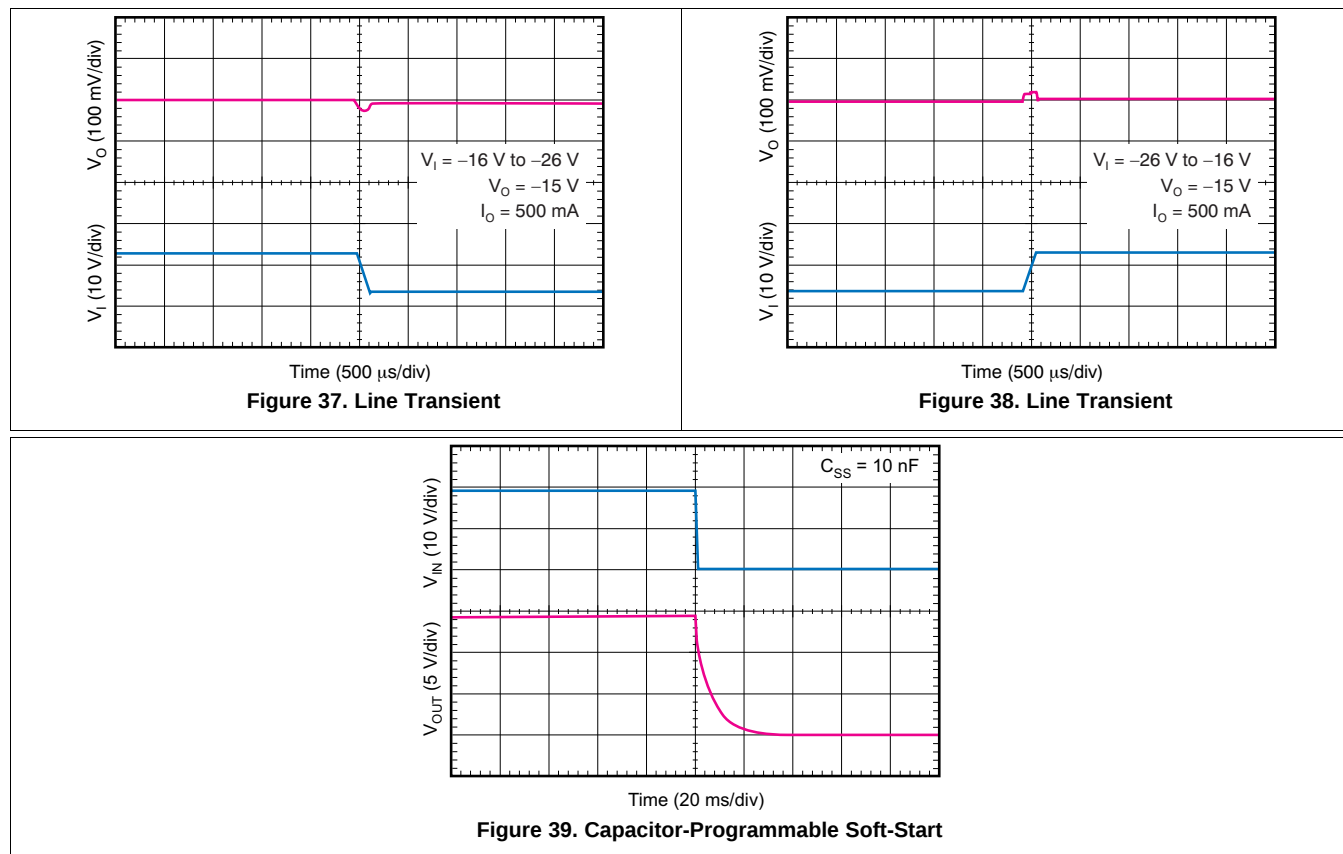


Figure 36. Load Transient

Typical Application (continued)



8.3 Do's and Don'ts

Place at least one low ESR 10-μF capacitor as close as possible to both the IN and OUT terminals of the regulator to the GND pin.

Provide adequate thermal paths away from the device.

Do not place the input or output capacitor more than 10 mm away from the regulator.

Do not exceed the absolute maximum ratings.

Do not float the EN pin.

Do not resistively or inductively load the NR/SS pin.

9 Power Supply Recommendations

The input supply for the LDO must be within its recommended operating conditions, from -35 V to -3 V . The input voltage must provide adequate headroom for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

Layout is a critical part of good power-supply design. Several signal paths that conduct fast-changing currents or voltages can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with a X5R or X7R dielectric.

10.1 Layout Guidelines

10.1.1 Improve PSRR and Noise Performance

To improve AC performance such as PSRR, output noise, and transient response, TI recommends designing the board with separate planes for IN, OUT, and GND. The IN and OUT planes should be isolated from each other by a GND plane section. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and equivalent series resistance (ESR) must be minimized in order to maximize performance and ensure stability. Every capacitor (C_{IN} , C_{OUT} , $C_{NR/SS}$, C_{FF}) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because they may impact system performance negatively and even cause instability.

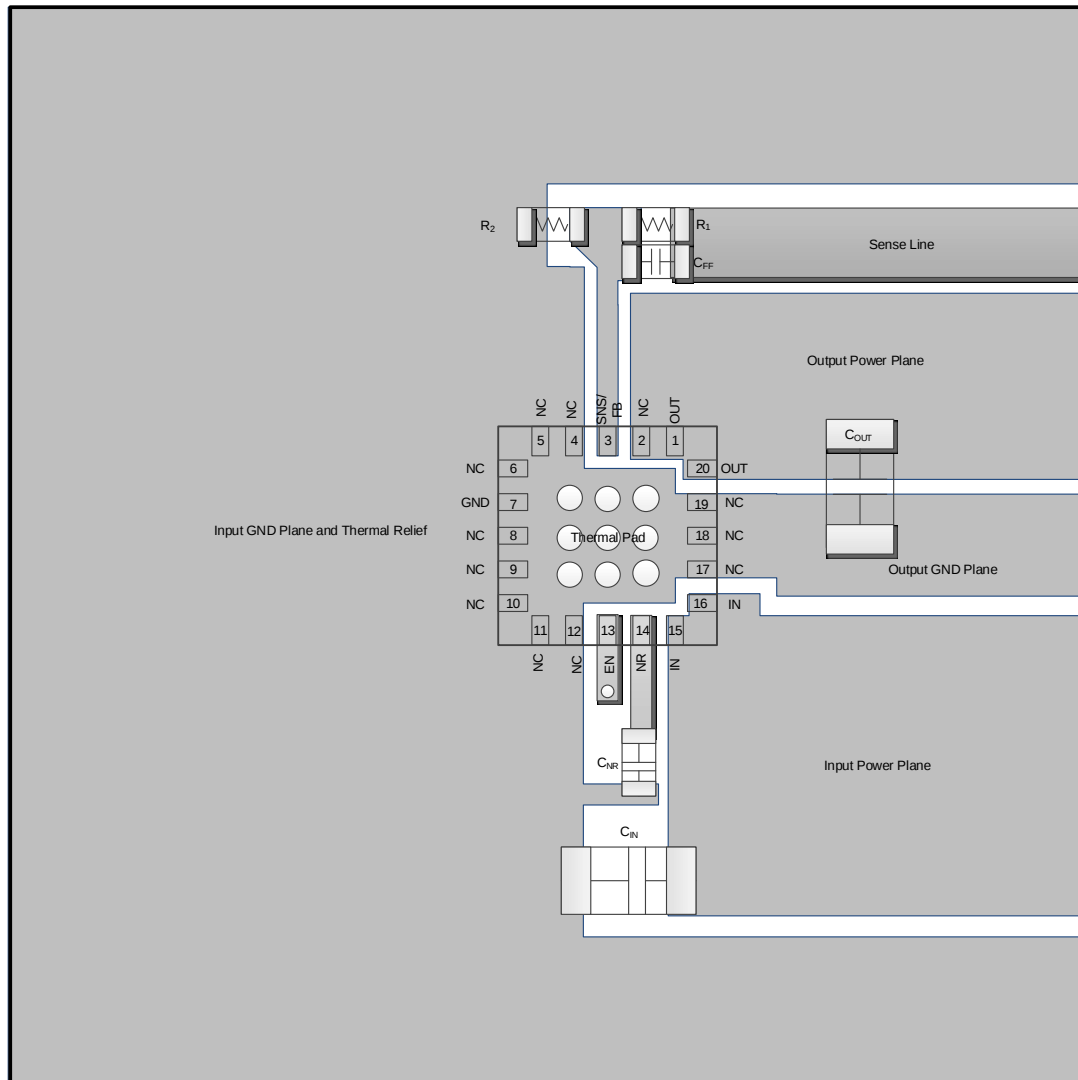
10.2 Layout Example

It may be possible to obtain acceptable performance with alternative PCB layouts; however, the layout shown in [Figure 41](#) and the schematic shown in [Figure 42](#) have been shown to produce good results and are meant as a guideline.

TPS7A33

SBVS169D –DECEMBER 2011–REVISED APRIL 2015

www.ti.com



Scale is 8:1
This figure shows a 1x1 layout; expand to 3x3 or at least 2x2.

Figure 40. TPS7A33 5-mm × 5-mm QFN-20 Layout Guideline

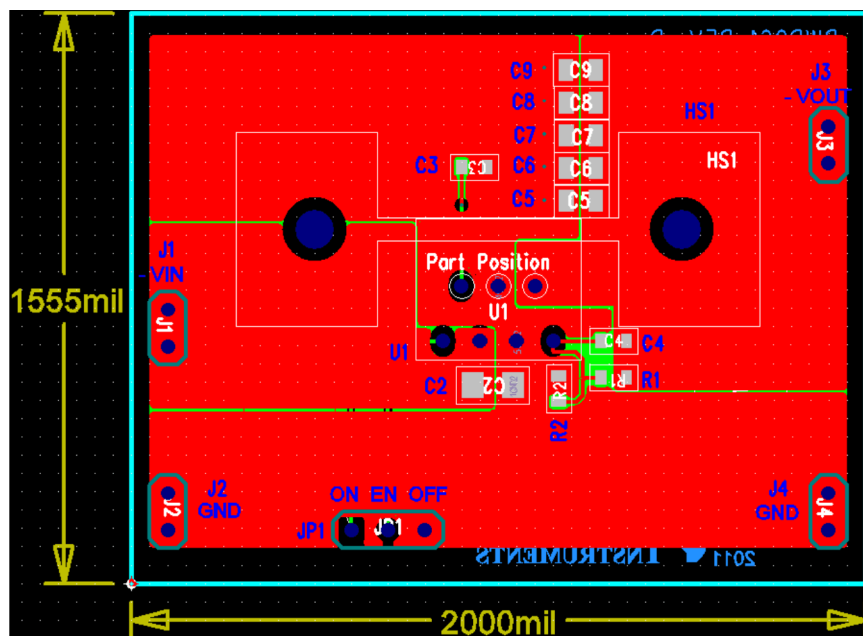


Figure 41. TPS7A33 TO-220 EVM PCB Layout Example: Top Layer

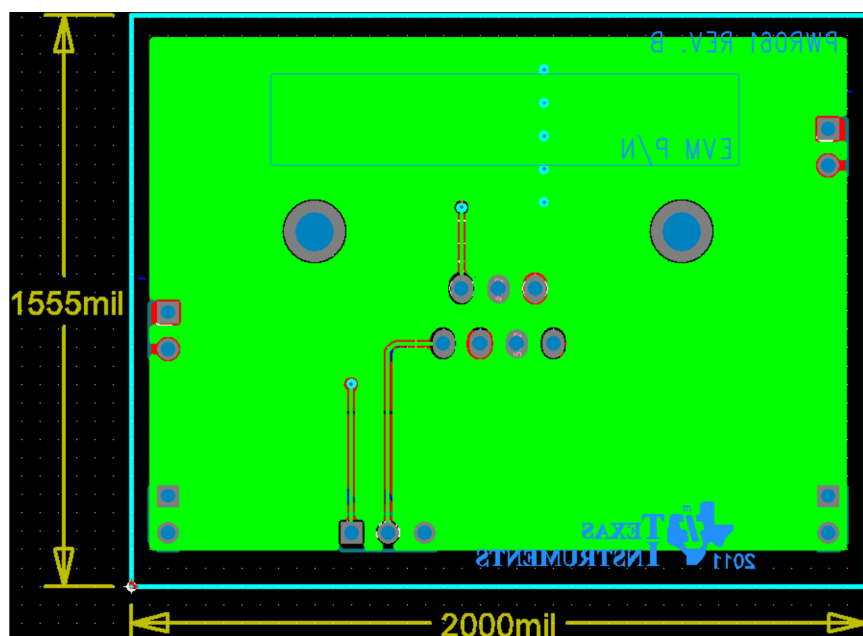


Figure 42. TPS7A33 TO-220 EVM PCB Layout Example: Bottom Layer

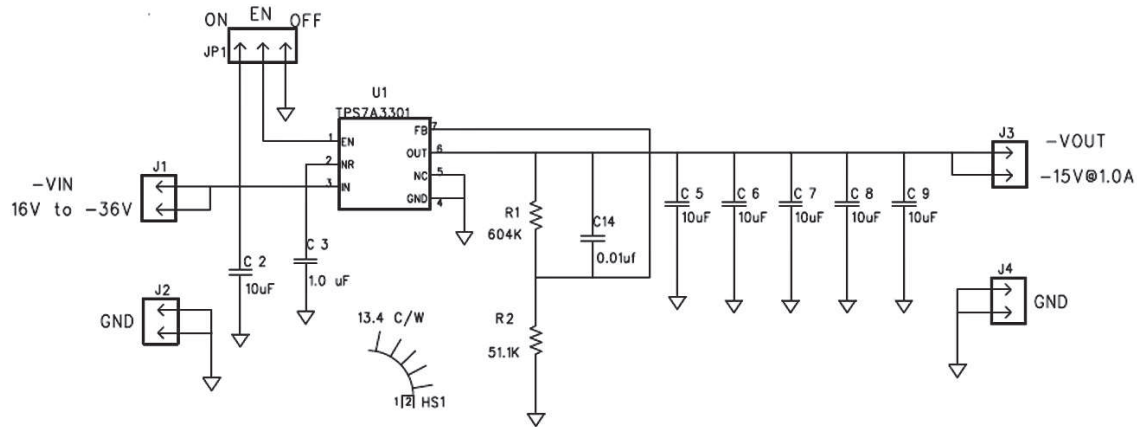


Figure 43. Schematic for TPS7A33 TO-220 EVM PCB Layout Example

10.3 Thermal Performance and Heat Sink Selection

The primary TPS7A33 application is to provide ultralow-noise voltage rails to high-performance analog circuitry in order to maximize system accuracy and precision. The high-current and high-voltage characteristics of this regulator means that, often enough, high power (heat) is dissipated from the device itself. This heat, if dissipated into the PCB (as is the case with SMT packages), creates a temperature gradient in the surrounding area that causes nearby components to react to this temperature change (drift). In high-performance systems, such drift may degrade overall system accuracy and precision.

Compared to surface-mount packages, the TO-220 (KC) package allows for an external heat sink to be used to maximize thermal performance and keep heat from dissipating into the PCB.

The heat generated by the device is a result of the power dissipation, which depends on input voltage and load conditions. Power dissipation (P_D) can be approximated by calculating the product of the output current times the voltage drop across the output pass element, as shown in [Equation 4](#):

$$P_D = (V_{IN} - V_{OUT}) I_{OUT} \quad (4)$$

Heat flows from the device to the ambient air through many paths, each of which represents resistance to the heat flow; this effect is called thermal resistance.

The total thermal resistance of a system is defined by: $\theta_{JA} = (T_J - T_A)/P_D$; where: θ_{JA} is the thermal resistance (in $^{\circ}\text{C}/\text{W}$), T_J is the allowable junction temperature of the device (in $^{\circ}\text{C}$), T_A is the maximum temperature of the ambient cooling air (in $^{\circ}\text{C}$), and P_D is the amount of power (heat) dissipated by the device (in W).

Whenever a heat sink is installed, the total thermal resistance (θ_{JA}) is the sum of all the individual resistances from the device, going through its case and heatsink to the ambient cooling air ($\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$). Realistically, only two resistances can be controlled: θ_{CS} and θ_{SA} . Therefore, for a device with a known θ_{JC} , θ_{CS} and θ_{SA} become the main design variables in selecting a heat sink.

The thermal interface between the case and the heat sink (θ_{CS}) is controlled by selecting the correct heat-conducting material. Once the θ_{CS} is selected, the required thermal resistance from the heat sink to ambient is calculated by the following equation: $\theta_{SA} = [(T_J - T_A)/P_D] - [\theta_{JC} + \theta_{CS}]$. This information allows the most appropriate heat sink to be selected for any particular application.

10.4 Package Mounting

The TO-220 (KC) 7-lead, straight-formed package lead spacing poses a challenge when creating a suitable PCB footprint without bending the leads. Component forming pliers can be used to manually bend the package leads into a 7-lead stagger pattern with increased lead spacing that can be more easily used.

The TPS7A33 evaluation board layout can be used as a guideline on suitable PCB footprints, available at www.ti.com. Refer to the [TPS7A3301EVM-061 user's guide](#) for more information.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS7A33. The [TPS7A3301EVM-061 evaluation module](#) (and related [user's guide](#)) can be requested at the TI website through the product folders or purchased directly from the [TI eStore](#).

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS7A33 is available through the product folders under the *Tools & Software* tab.

11.1.2 Device Nomenclature

Table 3. Device Nomenclature⁽¹⁾

PRODUCT	V _{OUT}
TPS7A3301YYYZ	YYY is the package designator. Z is the tape and reel quantity (R = 3000, T = 250).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following (available for download at www.ti.com):

- *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator*, [SBVA042](#)
- *TPS7A3301EVM-061 Evaluation Module User's Guide*, [SLVU602](#)

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A3301RGWR	ACTIVE	VQFN	RGW	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PXQQ	Samples
TPS7A3301RGWT	ACTIVE	VQFN	RGW	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PXQQ	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A3301RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS7A3301RGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A3301RGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS7A3301RGWT	VQFN	RGW	20	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

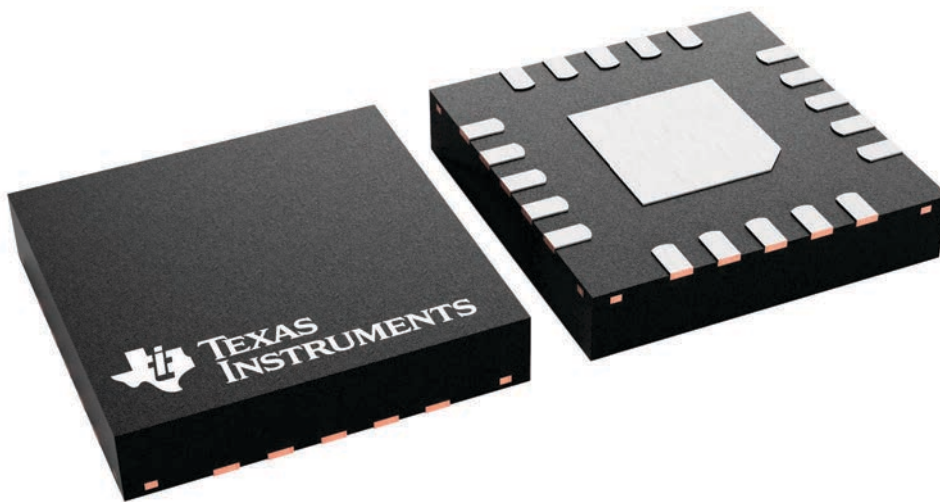
RGW 20

VQFN - 1 mm max height

5 x 5, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227157/A

VQFN - 1 mm max height

The drawing shows a 20-pin connector with the following dimensions and features:

- Overall Dimensions:** Width is 5.1 (4.9), and height is 5.1 (4.9).
- PIN 1 INDEX AREA:** A shaded rectangular area in the top-left corner.
- Top View:** Shows the 20 pins arranged in two rows of 10. The pin pitch is 2.6. The distance from the index area to the first pin is 1. The distance from the last pin to the edge is 10. The distance from the index area to the center of the pin array is 3.15 ± 0.1.
- Side View:** Shows the profile of the connector. The height of the pins is 1 MAX. The distance from the base to the top of the pins is 0.05 (0.00). The distance from the base to the top of the housing is 1. The distance from the base to the top of the pins is 0.05 (0.00).
- Bottom View:** Shows the 20 pins arranged in two rows of 10. The pin pitch is 2.6. The distance from the index area to the first pin is 1. The distance from the last pin to the edge is 10. The distance from the index area to the center of the pin array is 3.15 ± 0.1.
- Callouts:**
 - C:** A callout to the top view showing the seating plane and a 0.08 dimension.
 - SEATING PLANE:** A callout to the top view showing the seating plane.
 - SYMM:** A callout to the bottom view showing the center of symmetry.
 - PIN1 ID (OPTIONAL):** A callout to the bottom view showing the pin 1 identification area.
 - (0.1) TYP:** A callout to the side view showing the typical thickness of the pins.
- Feature Control Frames:**
 - Top view: 3.15 ± 0.1 (position), 2×2.6 (pitch), 6 (width), 10 (length).
 - Side view: 1 MAX (height), 0.05 (0.00) (distance from base to top of pins), 0.08 (distance from base to top of housing).
 - Bottom view: 16×0.65 (width), 2×2.6 (pitch), 5 (height), 11 (width), 15 (height), 20×0.36 (0.26) (width), 20×0.65 (0.45) (height).

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

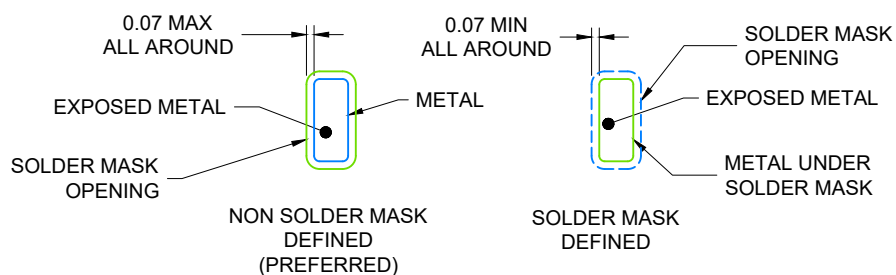
VQFN - 1 mm max height

Mechanical drawing of a PCB layout showing dimensions and component placement. The drawing includes a central square area with a blue border, surrounded by various components and dimensions.

Key dimensions and features:

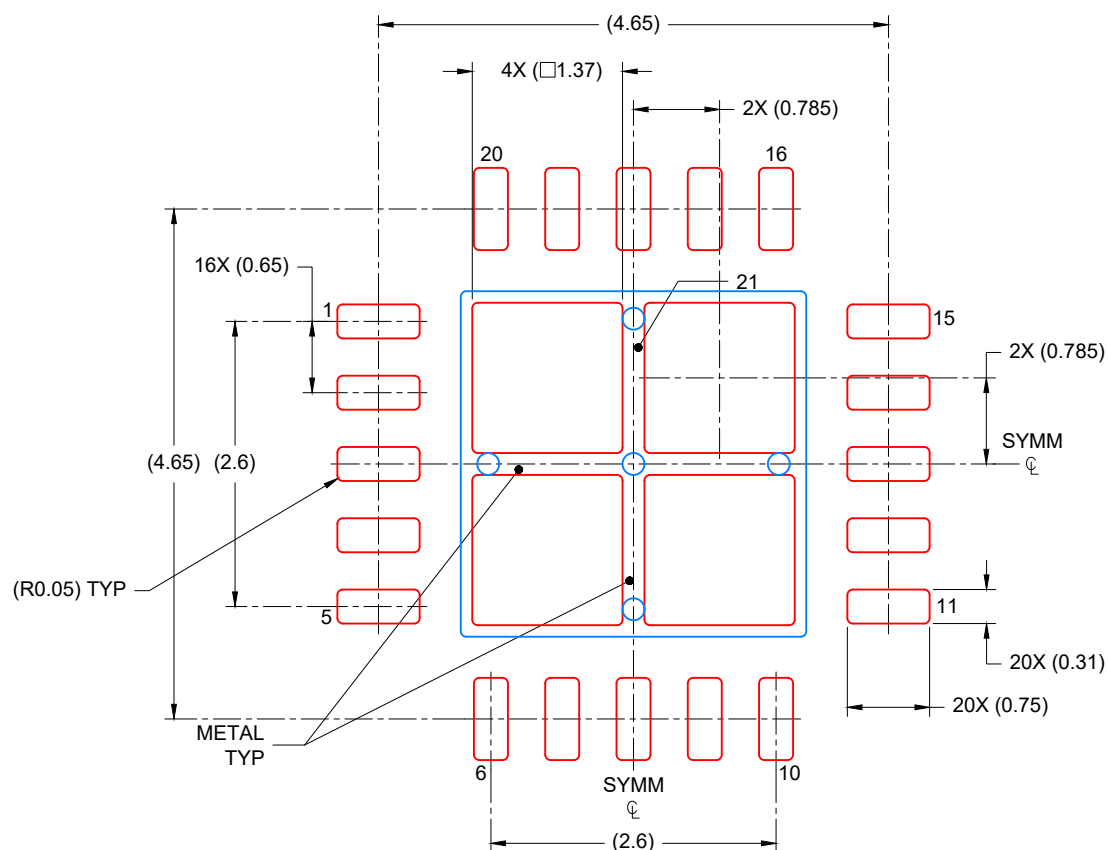
- Overall width: 4.65
- Overall height: 4.65
- Central square area: 3.15 (width) x 3.15 (height)
- Top row of components: 20 (width) x 16 (height)
- Bottom row of components: 6 (width) x 10 (height)
- Left side components: 16X (0.65) (height) x 1 (width)
- Right side components: 15 (width) x 11 (height)
- Dimensions: 1.325, 2.6, 2.0X (0.31), 20X (0.75)
- Labels: (R0.05) TYP, (Ø0.2) VIA TYP, SYMM, 21, 15, 11, 10, 6, 5, 1, 20, 16

SCALE: 15X



4219039/A 06/2018

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 15X

4219039/A 06/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.